

Jitter Test Methods for 200GAUI-4 and 400GAUI-8

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IEEE P802.3bs Task Force
Electrical Ad hoc, October 3, 2016

- Jitter test method for 200GAUI-4 and 400GAUI-8 in the current draft is largely based on Clause 94 with a few modifications
 - Baseline was 100GBASE-KP4 in Clause 94 (li_3bs_01a_0315.pdf)
 - CRJ and CDJ (as derived from J5 and J6) was changed to JRMS and J5 (hegde_3bs_03_0316.pdf, hegde_3bs_03_0516.pdf)
 - J5 was changed to J4 (dawe_3bs_0916.pdf, slide 11)

- This jitter test method in Clause 94 was once compared with the jitter test method in Clause 92 (healey_3bs_01_0915.pdf)
 - The conclusion was that Clause 94 was preferred, because dual-Dirac fitting in Clause 92 is not accurate (moore_3bj_01_0114.pdf)

- However, some discussion was not enough in the comparison
 - Both test methods exclude DDJ, but in a different way
 - The methods to exclude DDJ are obvious, but may not be discussed enough

Comparison of methods

	100GBASE-CR4/KR4	100GBASE-KP4
Reference	92.8.3.8.2	94.3.12.6
Test pattern	<u>PRBS9</u>	<u>JP03A (clock pattern with 2 UI period)</u>
Data acquisition	Histogram of zero crossing times for <u>isolated rising and falling transitions</u>	1-shot capture and post-processing (filtering, average UI, and error calculations)

- Both methods clearly exclude DDJ, but in a different way
 - Clause 92 measures **isolated transitions** in PRBS9 to exclude DDJ
 - Clause 94 uses **clock pattern** JP03A to exclude DDJ

- If we switch to PRBS13Q, we should revisit Clause 92 method, because PRBS13Q has a lot of DDJ similar to PRBS9

■ DDJ is excluded from PRBS9

- Jitter is measured on each of **two specific transitions** in a PRBS9 pattern
 - Transition between five zeros and four ones
 - Transition between nine ones and five zeros
- EBUJ and ERJ are derived by fitting dual-Dirac model

92.8.3.8.2 Effective bounded uncorrelated jitter and effective random jitter

Effective bounded uncorrelated jitter and effective random jitter are measured on each of two specific transitions in a PRBS9 pattern (see 83.5.10). The two transitions occur in the sequence of five zeros and four ones and nine ones and five zeros, respectively. The sequences are located at bits 10 to 18 and 1 to 14, respectively, where bits 1 to 9 are the run of nine ones.

- The jitter components are determined according to the following method. Acquire a horizontal histogram of a transition around the zero-crossing point. The number of acquired samples should be sufficiently large to yield consistent measurement results. Designate the total number of samples as NS , the number of bins as NB , the number of samples in each bin as N_i where i is the bin number from 1 to NB , and the sample time corresponding with the center of each bin as t_i .
- Create two cumulative distribution curves $CDFL_i$ and $CDFR_i$ according to Equation (92–10) and

EBUJ and ERJ are obtained by fitting the histogram to dual Dirac model

■ We can exclude DDJ from PRBS13Q in a similar way

- But, we can skip the remaining process of fitting to dual-Dirac model

- Measure jitter on each of **several specific transitions** in PRBS13Q in order to exclude DDJ
 - Get a horizontal histogram for each of specific transitions in PRBS13Q
 - Candidates for those specific transitions are provided in the next slide
 - Derive JRMS and J4 from the histogram using the method in 120D.3.1.1
 - The method to derive EBUJ and ERJ as in Clause 92 is discouraged
 - Because EBUJ may be converted to ERJ depending on the distribution type (moore_3bj_01_0114.pdf and healey_3bs_01_0915.pdf)
 - JRMS and J4 must meet the specification for each of specific transitions

Candidates of Specific Transitions in PRBS13Q

Label	Description	Gray coded PAM4 symbols	PAM4 symbol index			Threshold level	Binary levels		
			First	Transition	Last		MSB	LSB	
REF	Reference for index After seed value (S0 thru S12) of 0000010101011 (This is same as example sequence in 120.5.11.2.3)	1031320220 1111301031 2123121001 2102121023 131112	1			46			
R03	Rise transition from 0 to 3	10000 3 30	555	559	560	562	$(V_0+V_3)/2$	Rise Rise	
F30	Fall transition from 3 to 0	23333 0 01	8185	8189	8190	1 (8192)	$(V_0+V_3)/2$	Fall Fall	
R12	Rise transition from 1 to 2	0111111 2 222221	2363	2369	2370	2376	$(V_1+V_2)/2$	Rise Fall	
F21	Fall transition from 2 to 1	022222 1 13	8114	8119	8120	8122	$(V_1+V_2)/2$	Fall Rise	
R01	Rise transition from 0 to 1	100000 1 13	5560	5565	5566	5568	$(V_0+V_1)/2$		Rise
F10	Fall transition from 1 to 0	21111 0 03	1717	1721	1722	1724	$(V_0+V_1)/2$		Fall
R23	Rise transition from 2 to 3	32222 3 30	5549	5553	5554	5556	$(V_2+V_3)/2$		Rise
F32	Fall transition from 3 to 2	033333 2 222223	6459	6464	6465	6471	$(V_2+V_3)/2$		Fall
R02	Rise transition from 0 to 2	10000 2 23	1991	1995	1996	1998	$(V_0+V_2)/2$	Rise	
F20	Fall transition from 2 to 0	122222 0 000002	6007	6012	6013	6019	$(V_0+V_2)/2$	Fall	
R13	Rise transition from 1 to 3	011111 3 31	7049	7054	7055	7057	$(V_1+V_3)/2$	Rise	
F31	Fall transition from 3 to 1	23333 1 12	6630	6634	6635	6637	$(V_1+V_3)/2$	Fall	

V_0, V_1, V_2, V_3 are mean signal levels defined in 120D.3.1.2.1.

- When Tx circuit is binary (i.e. MSB+LSB)
 - MSB and LSB may be driven by different clock buffers
 - If jitter on MSB and jitter on LSB are
 - Positively correlated, then
 - R03 and F30 (same transition on MSB and LB) will be the worst
 - Negative correlated, then
 - R12 and F21 (opposite transition on MSB and LSB) will be the worst
 - Not correlated, then
 - R03, F30, R12, and F21 will be the worst
- When Tx circuit is not binary (e.g. using thermometer code)
 - Any of 12 types of transition could be the worst
- Hence,
 - R03, F30, R12, and F21 should be mandatory
 - The other 8 types of transitions may be optional (or mandatory as well)

- If the test pattern has a lot of DDJ, I recommend the above method to exclude DDJ, but the method is rather complicated

- Another option is just to use more clock test patterns:
 - Measure jitter on each of the following 6 test patterns
 - JP03A a repeating {0,3} sequence of PAM4 symbols
 - JP12A a repeating {1,2} sequence of PAM4 symbols
 - JP01A a repeating {0,1} sequence of PAM4 symbols
 - JP23A a repeating {2,3} sequence of PAM4 symbols
 - JP02A a repeating {0,2} sequence of PAM4 symbols
 - JP13A a repeating {1,3} sequence of PAM4 symbols
 - Last 4 patterns can be measured at differential 0V after AC coupling
 - Lack of DC balance is probably OK, but may cause some potential issue
 - This option will provide wider test coverage than testing only JP03A
 - JP03A and JP12A should be mandatory
 - JP01A, JP23A, JP02A, and JP13A may be optional (or mandatory as well)

■ Option A

- Measure jitter on several specific transitions in PRBS13Q (slide 4)

■ Option B

- Measure jitter on more clock test patterns including JP12A (slide 7)

■ Option C (no change)

- Measure jitter on only JP03A

■ EOJ is measured for JP03B

- It was changed back from PRBS13Q (healey_3bs_02_0516.pdf).
 - It is difficult to use PRBS13Q for EOJ measurement.

■ One option is just to use more EOJ test patterns:

■ Measure EOJ on each of the following 6 test patterns

- JP03B a repeating sequence of {0,3} x 15 times followed by {3,0} x 16 times
- JP12B a repeating sequence of {1,2} x 15 times followed by {2,1} x 16 times
- JP01B a repeating sequence of {0,1} x 15 times followed by {1,0} x 16 times
- JP23B a repeating sequence of {2,3} x 15 times followed by {2,3} x 16 times
- JP02B a repeating sequence of {0,2} x 15 times followed by {2,0} x 16 times
- JP13B a repeating sequence of {1,3} x 15 times followed by {3,1} x 16 times

■ Last 4 patterns may be measured at differential 0V after AC coupling

- Lack of DC balance is probably OK, but may cause some potential issue

■ This option will provide wider test coverage than testing only JP03B

■ JP03B and JP12B should be mandatory

- JP01B, JP23B, JP02B, and JP13B may be optional (or mandatory as well)

■ Option A

- Measure EOJ on multiple EOJ test patterns including JP12B (slide 9)

■ Option B (no change)

- Measure EOJ on only JP03B

- Pavel Zivny, Charles Moore: 802.3bj D2.1 Transmitter output jitter specification for NRZ PMDs
http://www.ieee802.org/3/bj/public/jul13/zivny_3bj_01a_0713.pdf
- Charles Moore: Experiments with simulated jitter
http://www.ieee802.org/3/bj/public/jan14/moore_3bj_01_0114.pdf
- Adam Healey: CDAUI-8 chip-to-chip transmitter output jitter requirements
http://www.ieee802.org/3/bs/public/15_09/healey_3bs_01_0915.pdf
- Raj Hegde, Magesh Valliappan, Adam Healey: CDAUI-8 Chip-to-chip Jitter Budget Proposal
http://www.ieee802.org/3/bs/public/16_03/hegde_3bs_03_0316.pdf
http://www.ieee802.org/3/bs/public/16_05/hegde_3bs_03_0516.pdf
- Adam Healey: CDAUI-8 chip-to-chip even-odd jitter measurements
http://www.ieee802.org/3/bs/public/16_05/healey_3bs_02_0516.pdf
- Piers Dawe: Jitter measurement and patterns for chip-to-chip 200GAUI-4 and 400GAUI-8
http://www.ieee802.org/3/bs/public/16_09/dawe_3bs_01_0916.pdf

Thank you