Electrical Interface Ad-hoc Meeting - Opening/Agenda

IEEE P802.3bs 400Gb/s Ethernet Task Force
4th September 2015

Opening

- The charter of the Electrical Interface Ad hoc is:
  - Address all issues in relation to the electrical interfaces to ensure progress towards a technically complete draft.
    - *Identify issues or omissions in the adopted Baselines*
    - *Find consensus now, rather than in comment resolution.*

- Next Ad-hoc Meeting
  - TBD

Patent Policy

- http://www.ieee802.org/3/patent.html

Agenda

Ad-hoc Opening/Agenda/Closing	Andre Szczepanek	szczepanek_01_090415_elect
120D/E TBD's in Draft 0.9		szczepanek_01_090415_elect
Options for CRU BW for 400GbE PAM4 PMDs*	Ali Ghiasi	ghiasi_01_082415_elect
CDAUI-8 Chip-to-Module (C2M) System Analysis	Stephane Dallaire Ben Smith	dallaire_01_090415_elect
Discussion time		szczepanek_01_090415_elect

* Held-over from 24Aug Ad-hoc call

“TBD”s in Draft 0.9

Annex 120D (C2C)

- EEE support
- Receiver Jitter Tolerance
- Device package model:
  - Single-ended device capacitance
  - Single-ended board capacitance
- Single-ended termination resistance

Annex 120E (C2M)

- Transition time
- Host stressed input pattern generator jitter characteristics (Table 120E-5)
- Single-ended voltage tolerance range (min)
- Module stressed input Pattern generator jitter characteristics (Table 120E-8)

Discussion

Summary from frlan_01_082415_elect

Summary

SEMTECH
GENNUM PRODUCTS

- **A standard 1z/2p CTLE should be adequate for most expected VSR channels in the host-to-module direction**
  - A 2-tap FIR in the host with some small pre-cursor de-emphasis can help to provide additional system margin
- **A channel at maximum VSR loss with higher ILD may require one of:**
  - Multi-tap FIR
    - This should not be mandatory for 56G-VSR-PAM4 as it is not the only option and forces too narrow a solution space
  - Higher performance reference CTLE
    - This needs further study but is likely the preferable solution to minimize module power
  - Note: The challenges of a host ASIC and a module retimer IC are fundamentally different. This drives different optimized solutions for each end the link

Recommendations from dallaire_01_090415_elect

Recommendations

- LFEQ+CTLE is **not enough** to close the link for higher loss channels
  - TXFIR is required to provide >2dB link margin
- We are proposing:
  - Reference Receiver: VSR-56G CTLE + Fixed LFEQ
  - Reference Transmitter: 2-tap TX FIR with 3 coarse settings; 0%, 5%, 10% pre-emphasis
- EH6
  - Discussions about link closure are centered around eye height requirements
  - Current EH6 requirements are unreasonably large for high loss channels
- TX SNDR
  - We need an agreed upon definition and model
  - At 29dB, it's a (potentially) large impairment, so it's critical that we model it consistently
- Eye Linearity (RLM)
  - We should consider tightening the requirement from current OIF value
- ILD
  - A suitable limit on ILD needs to be agreed upon

Options from mazzini_01_082415_elect

Options to be considered for CDAUI-8 C2M.

Six items (last one if strickly needed) that should be considered into C2M CDAUI-8, to allow TP1a EW/EH compliance and safe C2M link closure.

1. Define a more complex standard CTLE RX equalizer.
   - 3p2z or better.
   - Introduce a LF filter on the standard reference RX equalizer too?
2. Definition of continuos adaptation of module's CTLE RX.
   - Proposed +/- 1dB variation with respect to the previous CTLE gain setting with a minimum 1Hz frequency rate
3. Introduce a channel ILD deviation mask requirement.
   - Value to be agreed.
4. Improve TP0 TX SNDR requirement.
   - Value to be agreed (from 27 to 29dB ?).
5. Include TP1 VEC requirement.
   - Value to be agreed.
6. Allow "Coarse" host TX pre-cursor tap for long channels only (off for short ones) – this would be a fixed and "static" value.
   - Value and loss range to be eventually defined.
   - Symmetrically the same tap should be needed on module's transmitter too so should be writable by the host into the module.

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My personal conclusions (C2M)

- The agreed C2M baseline does not provide adequate margin on all the submitted channels. Our options are to:
  - Change the channel requirements (ILM)
  - Change the margin requirement (COM/Eye Height)
  - Change the PHY requirements (Rx Eq complexity, Tx eq)
  - A combination of the above

- We need change proposals at the interim
  - ILM, Eye Height, 3p2z CTLE, LF CTLE, Tx EQ, etc.

Backup

Participants, Patents, and Duty to Inform

All participants in this meeting have certain obligations under the IEEE-SA Patent Policy.

- **Participants [Note: Quoted text excerpted from IEEE-SA Standards Board Bylaws subclause 6.2]:**
  - **"Shall inform the IEEE (or cause the IEEE to be informed)" of the identity of each "holder of any potential Essential Patent Claims of which they are personally aware" if the claims are owned or controlled by the participant or the entity the participant is from, employed by, or otherwise represents**
  - **"Should inform the IEEE (or cause the IEEE to be informed)" of the identity of "any other holders of potential Essential Patent Claims" (that is, third parties that are not affiliated with the participant, with the participant's employer, or with anyone else that the participant is from or otherwise represents)**
- **The above does not apply if the patent claim is already the subject of an Accepted Letter of Assurance that applies to the proposed standard(s) under consideration by this group**
- **Early identification of holders of potential Essential Patent Claims is strongly encouraged**
- **No duty to perform a patent search**

Patent Related Links

All participants should be familiar with their obligations under the IEEE-SA Policies & Procedures for standards development.

Patent Policy is stated in these sources:

IEEE-SA Standards Boards Bylaws

http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#6

IEEE-SA Standards Board Operations Manual

http://standards.ieee.org/develop/policies/opman/sect6.html#6.3

Material about the patent policy is available at

http://standards.ieee.org/about/sasb/patcom/materials.html

If you have questions, contact the IEEE-SA Standards Board Patent Committee Administrator at patcom@ieee.org or visit http://standards.ieee.org/about/sasb/patcom/index.html

This slide set is available at https://development.standards.ieee.org/myproject/Public/mytools/mob/slideset.ppt

Call for Potentially Essential Patents

- If anyone in this meeting is personally aware of the holder of any patent claims that are potentially essential to implementation of the proposed standard(s) under consideration by this group and that are not already the subject of an Accepted Letter of Assurance:
  - Either speak up now or
  - Provide the chair of this group with the identity of the holder(s) of any and all such claims as soon as possible or
  - Cause an LOA to be submitted