50G PAM4 C2M ADS and COM Eye Simulation Comparison

Mike Dudek Cavium
Tao Hu Cavium
3/6/2017

Introduction

- This presentation explores the difference between ADS simulation and COM on an excellent chip to module link with and without crosstalk.
- The loss of the long package and host PCB traces used in COM are concatenated with a measured mated test fixture file which includes crosstalk. No other degradations in the Tx and package and PCB traces are included.
- All ADS simulation eye height and eye width measurements are from the ADS measurement methodology not the method adopted in the 802.3bs draft.
- A separate presentation will be made to investigate the effects of the other degradations.

Methodology

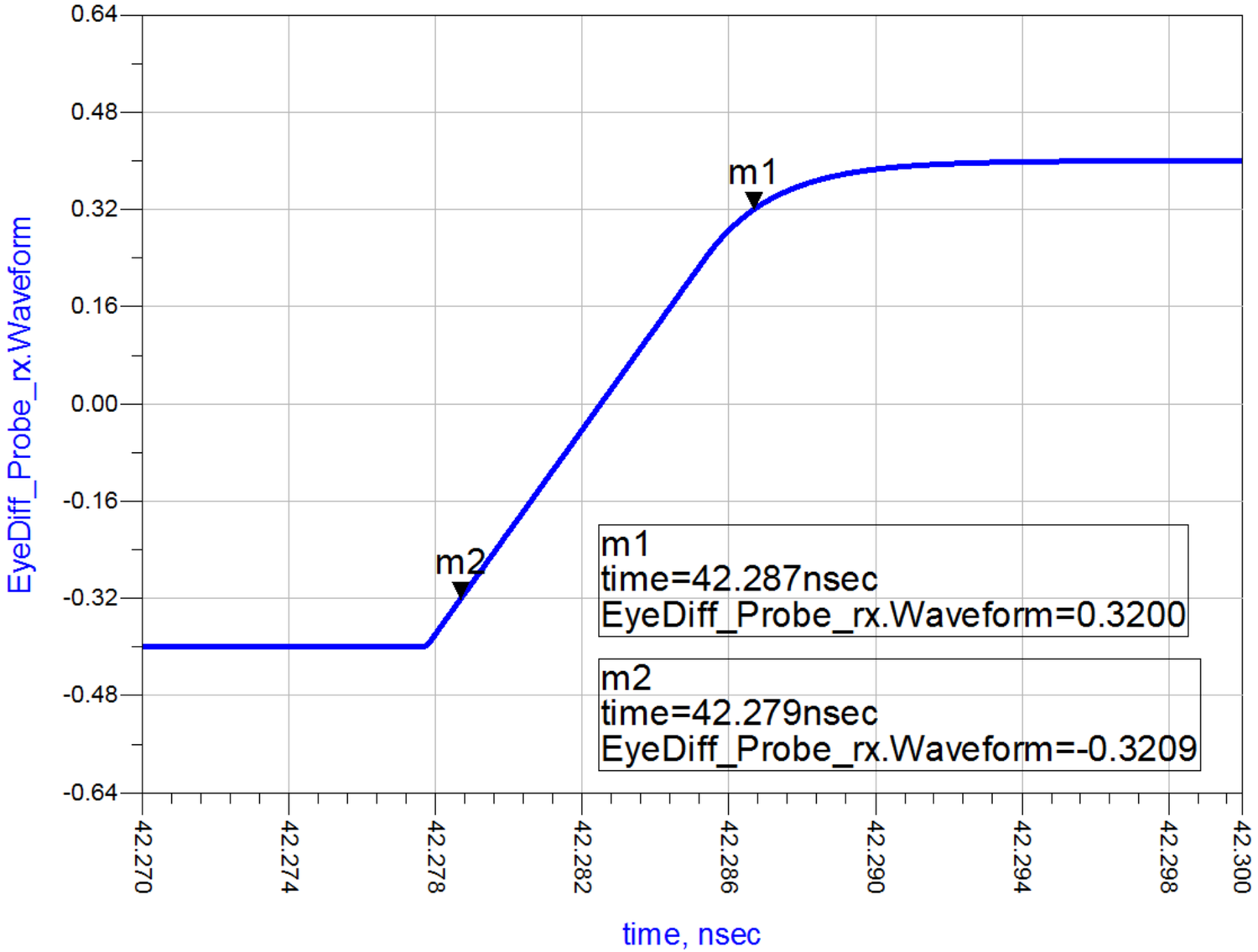
- **Characterize ADS PAM4 driver to match the Tx used in COM**
  - 0.8V voltage swing
  - 8pS 20-80% risetime
- **In ADS, sweep TX FIR and CTLE to find optimal eye at BER 1E-5**

  pre1: -0.15 to 0 with step 0.05

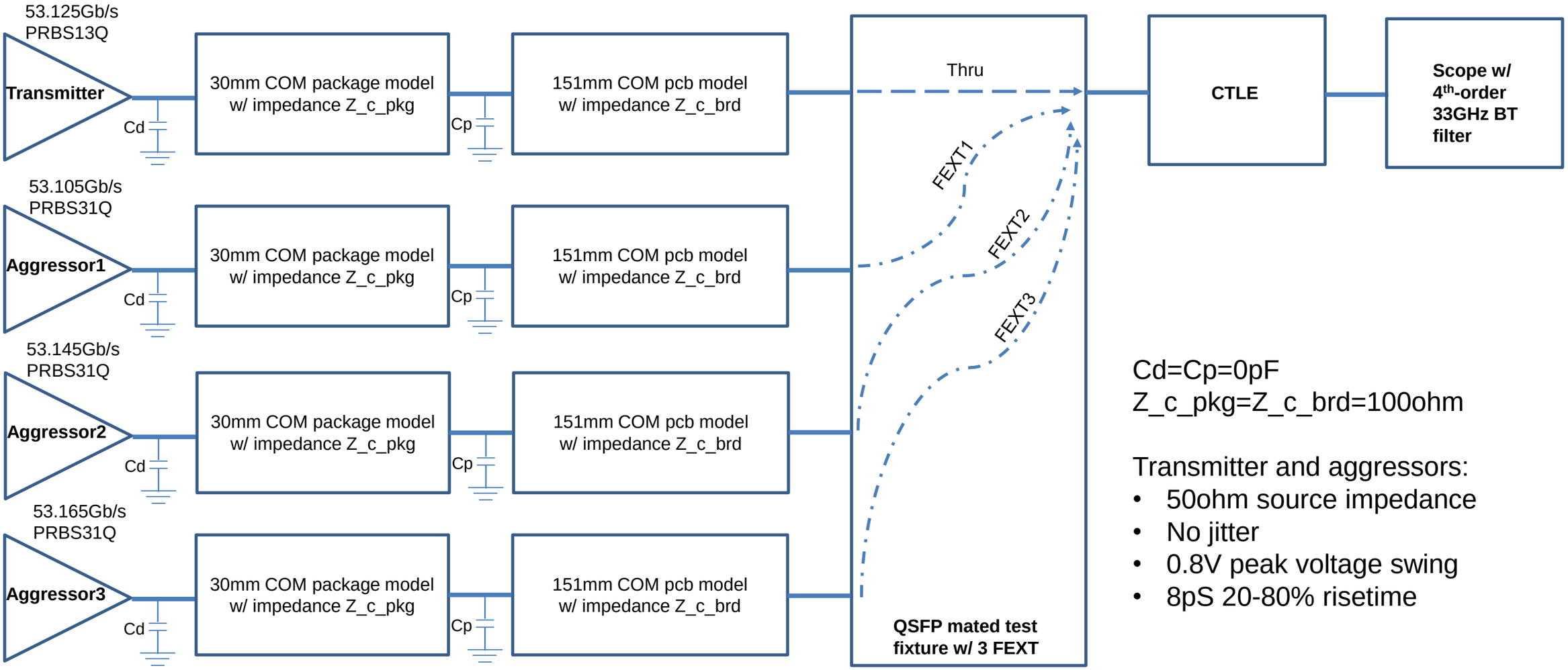
  pre2: 0 to 0.1 with step 0.025

  post1: -0.25 to 0 with step 0.05
- **Run simulation in COM to get eye height at BER 1E-5**

ADS PAM4 driver: 0.8V voltage swing and 8pS risetime 20-80%



Chip to module block diagram

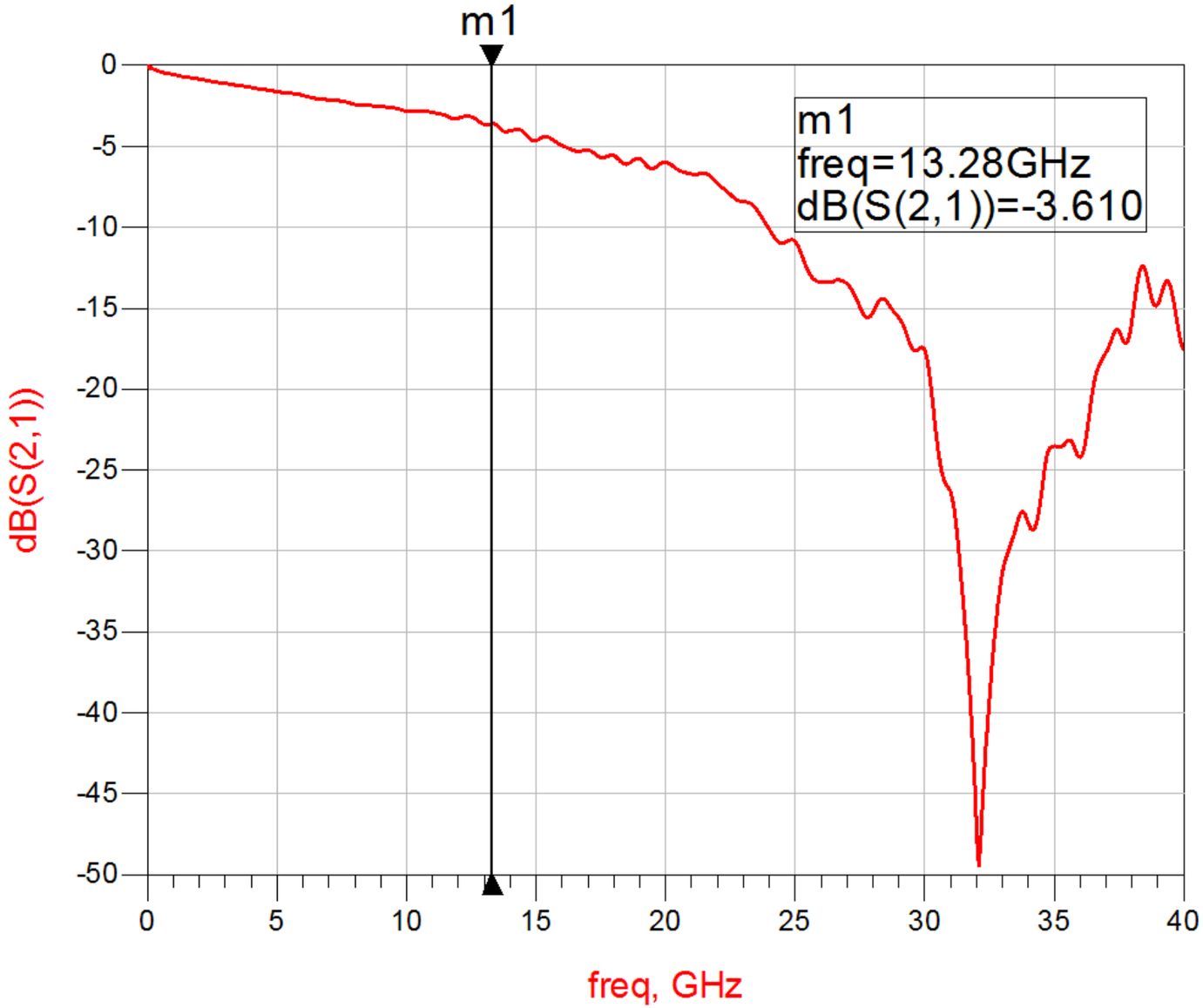


Cd=Cp=0pF
Z_c_pkg=Z_c_brd=100ohm

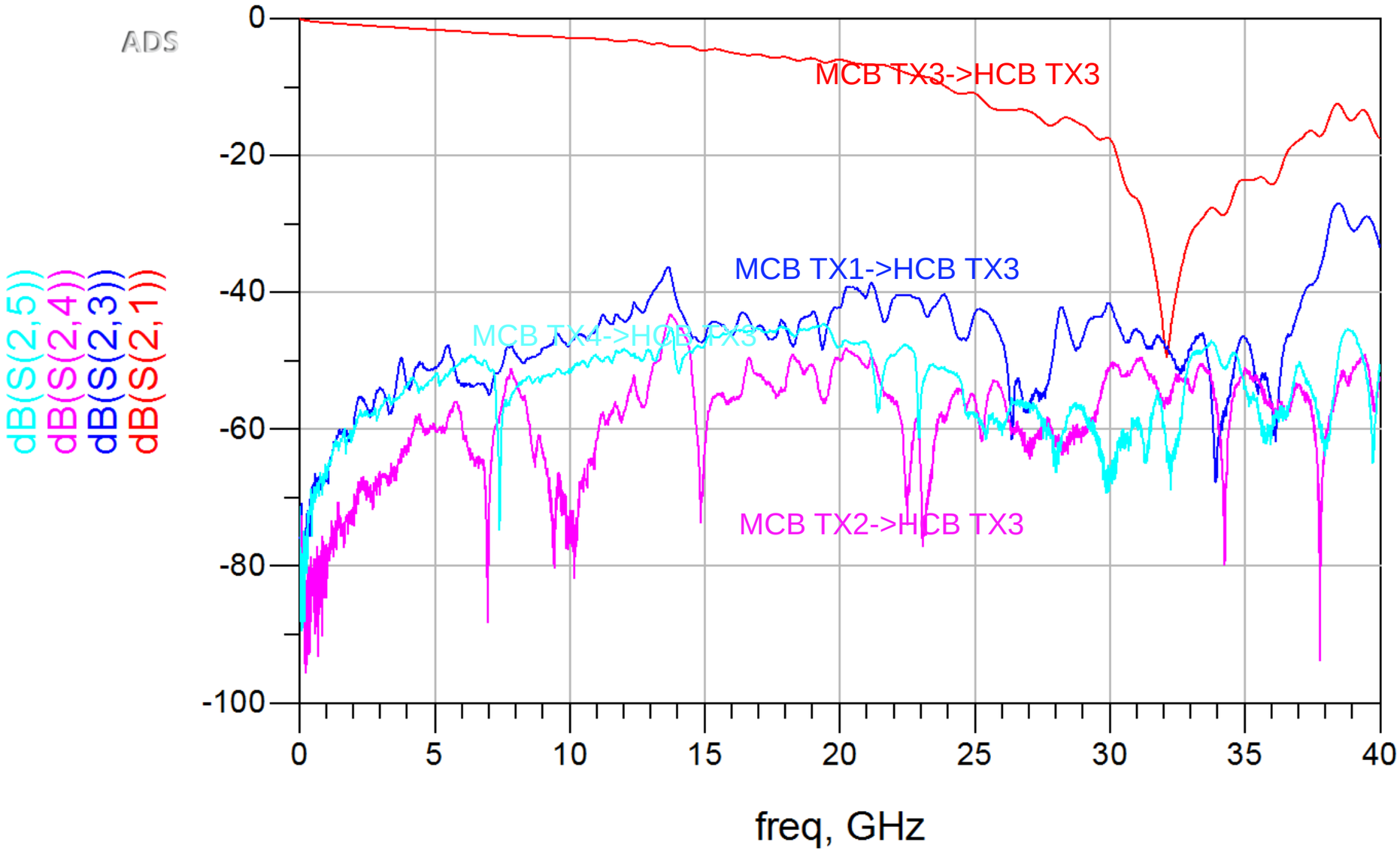
Transmitter and aggressors:

- 50ohm source impedance
- No jitter
- 0.8V peak voltage swing
- 8pS 20-80% risetime

Mated QSFP test fixture insertion loss

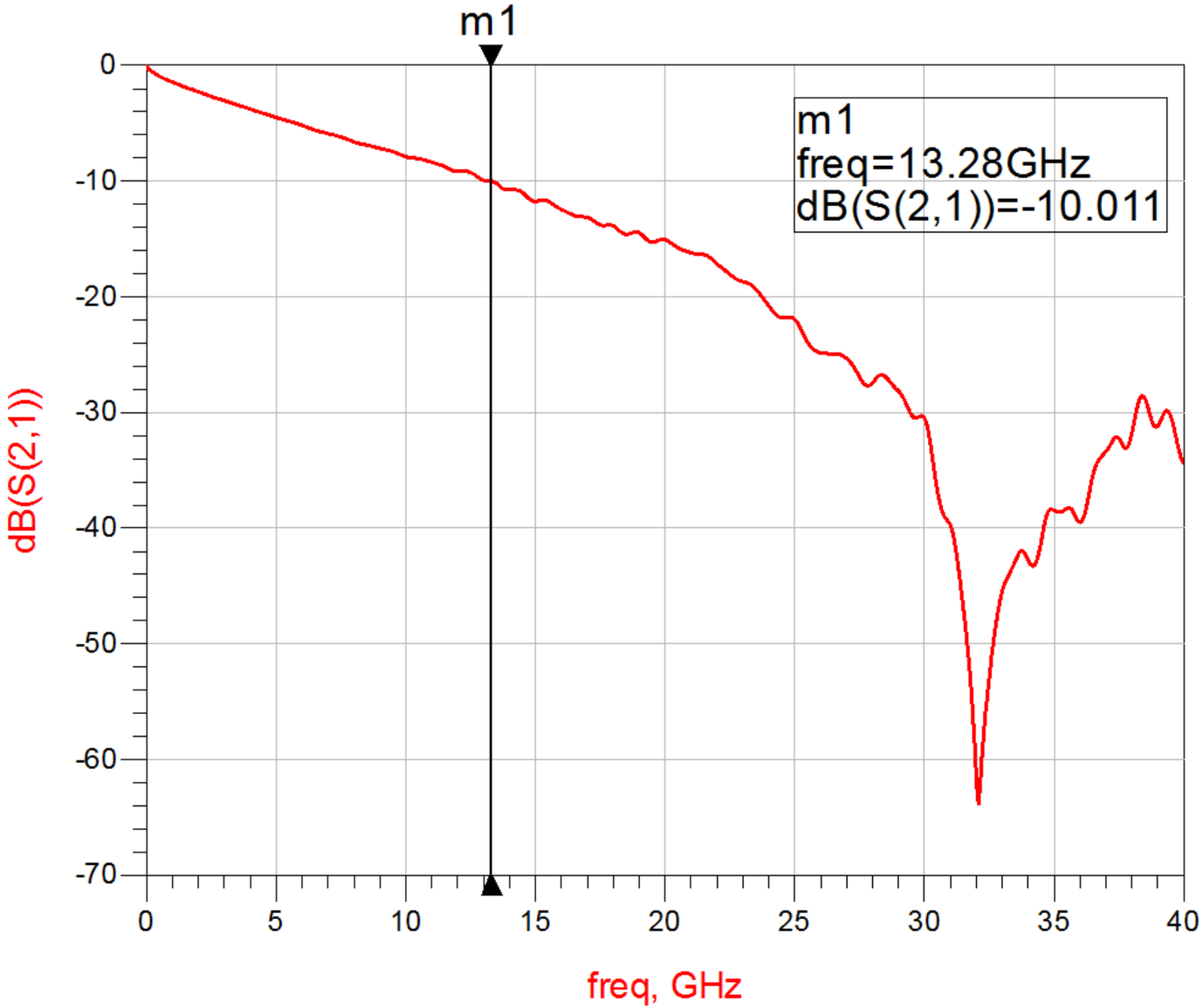


QSFP mated test fixtures THRU and FEXT

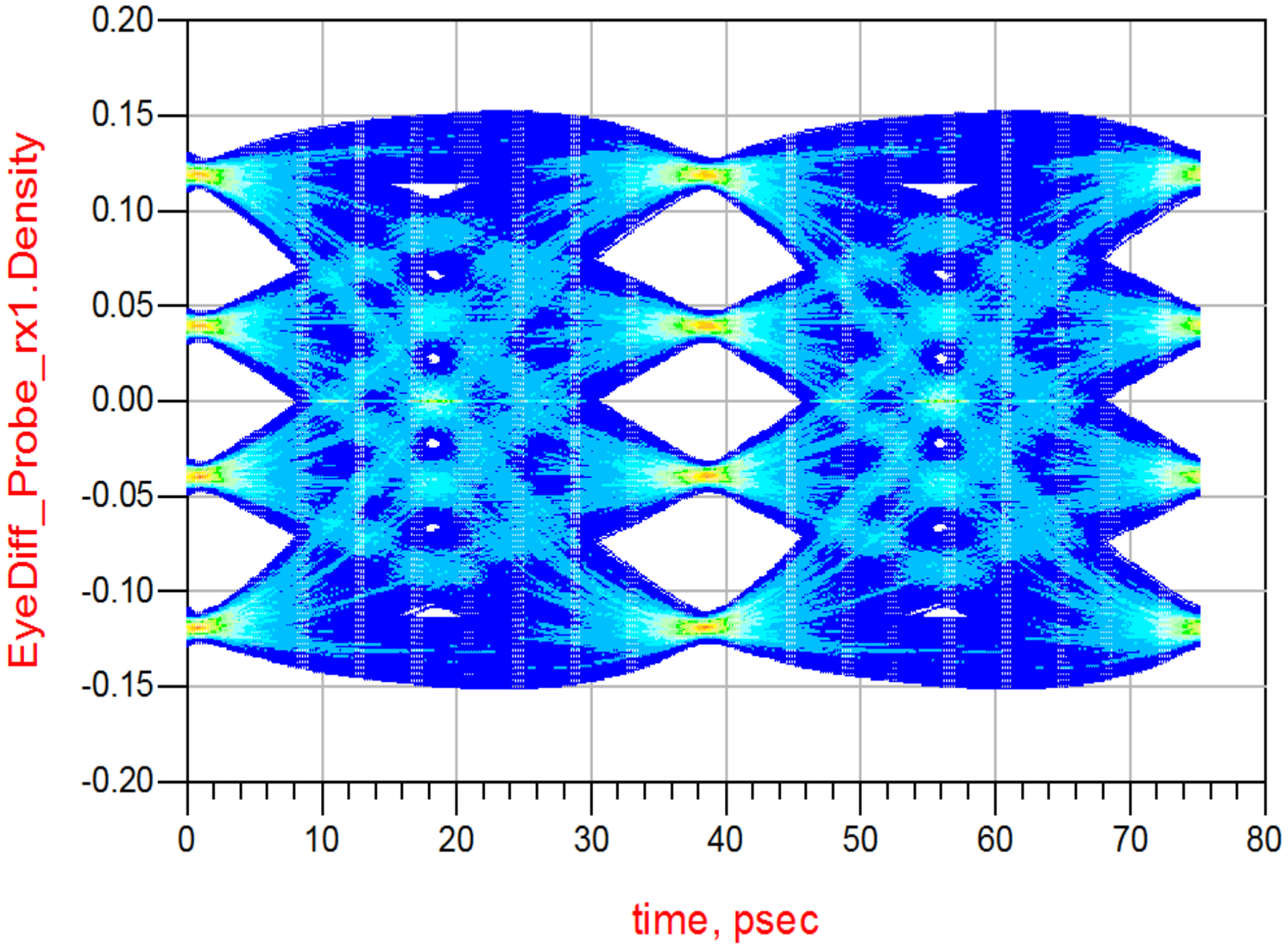


FEXT measured per procedure for mated test boards =2.7mV rms.

151mm 100ohm PCB plus mated QSFP test fixture insertion loss



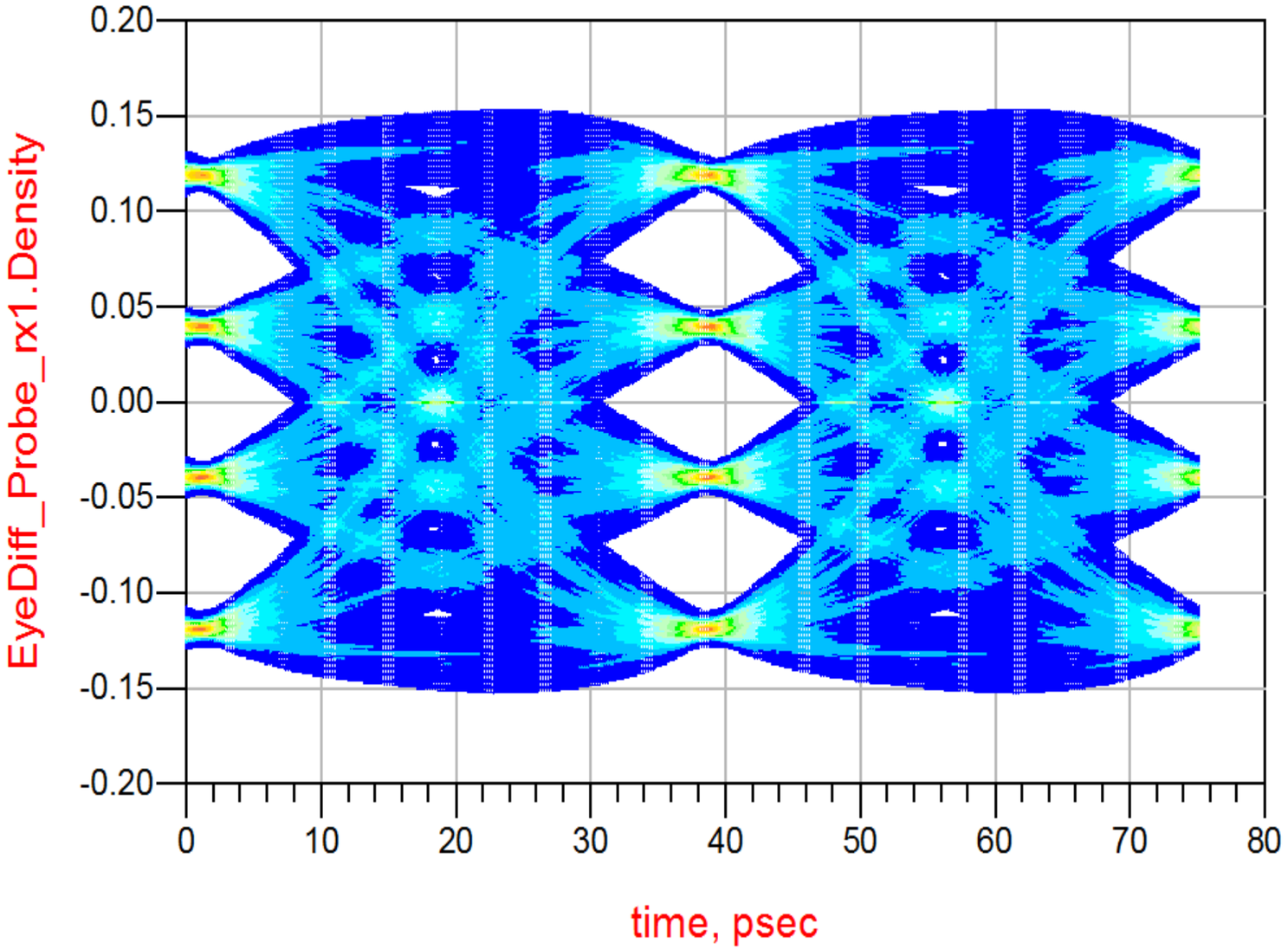
ADS BER 1E-5 eye @ HCB w/o xtalk



measurement	...robe_rx1.Summary batchNumber=1
WidthAtBER0	1.506E-11
WidthAtBER1	1.506E-11
WidthAtBER2	1.544E-11
HeightAtBER0	0.064
HeightAtBER1	0.063
HeightAtBER2	0.065

Optimal settings:
FIR: -0.1 0.85 -0.05
CTLE: 6.5dB

ADS BER 1E-5 eye @ HCB w/ xtalk



measurement	...robe_rx1.Summary batchNumber=1
WidthAtBER0	1.468E-11
WidthAtBER1	1.468E-11
WidthAtBER2	1.506E-11
HeightAtBER0	0.062
HeightAtBER1	0.061
HeightAtBER2	0.063

Optimal settings:
FIR: -0.1 0.85 -0.05
CTLE: 6.5dB

COM simulation

COM configurations

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	26.5625	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[30]	mm	[test cases]
z_p (NEXT)	[12]	mm	[test cases]
z_p (FEXT)	[30]	mm	[test cases]
z_p (RX)	[0 0]	mm	[test cases]
C_p	[0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.15:0.05:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		
c(1)	[-0.25:0.05:0]		[min:step:max]
g_DC	.5 3 3.5 4 4.5 5 5.5 6 6.5 7 7	dB	[min:step:max]
f_z	6.155 5.733 5.353 5.007 4.	GHz	
f_p1	6 15.6 15.6 15.6 15.6 15.6 1	GHz	
f_p2	1 14.1 14.1 14.1 14.1 14.1 1	GHz	
A_v	0.4	V	
A_fe	0.4	V	
A_ne	0.4	V	
L	4		
M	32		
N_b	0	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
sigma_RJ	0	UI	
A_DD	0	UI	
eta_0	0.00E+00	V^2/GHz	
SNR_TX	100	dB	
R_LM	1		
DER_0	1.00E-05		
Operational control	1		
COM Pass threshold	3	dB	
Include PCB	1	Value	0, 1
PHY_type	C2M		
EH_min	32	Value	EH limit
EH_max	34	Value	EH limit
f_HP_P	1.2 1.2 1.2 1.2 1.2 1.2 1.2	GHz	
f_HP_Z	1 1.075 1.05 1.025 1 1 1 1	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
Display frequency domain	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\C2C_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	c2m_MTF	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	8.00E-03	ns
FORCE_TR	1	logical

Non standard control options		
INC_PACKAGE	1	logical
IDEAL_RX_TERM	0	logical
INCLUDE_CTLE	1	logical
INCLUDE_TX_RX_FILTER	1	logical
COM_CONTRIBUTION	0	logical

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	100	Ohm

Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	151	mm
z_bp (RX)	0	mm

COM results

QLOGIC
a Cavium company

```
          code_revision: '1.65'
            config_file: 'eq_qsfp_mtf.xls'
             file_names: '"c2m_MTF --A_MCB_P1P3_TX3_tcard_P2P4_TX3"'
                 levels: 4
              Pkg_len_TX: 30
            Pkg_len_NEXT: 12
            Pkg_len_FEXT: 30
              Pkg_len_RX: 0
           baud_rate_GHz: 26.5625
           f_Nyquist_GHz: 13.2813
channel_operating_margin_dB: 16.2892
       peak_interference_mV: 5.7500
peak_channel_interference_mV: 5.7500
            peak_ISI_mV: 5.7500
      peak_uneq_pulse_mV: 186.8247
  peak_MDXTK_interference_mV: 0
 peak_MDNEXT_interference_mV: 0
 peak_MDFEXT_interference_mV: 0
available_signal_after_eq_mV: 37.5083
     steady_state_voltage_mV: 119.4958
                  VEO_mV: 63.5166
         VEO_normalized: 0.8467
                  VEC_dB: 1.4454
    fit_loss_dB_at_Fnq: 10.1973
           cable_loss: 3.6102
         IL_dB_at_Fnq: 10.0175
              FOM_ILD: 0.0767
               ICN_mV: 0
    equivalent_ISI_ICN: 0
      sci_noise_FD_RMS: 0.2752
       CTLE_zero_poles: [9.2459e+09 1.0000e+09 1.4100e+10 1.5600e+10 1.2000e+09]
       CTLE_DC_gain_dB: -7
             TXLE_taps: [0.0250 -0.1500 0.8250 0 0 0]
              DFE_taps: [0×1 double]
      cci_noise_TD_BER: 0
peak_interference_at_BER: 0.0058
                  FOM: 28.4608
              DFE4_RSS: 0
              DFE2_RSS: 0
```

No xtalk

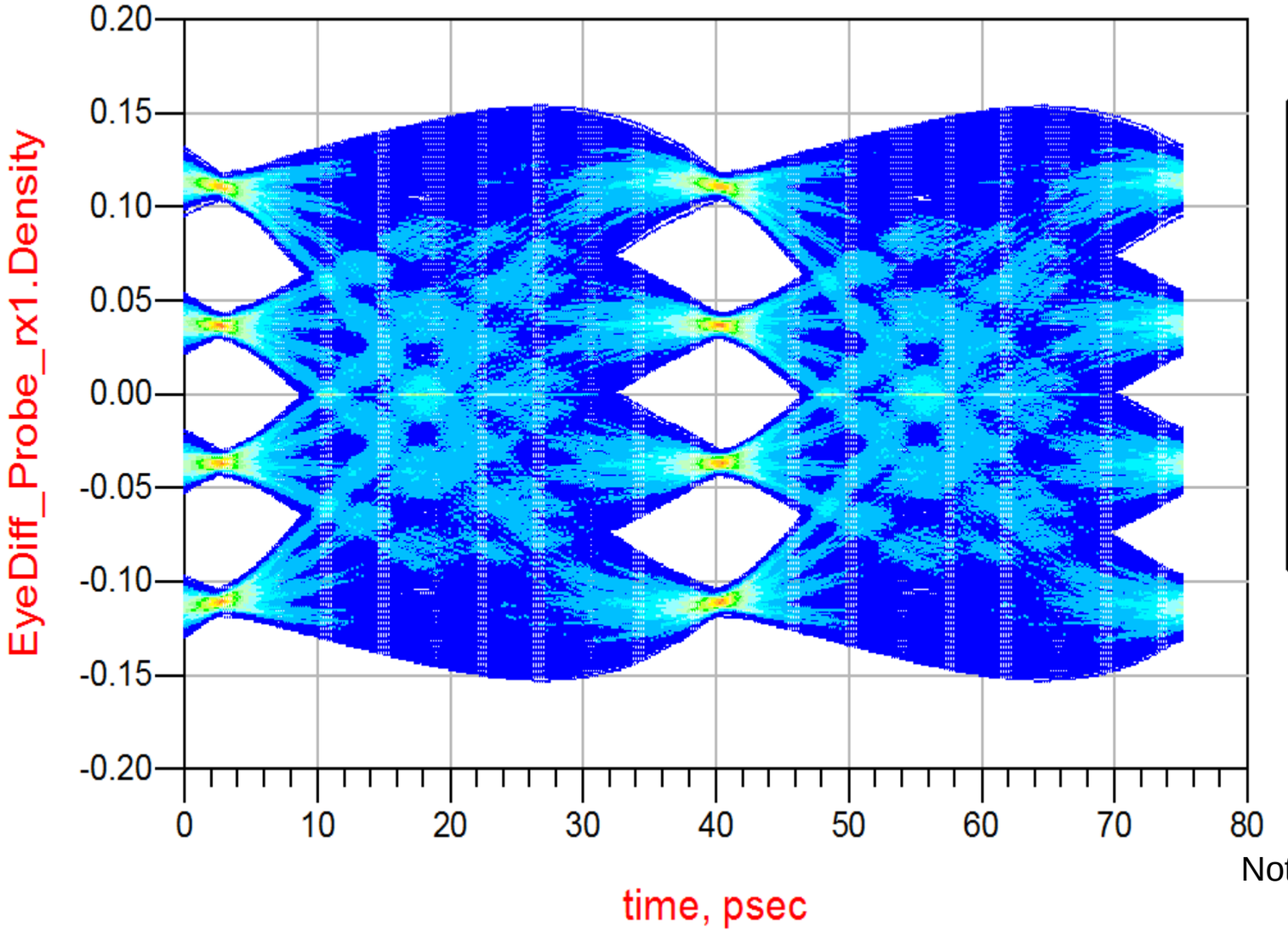
```
com_ieee8023_93a_165('eq_qsfp_mtf.xls', 0, 0,
'A_MCB_P1P3_TX3_tcard_P2P4_TX3.s4p')
```

```
          code_revision: '1.65'
            config_file: 'eq_qsfp_mtf.xls'
             file_names: '"c2m_MTF --A_MCB_P1P3_TX3_tcard_P2P4_TX3,c2m_MTF --MCB_P1P3_TX1_HCB_P2…'
                 levels: 4
              Pkg_len_TX: 30
            Pkg_len_NEXT: 12
            Pkg_len_FEXT: 30
              Pkg_len_RX: 0
           baud_rate_GHz: 26.5625
           f_Nyquist_GHz: 13.2813
channel_operating_margin_dB: 15.3998
       peak_interference_mV: 6.3700
peak_channel_interference_mV: 6.3700
            peak_ISI_mV: 5.7500
      peak_uneq_pulse_mV: 0.4183
  peak_MDXTK_interference_mV: 2.3000
 peak_MDNEXT_interference_mV: 0
 peak_MDFEXT_interference_mV: 2.3000
available_signal_after_eq_mV: 37.5083
     steady_state_voltage_mV: 119.4958
                  VEO_mV: 62.2766
         VEO_normalized: 0.8302
                  VEC_dB: 1.6167
    fit_loss_dB_at_Fnq: 10.1973
           cable_loss: 3.6102
         IL_dB_at_Fnq: 10.0175
              FOM_ILD: 0.0767
               ICN_mV: 1.3132
    equivalent_ISI_ICN: 4.4069e-04
      sci_noise_FD_RMS: 0.2752
       CTLE_zero_poles: [9.2459e+09 1.0000e+09 1.4100e+10 1.5600e+10 1.2000e+09]
       CTLE_DC_gain_dB: -7
             TXLE_taps: [0.0250 -0.1500 0.8250 0 0 0]
              DFE_taps: [0×1 double]
      cci_noise_TD_BER: 0.0023
peak_interference_at_BER: 0.0064
                  FOM: 27.6682
              DFE4_RSS: 0
              DFE2_RSS: 0
```

With xtalk

```
com_ieee8023_93a_165('eq_qsfp_mtf.xls', 3, 0,
'A_MCB_P1P3_TX3_tcard_P2P4_TX3.s4p',
'MCB_P1P3_TX1_HCB_P2P4_TX3_term_changed.s4p',
'MCB_P1P3_TX2_HCB_P2P4_TX3_term_changed.s4p',
'MCB_P1P3_TX4_HCB_P2P4_TX3_term_changed.s4p')
```

ADS BER 1E-5 Eye @ HCB w/o xtalk using COM optimized settings

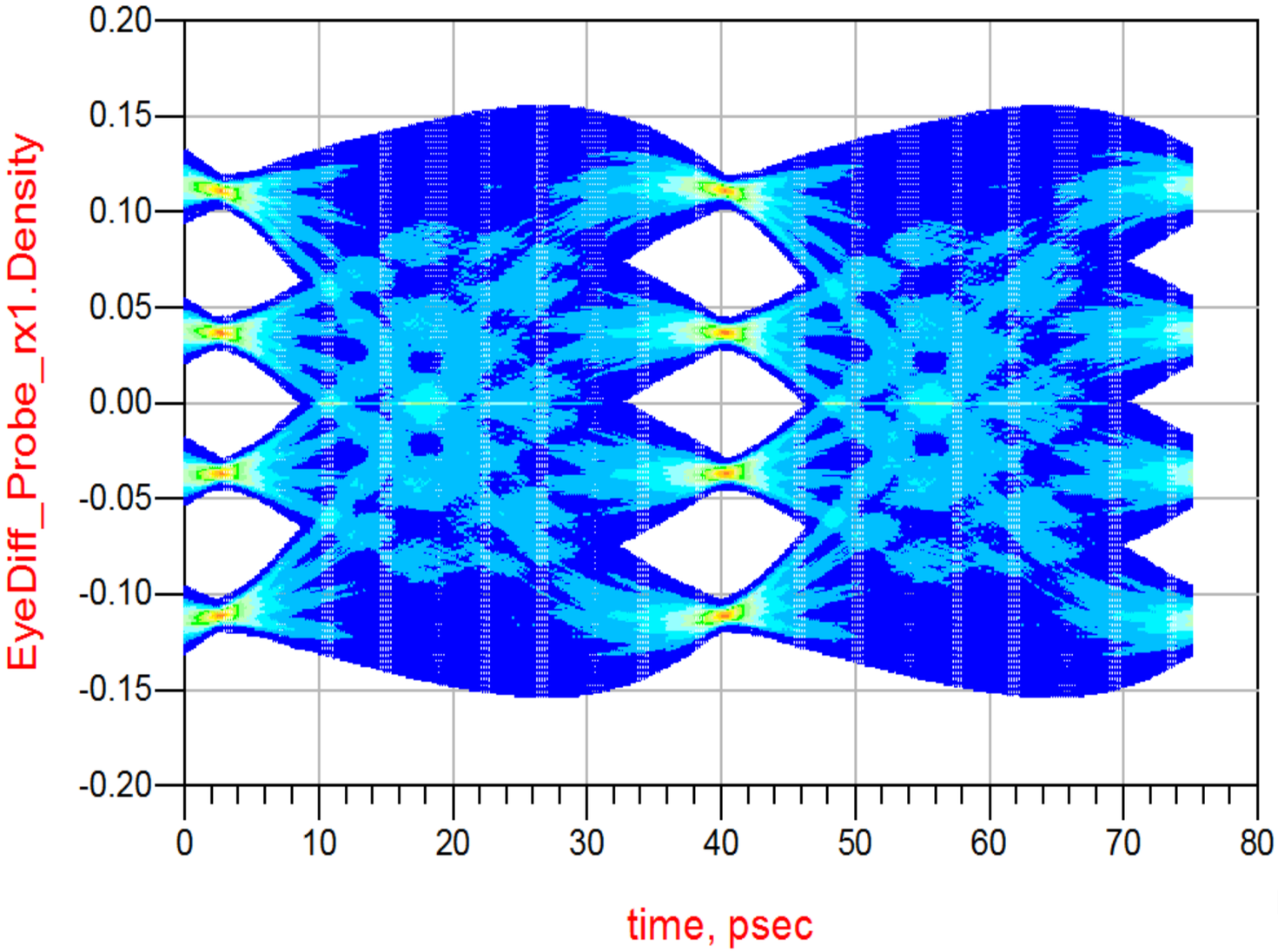


measurement	...robe_rx1.Summary batchNumber=1
WidthAtBER0	1.431E-11
WidthAtBER1	1.374E-11
WidthAtBER2	1.412E-11
HeightAtBER0	0.061
HeightAtBER1	0.060
HeightAtBER2	0.061

COM settings:
FIR: 0.025 -0.15 0.825 0 0
CTLE: 7dB

Note VEO from COM was 63.5mV

ADS BER 1E-5 Eye @ HCB w/ xtalk using COM optimized settings



measurement	...robe_rx1.Summary batchNumber=1
WidthAtBER0	1.393E-11
WidthAtBER1	1.355E-11
WidthAtBER2	1.374E-11
HeightAtBER0	0.058
HeightAtBER1	0.057
HeightAtBER2	0.058

COM settings:
FIR: 0.025 -0.15 0.825 0 0
CTLE: 7dB

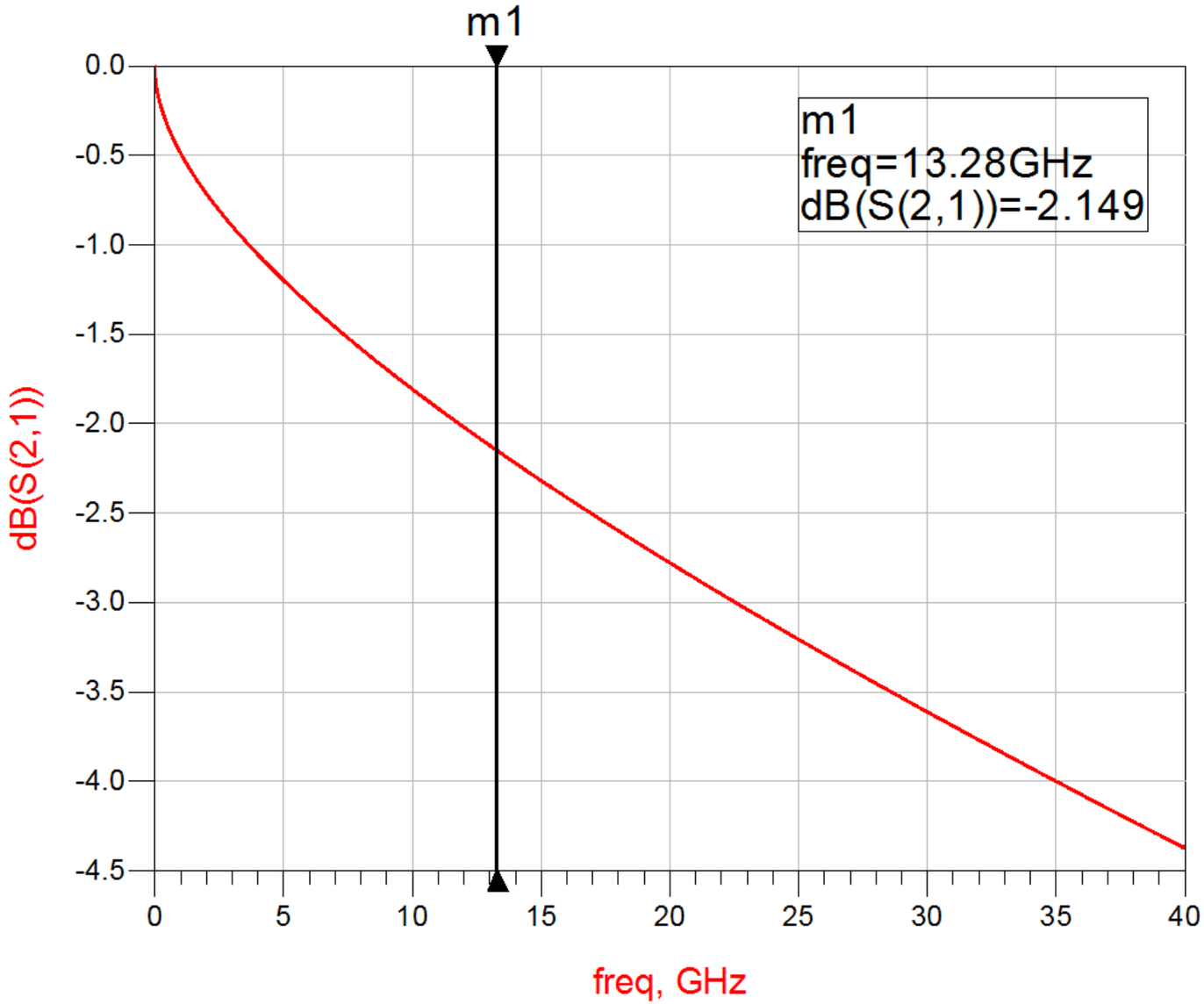
Note VEO from COM was 62.3mV

Conclusions

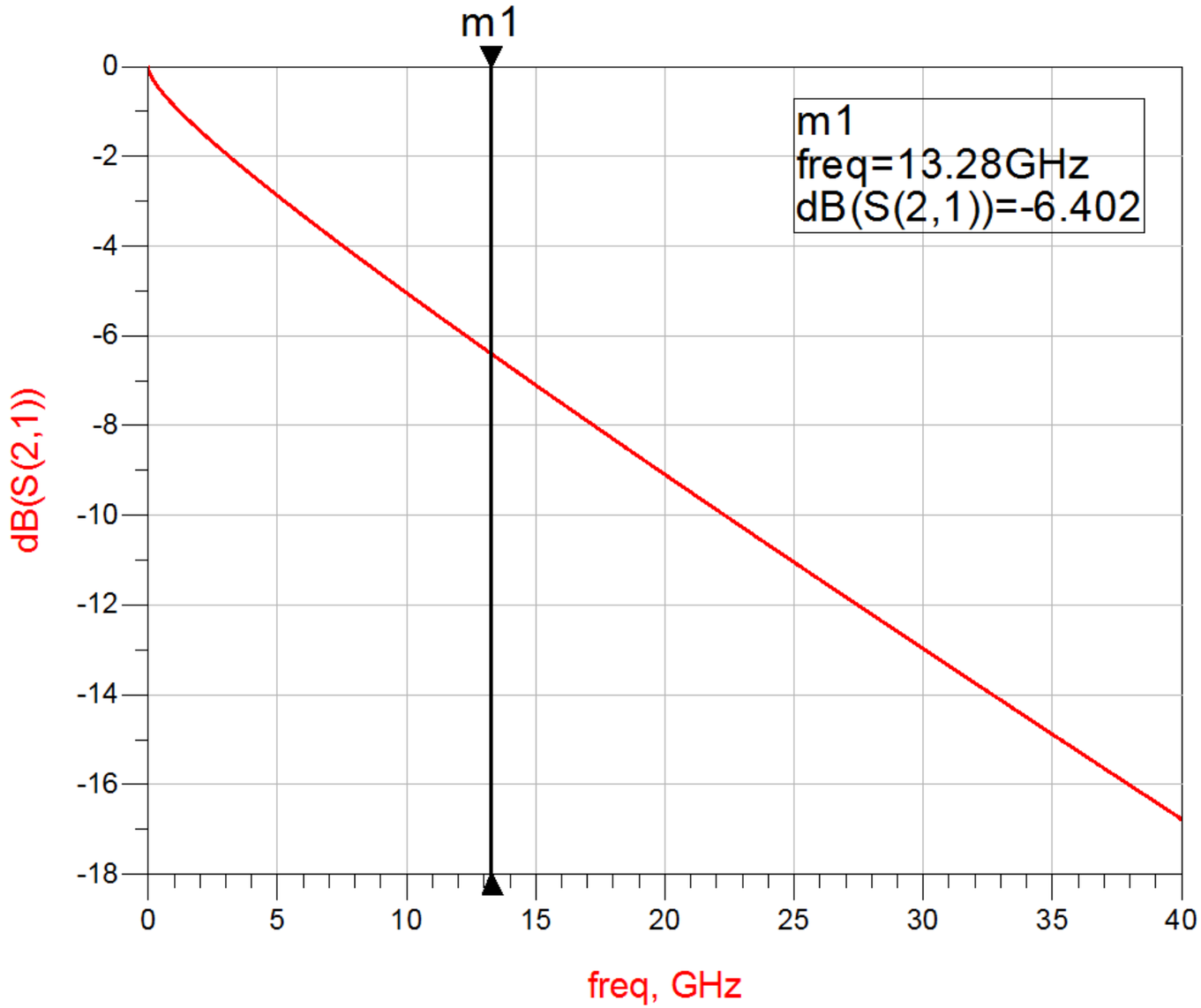
- The adaptation in COM does not find the optimum settings for eye height and eye width.
- ADS simulation gives a significantly smaller eye height than COM VEO for the same settings.
- The ADS eye height and COM VEO are similar for this test condition but that is because optimism in the simulation appears to be compensating for not finding the optimum settings.
- With an unrealistically good host and IC package the 32mV eye amplitude is easily achieved with a 10dB channel
- There is a small degradation in eye height with test board FEXT of 2.7mV .

Backup.

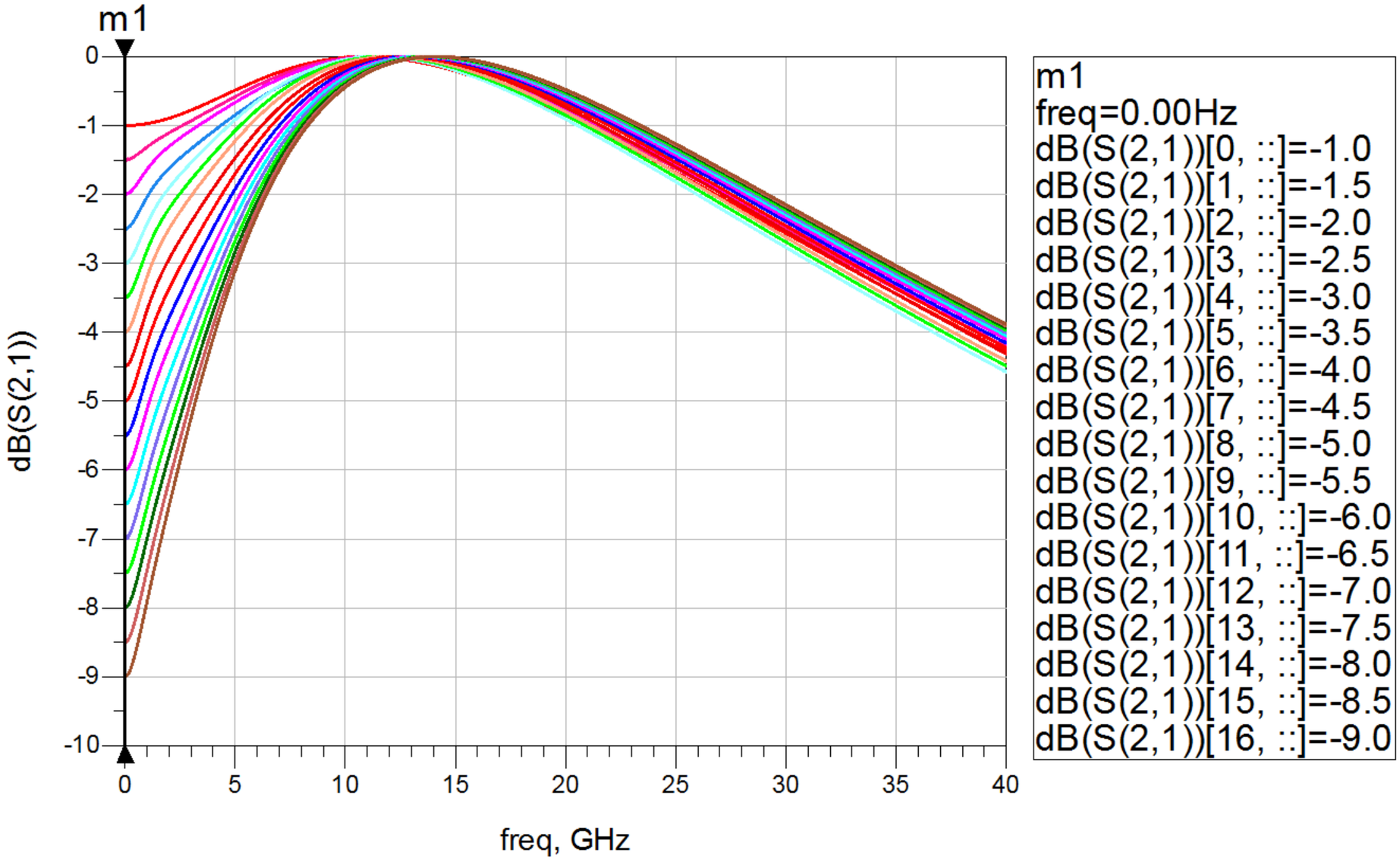
30mm 100ohm COM package insertion loss



151mm 100ohm COM PCB insertion loss



CTLE curves


m1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
dB(S(2,1))
0
5
10
15
20
25
30
35
40
freq, GHz
m1
freq=0.00Hz
dB(S(2,1))[0, ::]=-1.0
dB(S(2,1))[1, ::]=-1.5
dB(S(2,1))[2, ::]=-2.0
dB(S(2,1))[3, ::]=-2.5
dB(S(2,1))[4, ::]=-3.0
dB(S(2,1))[5, ::]=-3.5
dB(S(2,1))[6, ::]=-4.0
dB(S(2,1))[7, ::]=-4.5
dB(S(2,1))[8, ::]=-5.0
dB(S(2,1))[9, ::]=-5.5
dB(S(2,1))[10, ::]=-6.0
dB(S(2,1))[11, ::]=-6.5
dB(S(2,1))[12, ::]=-7.0
dB(S(2,1))[13, ::]=-7.5
dB(S(2,1))[14, ::]=-8.0
dB(S(2,1))[15, ::]=-8.5
dB(S(2,1))[16, ::]=-9.0