






Architecture and Electrical Interfaces

IEEE P802.3bs 400GbE Task Force
Electrical Interface Ad Hoc

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IEEE 802.3 Sept 2014 Interim

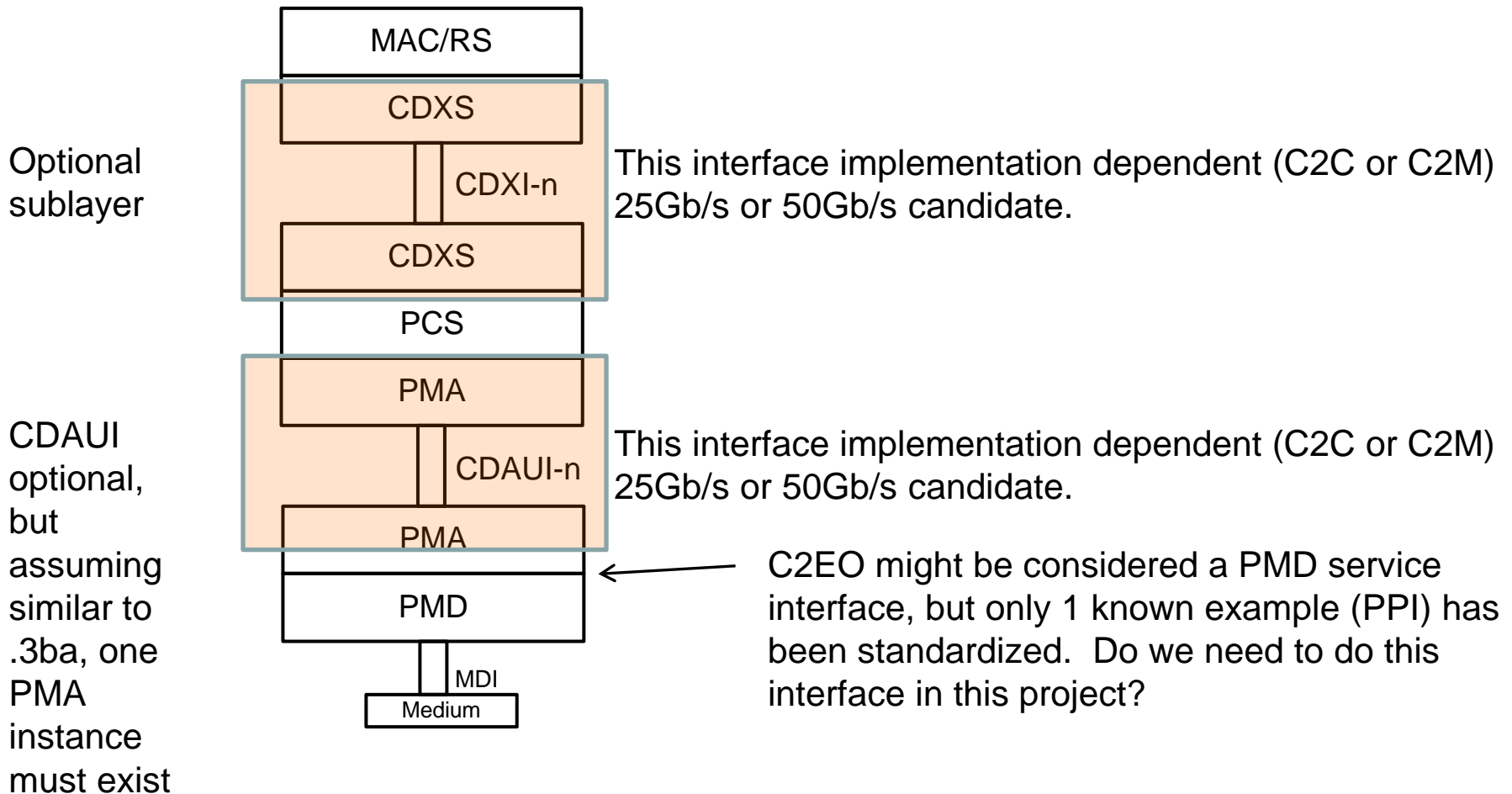
From goergen_3bs_01_0914

	< 10mm/0.4in	USR	1.5dB@14GHz 3dB@28GHz	Bump-to-bump Inside MCM or 3D Stack
	< 50mm/2.0in	XSR C2EO	4dB@14GHz 8dB@28GHz	Ball-to-ball Across PCB
	< 200mm/7.9in	VSR C2M	10dB@14GHz 20dB@28GHz	Ball-to-ball
	< 500mm/19.7in	MR C2C	20dB@14GHz 40dB@28GHz	Ball-to-ball
	< 1000mm/39.4in	LR C2F	35dB@14GHz	Ball-to-ball

Questions We Need to Ask?

- Where do these interfaces exist in the stack?
 - C2EO
 - C2M
 - C2C

Architecture Consideration



Proposal Consideration

- Will either interface require FEC?
 - FEC needs to be considered as part of a CDXS proposal
 - FEC would need to be considered into the proposal of CDAUI
- EEE?

Thank You!