Very Short Reach/Chip-to-Module Channels

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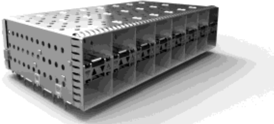


TE connectivity

Purpose

- This is an update to the channels submitted to the task force in June 2014 [shanbhag_3bs_14_0623.pdf]
- These are VSR channel models with an SMT and a Stacked press-fit connectors.
- The channels have been modified to reflect trace loss using Megtron6 material for a typical trace geometry using a 4” host and a 10” host for each connector type.
- Channel models:
  - “Next generation 28Gb/s high density SMT IO, 4 inch host” → [shanbhag_02_1014.zip]
  - “Next generation 28Gb/s high density SMT IO, 10 inch host” → [shanbhag_03_1014.zip]
  - “Next generation 28Gb/s press-fit stacked IO, 4 inch host” → [shanbhag_04_1014.zip]
  - “Next generation 28Gb/s press-fit stacked IO, 10 inch host” → [shanbhag_05_1014.zip]
- These channels include module connector *concepts* that are being evaluated for 28Gb/s applications. These are NOT existing connectors and they have been designed for *28Gb/s* applications, however they are being contributed for this analysis due their favorable performance.
- This is a good time for feedback.

Connector Concepts

- “Next generation 28Gb/s high density SMT IO” is a connector *concept* that achieves density by placing contacts on a pitch less than 0.6mm
  - The connector interfaces to the host PCB via surface mount attachment
- “Next generation 28Gb/s press-fit stacked IO” is a connector *concept* that has contact density at 0.6mm
  - The connector is a “stacked” dual port solution and interfaces to the host PCB via press-fit attachment methodology
- Both connector concepts use PCB card edge interfaces as the mating interface

TE connectivity

Channel Details
Next Generation 28Gbps High Density SMT IO

Host PCB

- 2.86mm thick, 23 Layers(12 GND planes)
- 2 Layer route out (Layer 10,12)
- 8mil stub on signal vias
- Stripline trace loss added to model
  - 4” 5-6-5 mils Megtron 6 (Loss Tangent=0.007), [shanbhag_02_1014.zip]
  - 10” 5-6-5 mils Megtron 6 (Loss Tangent=0.007), [shanbhag_03_1014.zip]

Module PCB details

- 1mm thick, 6 layer PCB (4 GND Planes)
- Microstrip trace route-out from 0.35x1.4mm mating pads
- Microstrip trace loss added to model
  - 1.25” 7-5-7 mils Megtron 6 (Loss Tangent=0.007)

TE connectivity

Channel Details

Next Generation 28Gbps Pressfit Stacked IO

Host PCB

- 3.425mm thick, 26 Layers(15 GND planes)
- 4 Layer route out (Layer 7, 11, 17, 21)
- 8mil stub on signal vias
- Stripline trace loss added to model
    - 4” 5-6-5 mils Megtron 6 (Loss Tangent=0.007), [shanbhag_04_1014.zip]
    - 10” 5-6-5 mils Megtron 6 (Loss Tangent=0.007), [shanbhag_05_1014.zip]

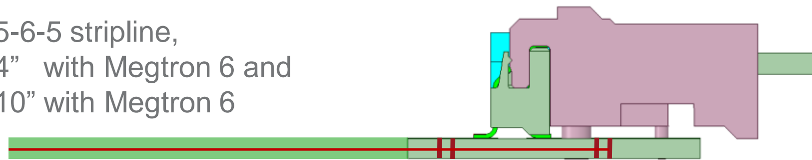
Module PCB details

- 1mm thick, 6 layer PCB (4 GND Planes)
- Microstrip trace route-out from 0.35x1.4mm mating pads
- Microstrip trace loss added to model
    - 1.25” 7-5-7 mils Megtron 6 (Loss Tangent=0.007)

Visual Representation

"Next generation 28Gb/s high density SMT IO":

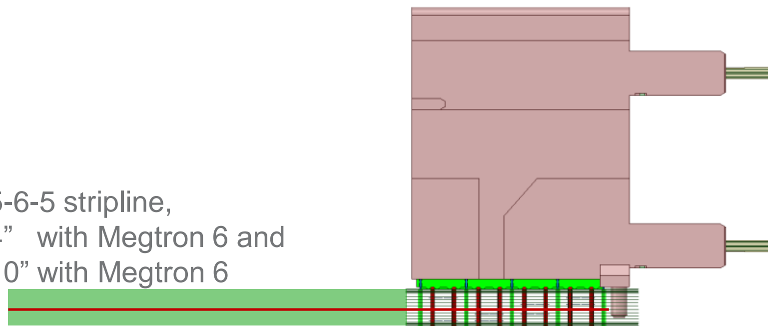
5-6-5 stripline,
4" with Megtron 6 and
10" with Megtron 6



7-5-7 microstrip,
1.25" with Megtron 6

"Next generation 28Gb/s press fit stacked IO":

5-6-5 stripline,
4" with Megtron 6 and
10" with Megtron 6

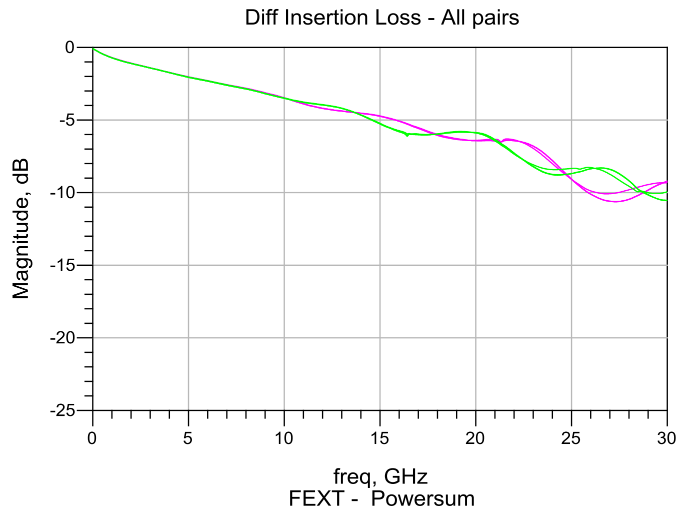


7-5-7 microstrip,
1.25" with Megtron 6

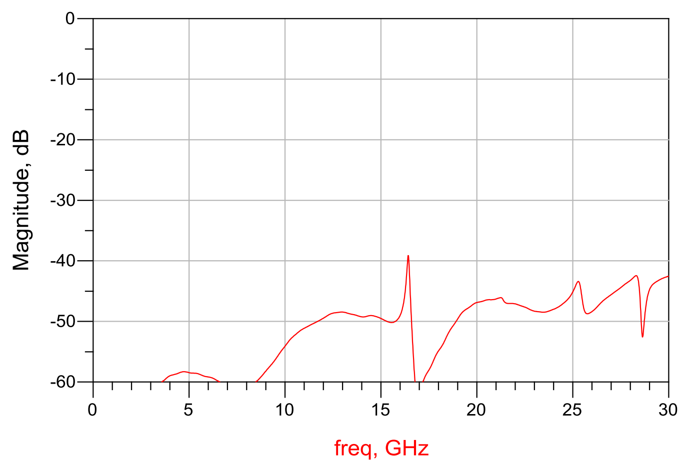
7-5-7 microstrip,
1.25" with Megtron 6

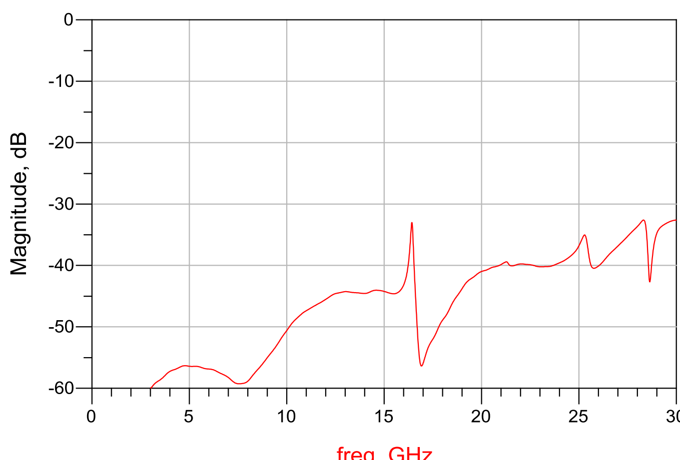
Channel Performance

Next Generation 28Gbps High Density SMT IO with 4” Host

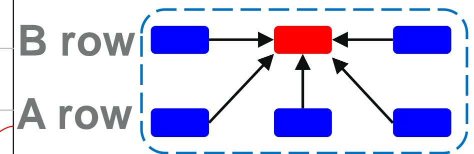


Green – B row pairs
Pink – A row pairs





Red - Top row Victim (5 Aggressors)

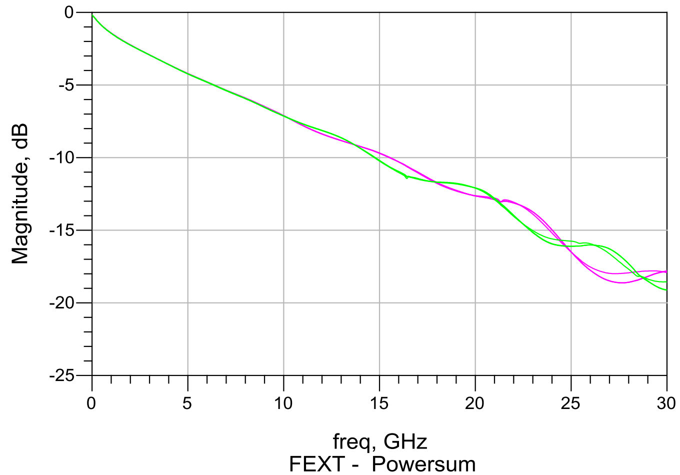


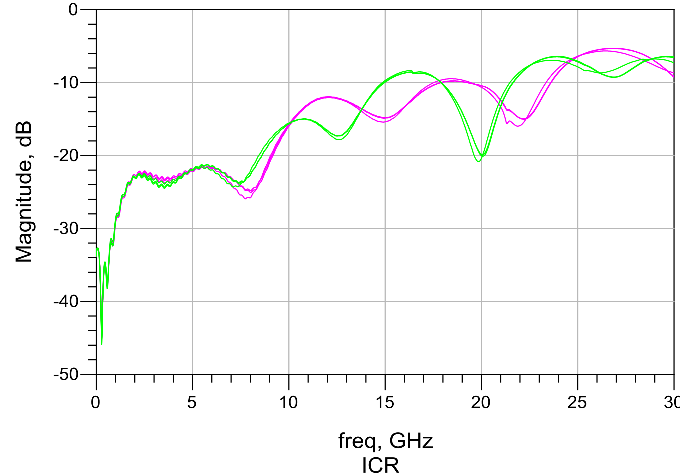
Actual data goes out to 42GHz and will be contributed as a Touchstone .s4p file for THRU and FEXT

TE connectivity

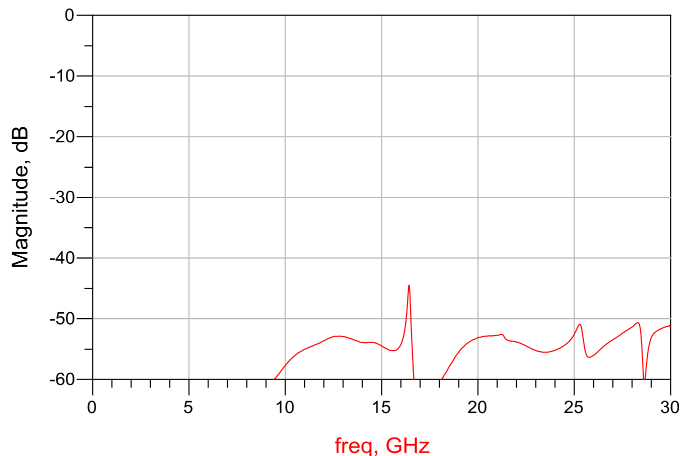
Channel Performance

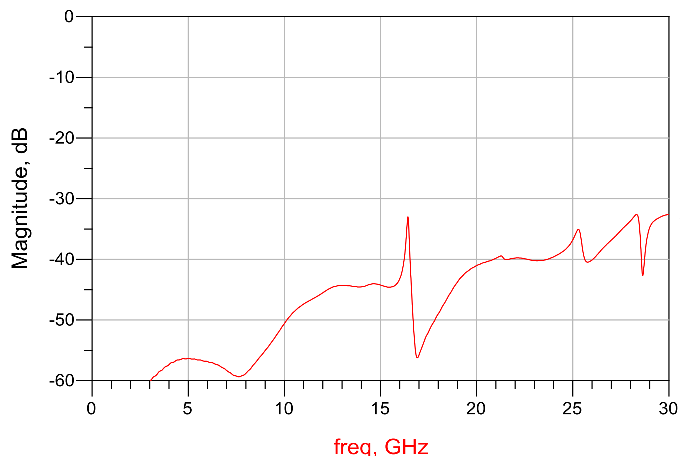
Next Generation 28Gbps High Density SMT IO with 10” Host



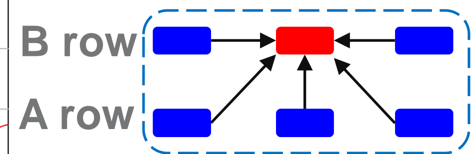


Green – B row pairs
Pink – A row pairs





Red - Top row Victim (5 Aggressors)

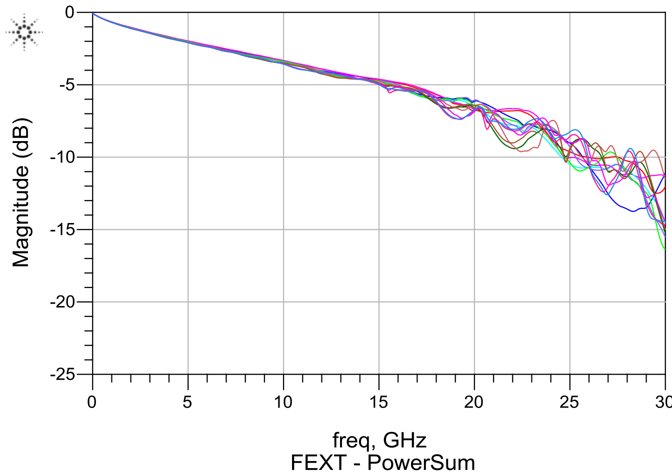


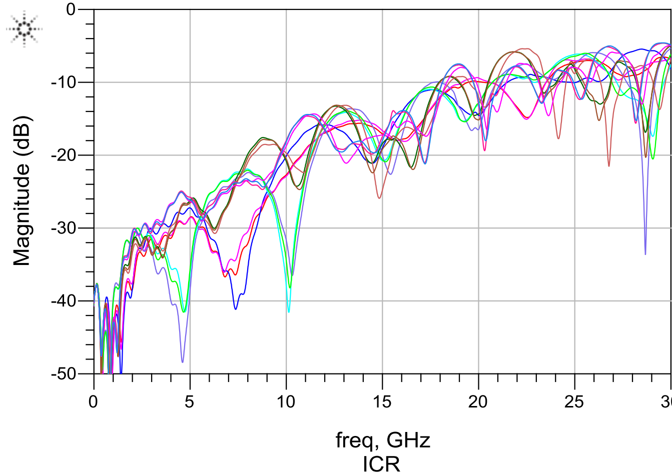
Actual data goes out to 42GHz and will be contributed as a Touchstone .s4p file for THRU and FEXT

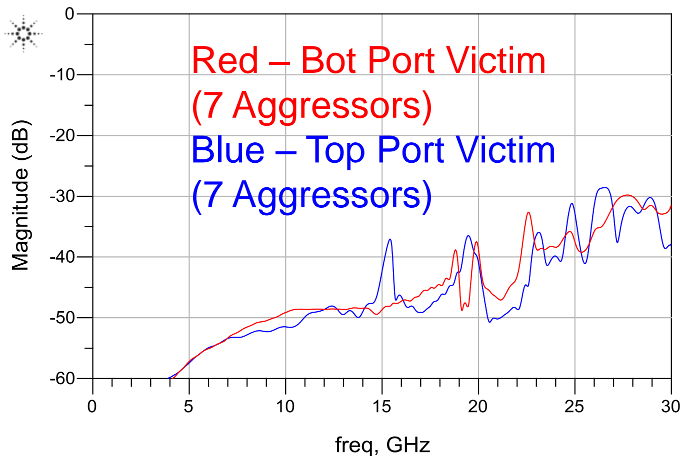
TE connectivity

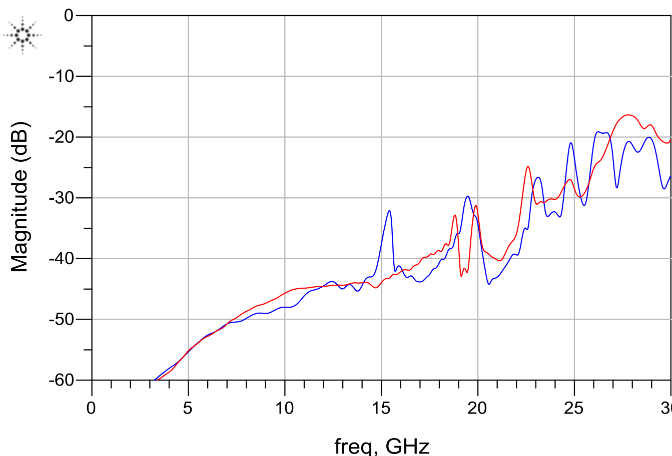
Channel Performance

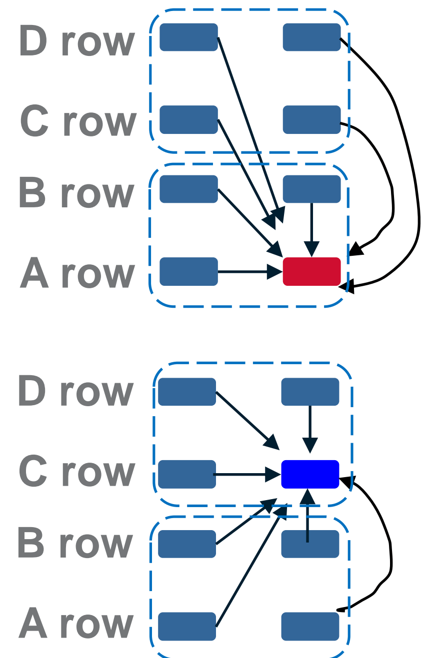
Next Generation 28Gbps Pressfit Stacked IO with 4” Host





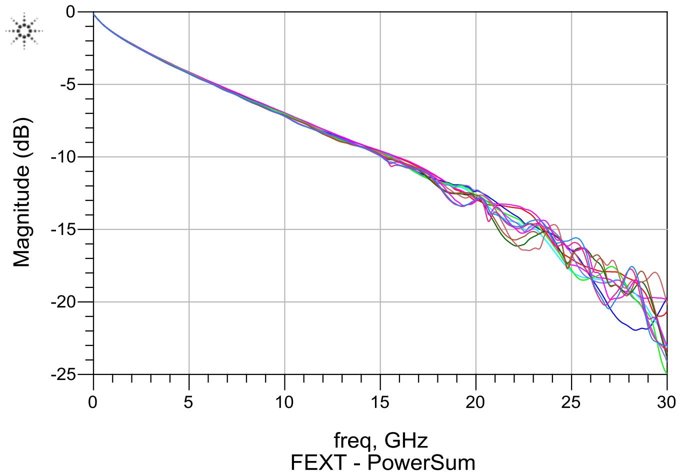


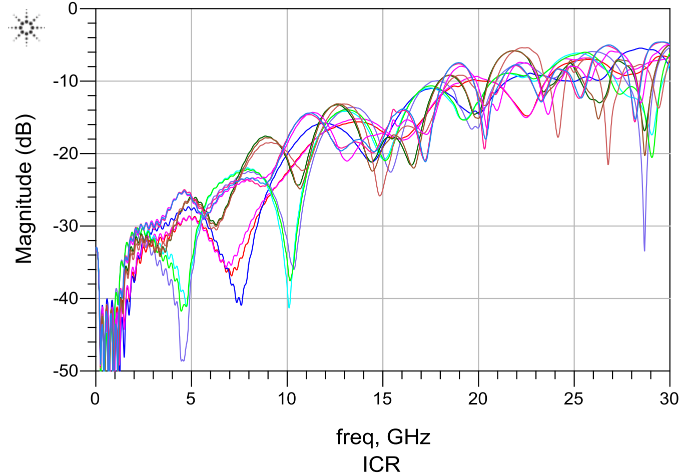


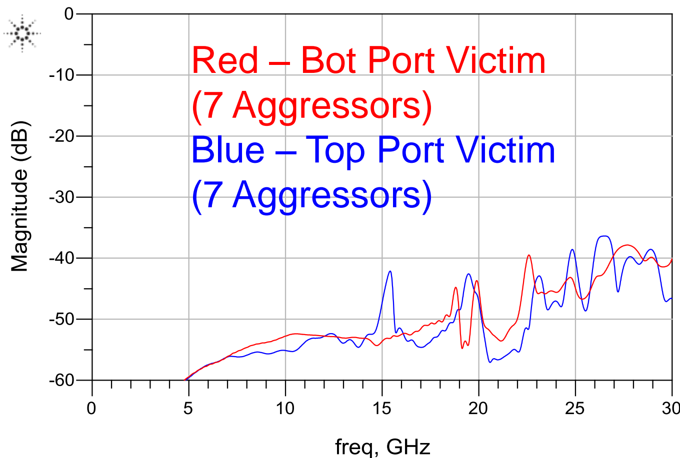


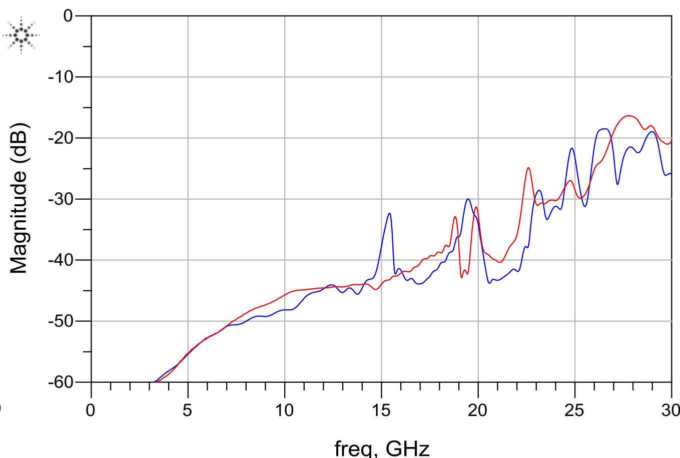
Channel Performance

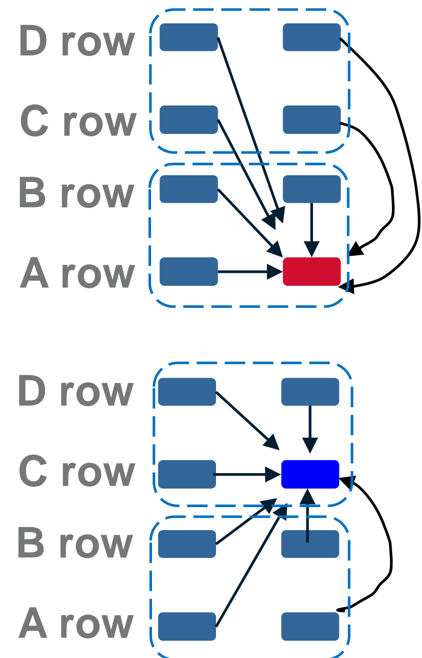
Next Generation 28Gbps Pressfit Stacked IO with 10" Host











TE connectivity

Summary

- Four revised channel models have been contributed for IEEE member analysis as 50Gbps channels
- Connector/channel power sum noise and ICR suggest these are good candidates for 50Gbps VSR/Chip-to-Module analysis
- Both solutions provide high density and use low cost PCB mating interfaces
- One surface mount and one press-fit allow consideration of both mounting conditions
- Feedback is solicited while the connector designs are not finalized