Electrical Interface Update

EA Meeting / Brocade Center
15 Oct 2014 Version r2

Opening

This is the personal view of Joel Goergen and not the view of IEEE P802.3bs. Joel Goergen makes no attempt to speak on behalf of the task force in any manor.

Please note the incredible work being done at this URL - http://www.ieee802.org/3/bs/public/adhoc/index.shtml

The Process Steps

The following simplified process steps are used to build consensus:

- Defining / Discussing Reach
- System Architecture
- **Channel Loss**
- **Modulation**
- Equalization
- Error Correction
- Power

We Are Here

From Sept 2014 Unapproved Minutes

Motion 4 (as modified by motion #5):

Move to adopt 16 x 25Gb/s and 8 x 50Gb/s as the basis for the lane rates for any optional C2C and C2M electrical interfaces

- - M: J. Goergen
- - S: V. Parthasarathy
- - Technical (>= 75%),
- - Y:102 ,N:0 ,A:4

Motion #6:

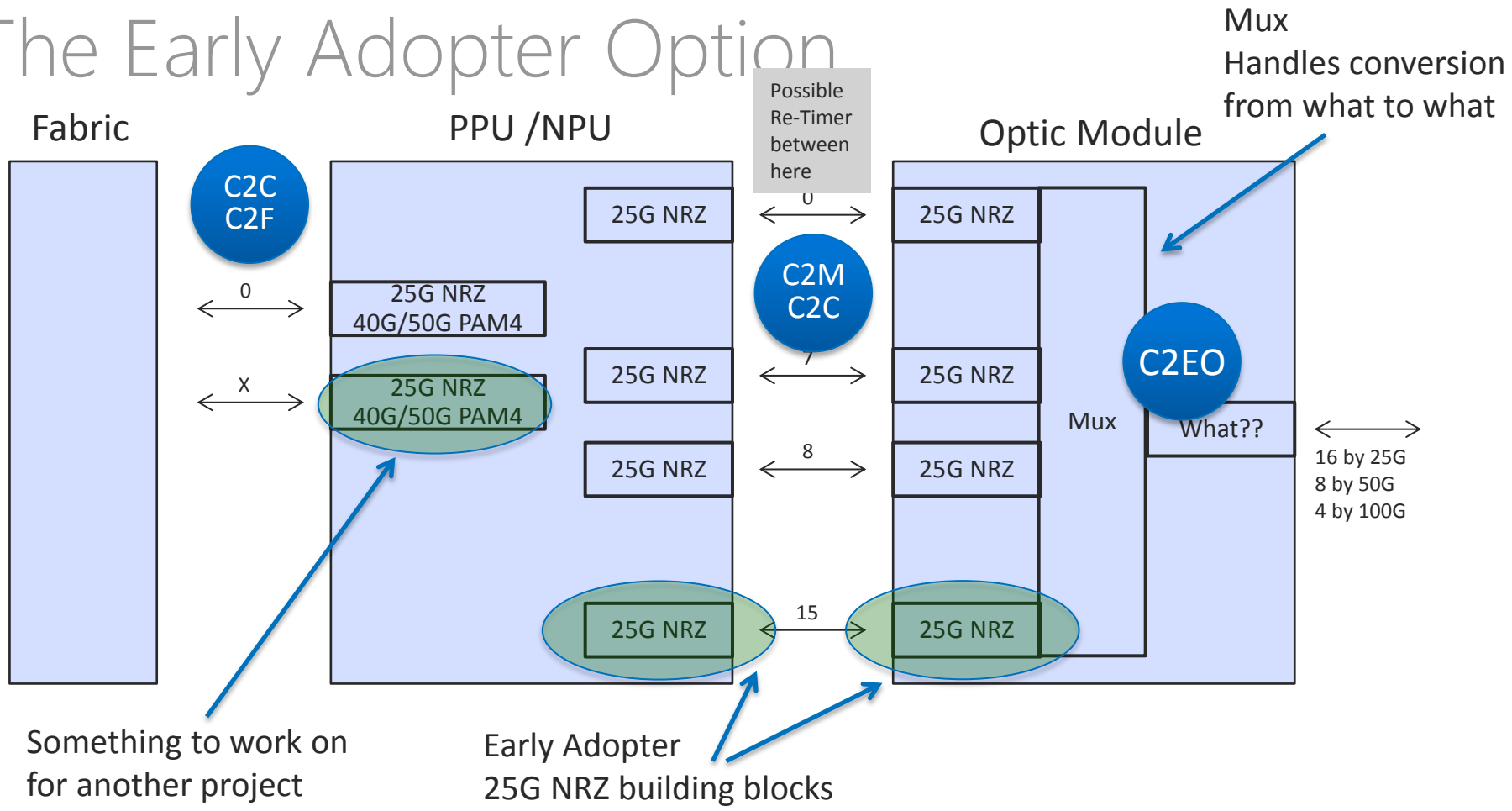
Move to adopt the P802.3bm C2C and C2M specifications with current values (except that the BER requirement is TBD) as a baseline draft for the 16 x 25Gb/s electrical interfaces

- - M: J. Goergen
- - S: V. Parthasarathy
- - Technical (>= 75%),
- - Y:78 ,N:0 ,A:18

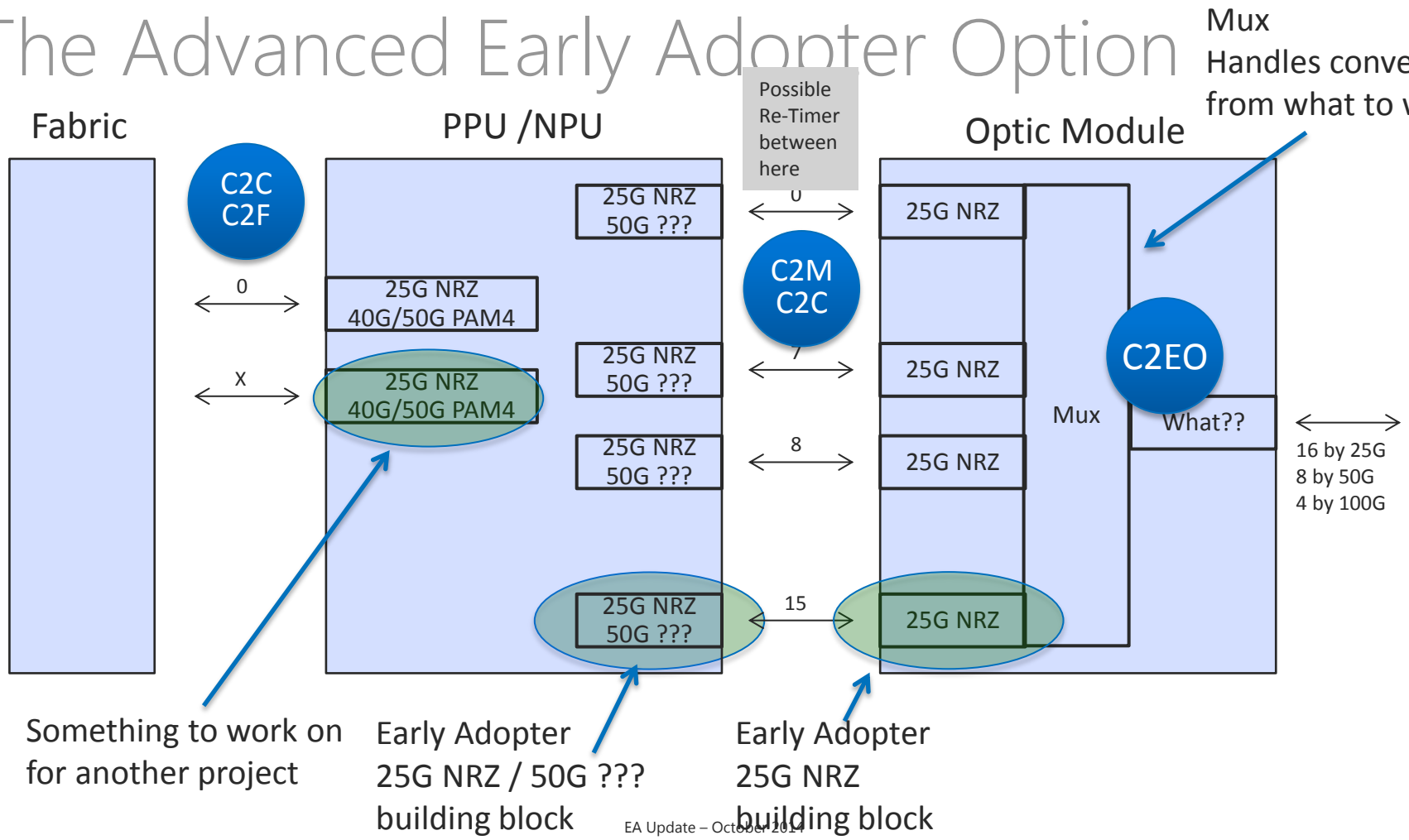
System Architectures

System building blocks at a high level

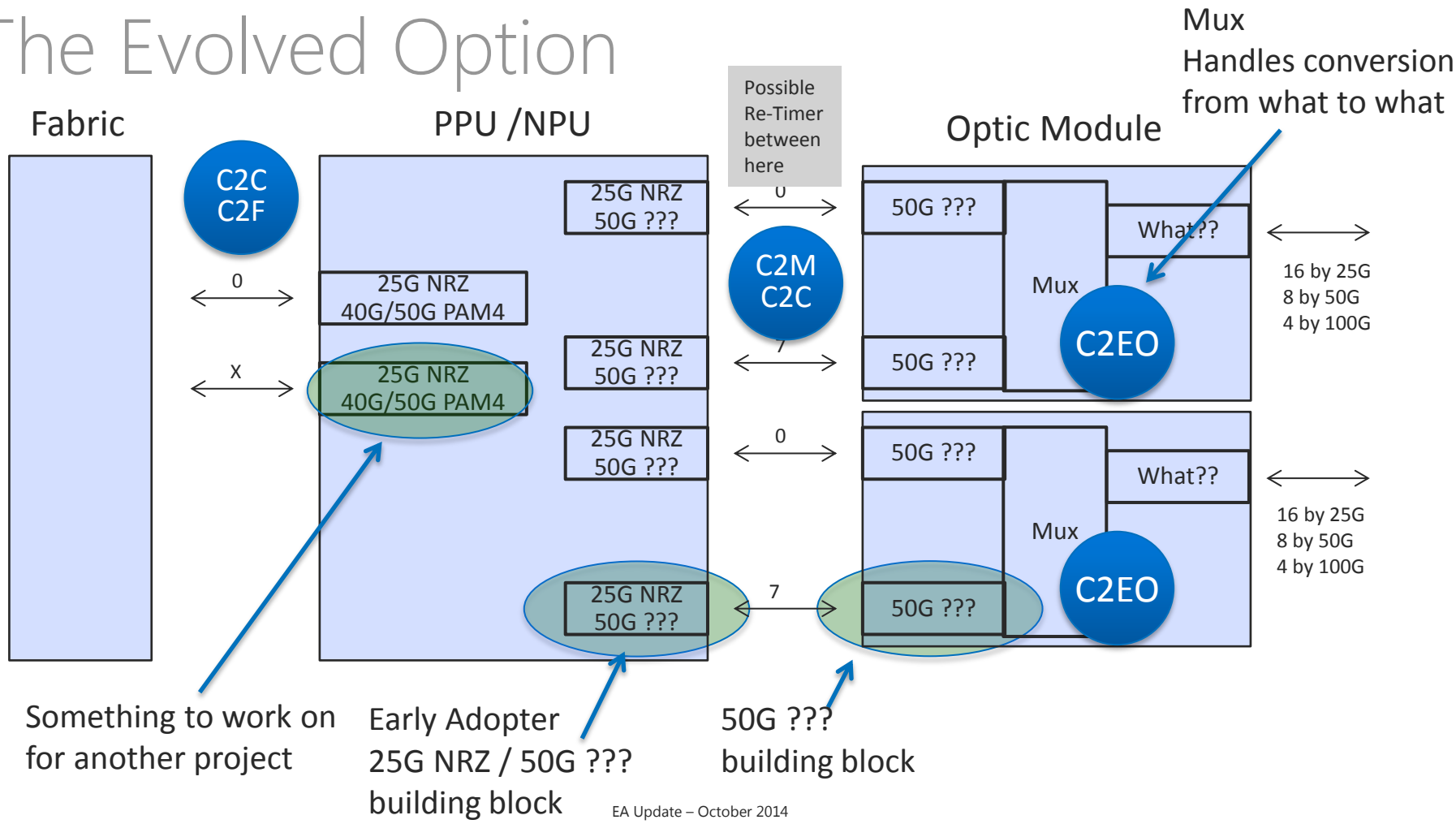
The Early Adopter Option



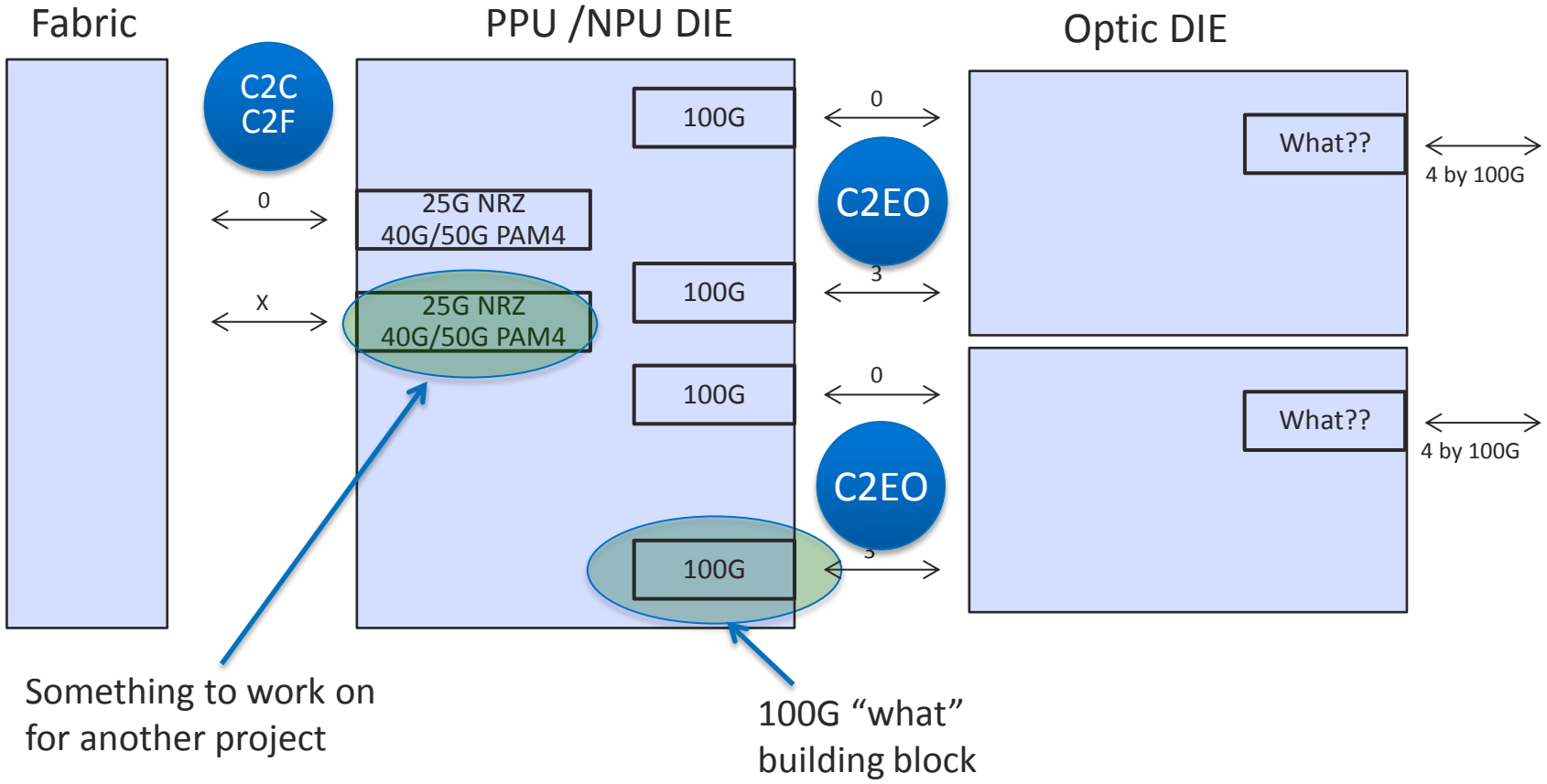
The Advanced Early Adopter Option



The Evolved Option

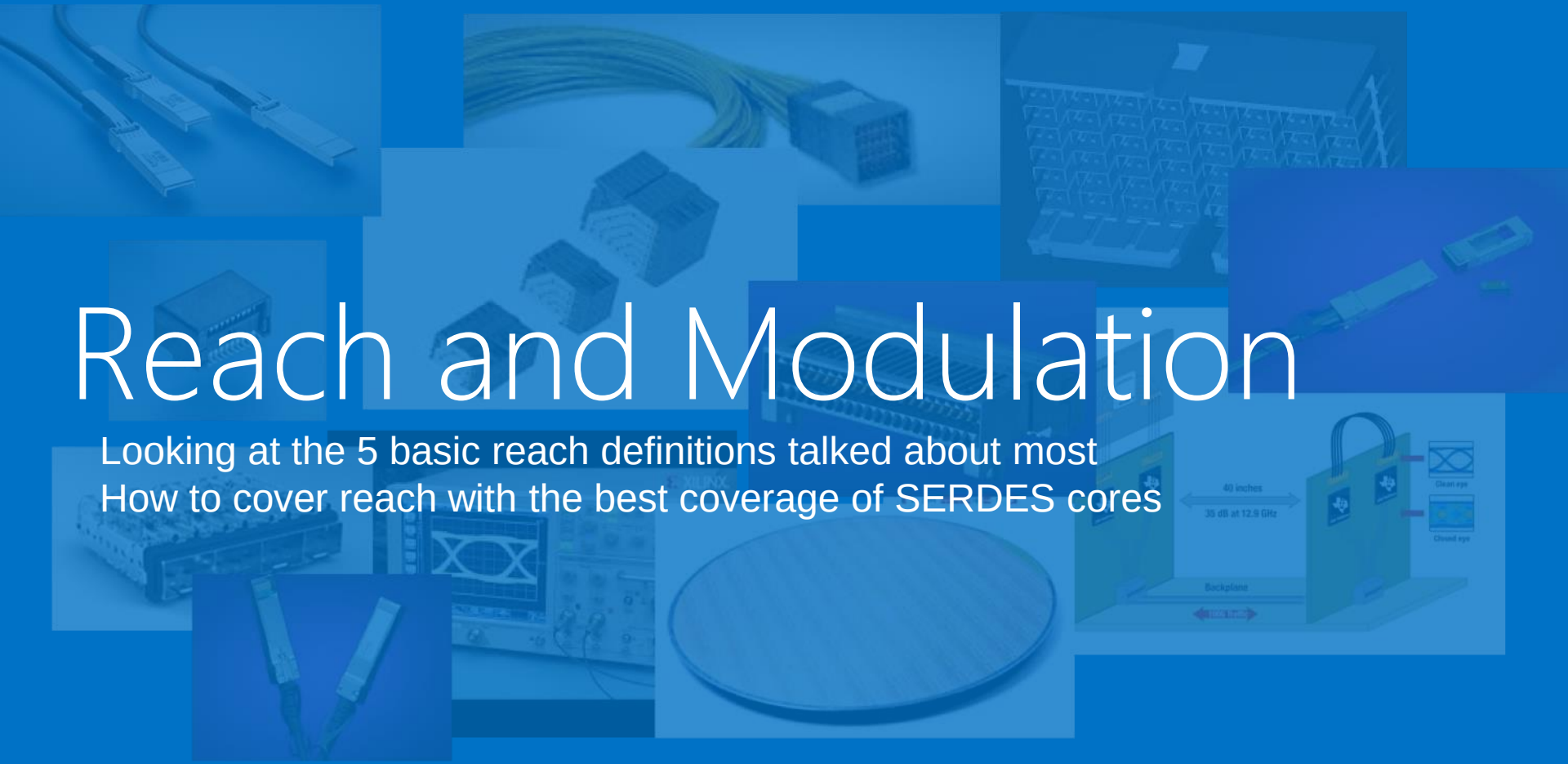


The Maybe-Some-day Option

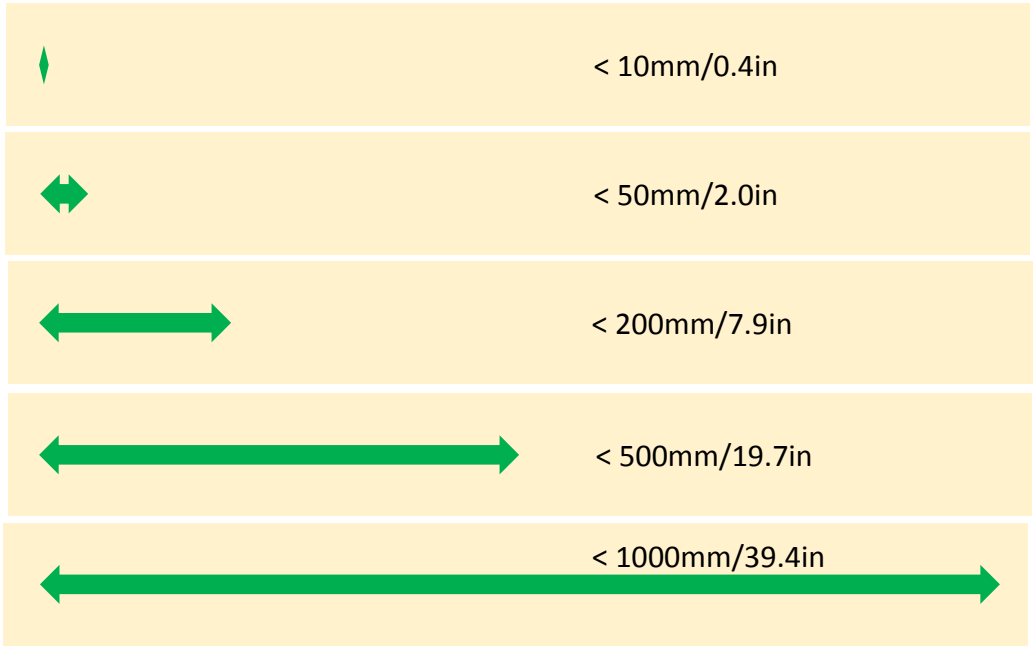


Reach and Modulation

Looking at the 5 basic reach definitions talked about most
How to cover reach with the best coverage of SERDES cores



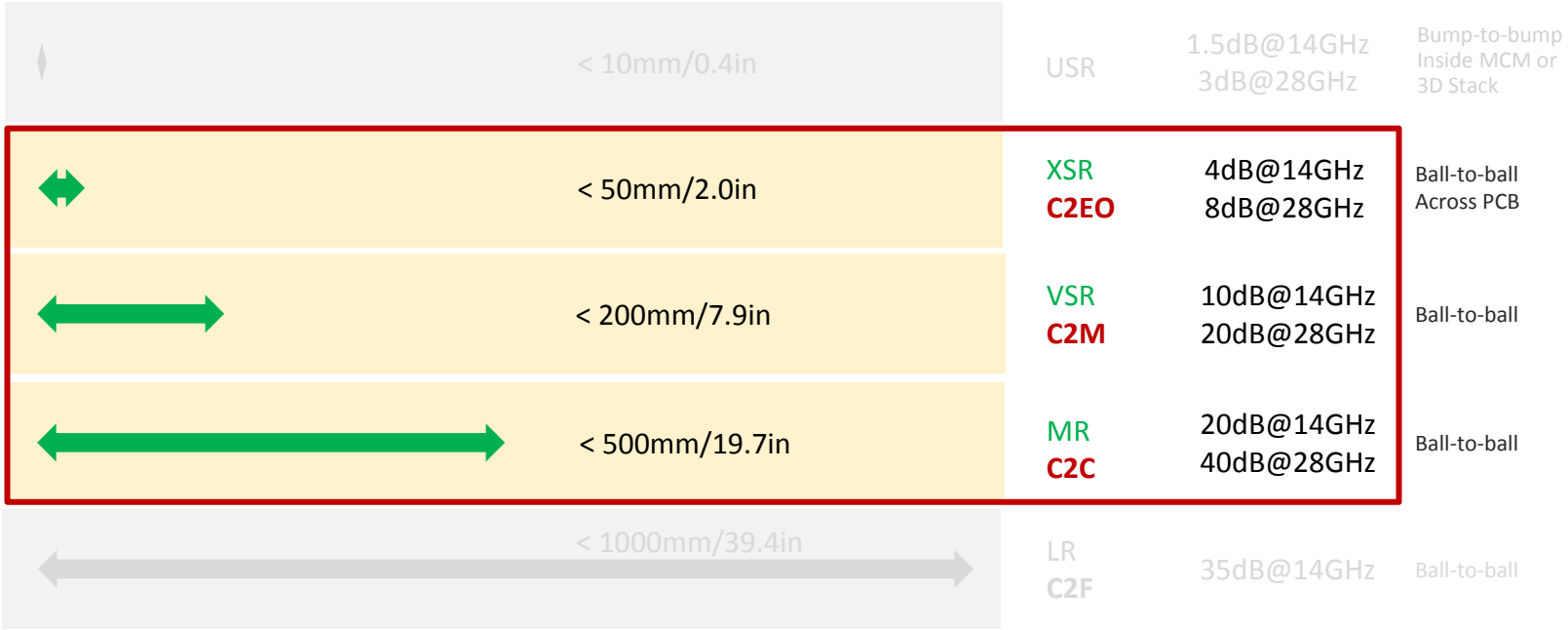
Length, Loss & Applications



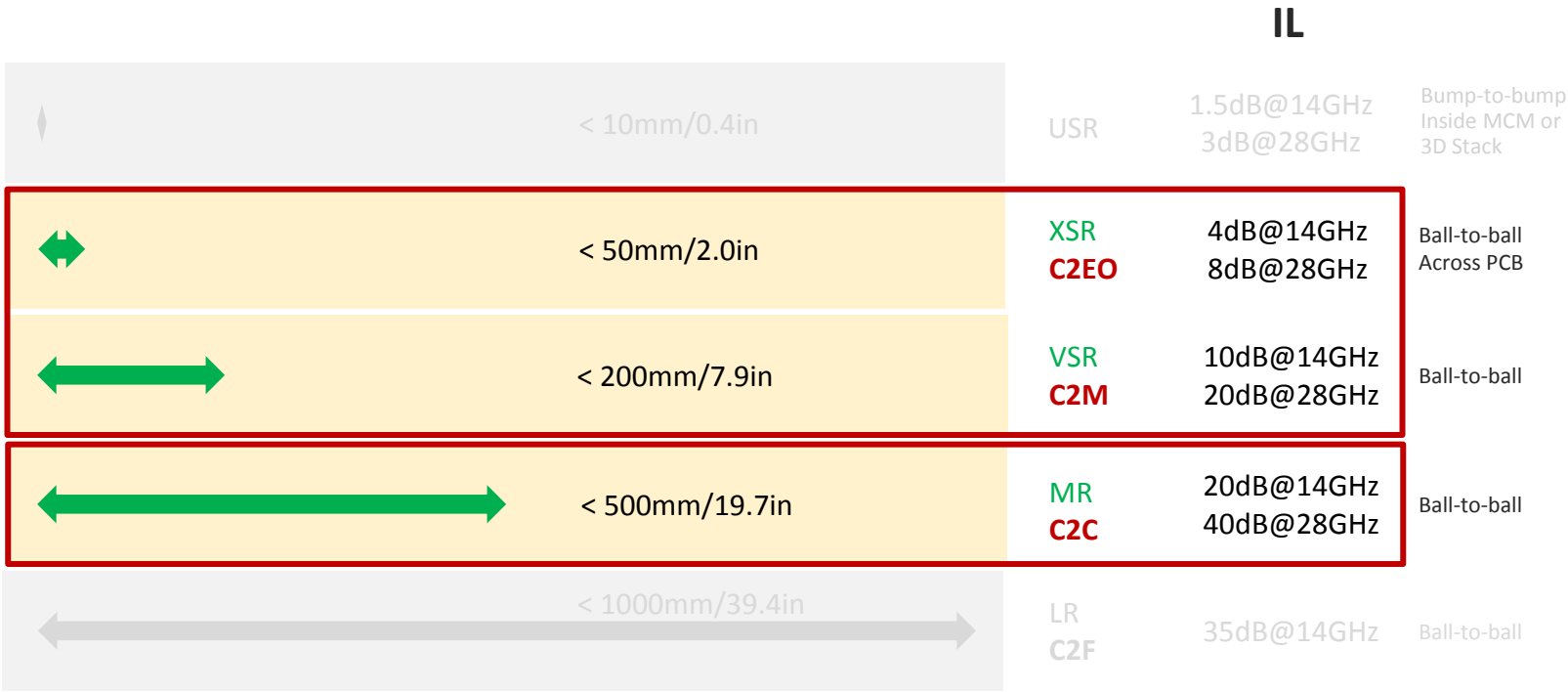
	IL	
USR	1.5dB@14GHz 3dB@28GHz	Bump-to-bump Inside MCM or 3D Stack
XSR **C2EO**	4dB@14GHz 8dB@28GHz	Ball-to-ball Across PCB
VSR **C2M**	10dB@14GHz 20dB@28GHz	Ball-to-ball
MR **C2C**	20dB@14GHz 40dB@28GHz	Ball-to-ball
LR **C2F**	35dB@14GHz	Ball-to-ball

Length, Loss & Applications:
Today a single 25GB/s SERDES core can cover all these ranges

These ranges can be easily covered with one SERDES core today for 25Gb/s.

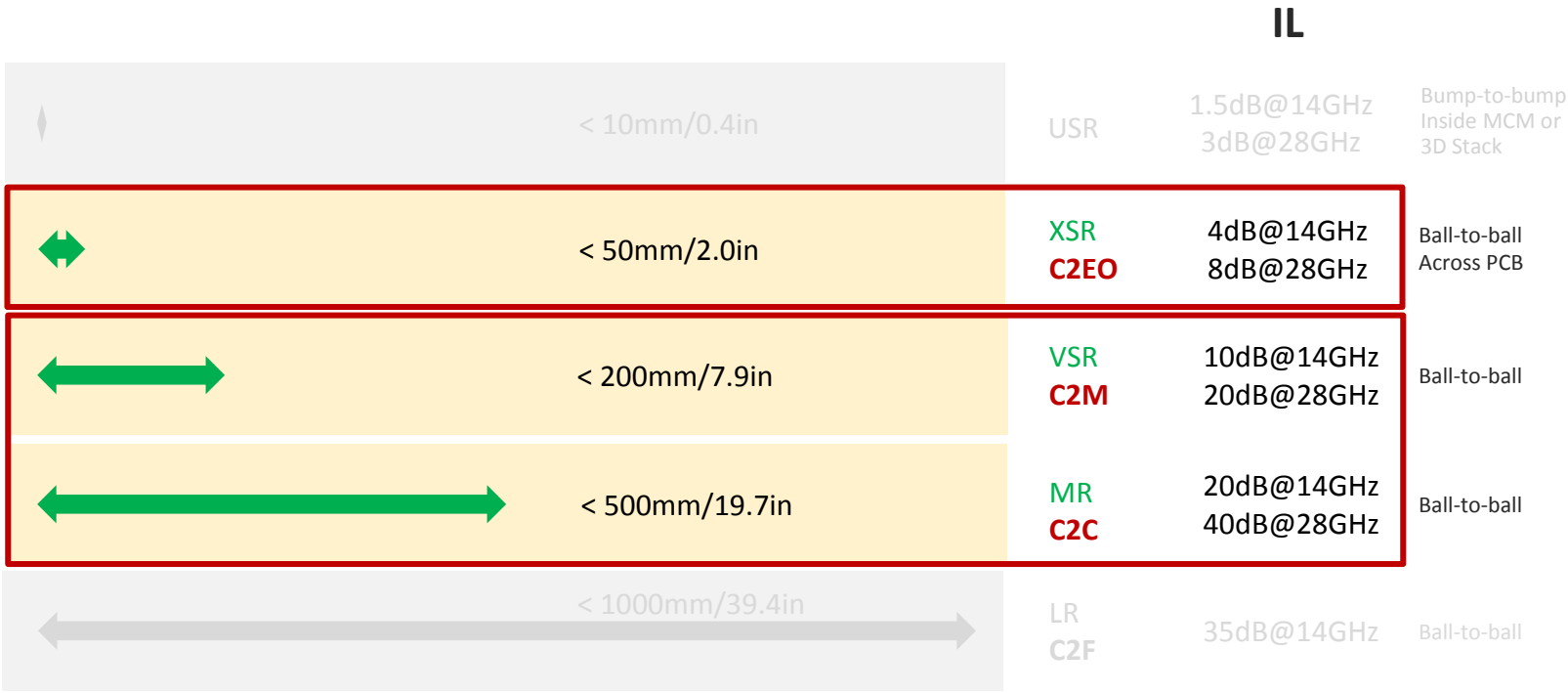


Length, Loss & Applications: Grouping (Perspective 1)
How does a 50Gb/s SERDES core cover these ranges optimally?



Unconfirmed but … Under the impression from the group the cores should be compatible

Length, Loss & Applications: Grouping (Perspective 2)
How does a 50Gb/s SERDES core cover these ranges optimally?



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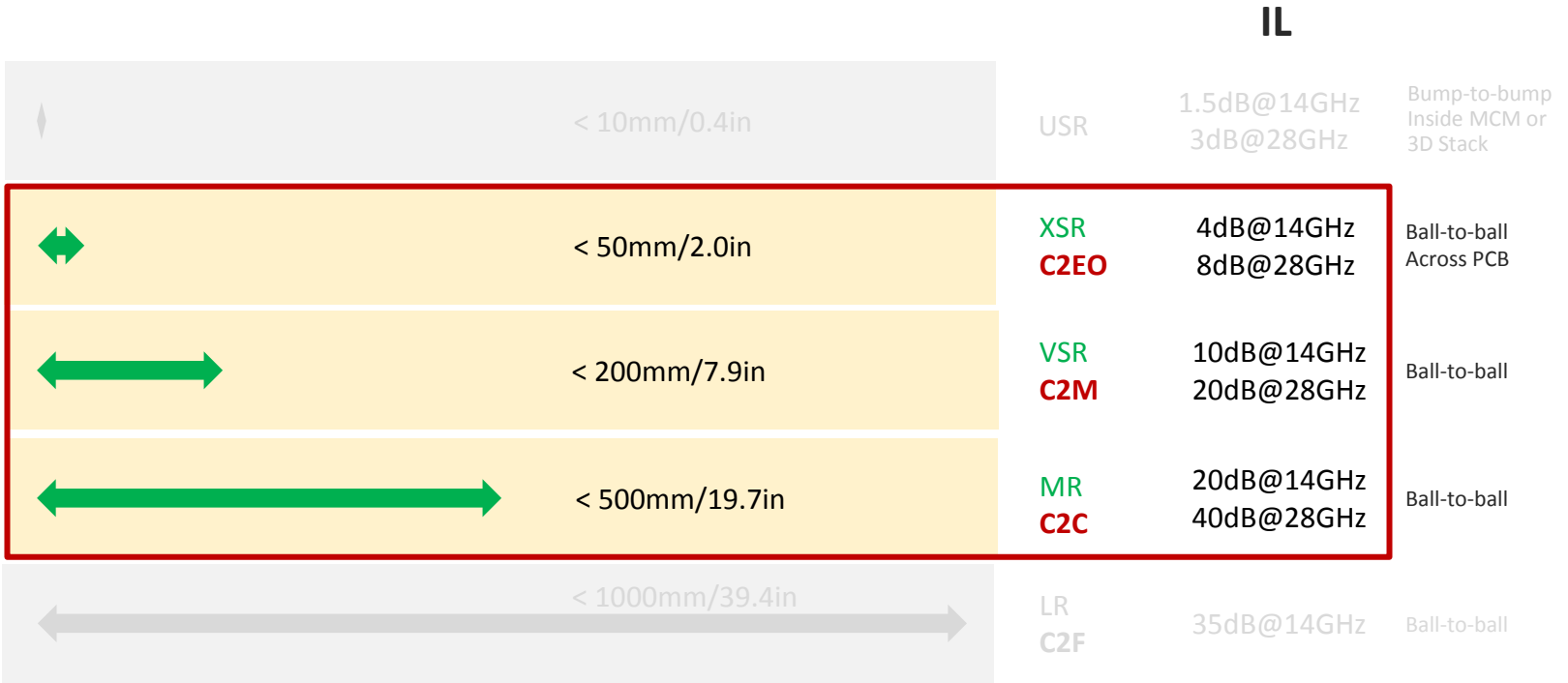
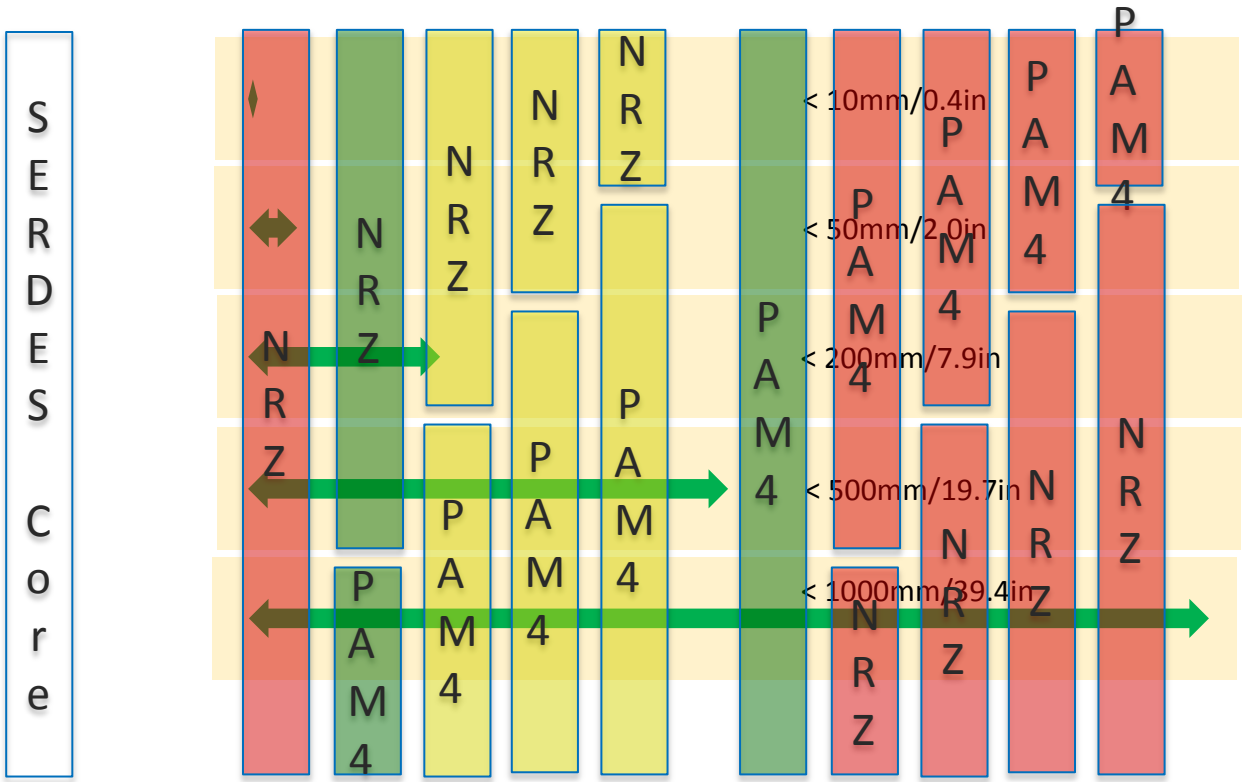
Length, Loss & Applications:
Future: a single 50GB/s SERDES core to cover all these ranges

These ranges should be covered with one SERDES core in the future for 50Gb/s.



I think the discussion comes down to this – even though we are only focused on C2C and C2M



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Not Really Feasible | Compatibility Concerns | Feasible Technology – Min Compatibility Concern

Confirming Action Item from Sept 2014 Meeting
Length, Loss & Application: Technologies for 50Gb/s

These Values are under discussion

Application	Length	Loss	Modulation	pJ/bit	DFE?	FEC?
C2EO (XSR)	< 2in	<4dB@14GHz	PAM-4	TBD	TBD	TBD
		<8dB@28GHz	NRZ	TBD	TBD	TBD
C2M (VSR)	2-8in	4-10dB@14GHz	PAM-4	TBD	TBD	TBD
		8-20dB@28GHz	NRZ	TBD	TBD	TBD
C2C (MR)	8-20in	10-20dB@14GHz	PAM-4	TBD	TBD	TBD
		20-40dB@28GHz	NRZ	TBD	TBD	TBD

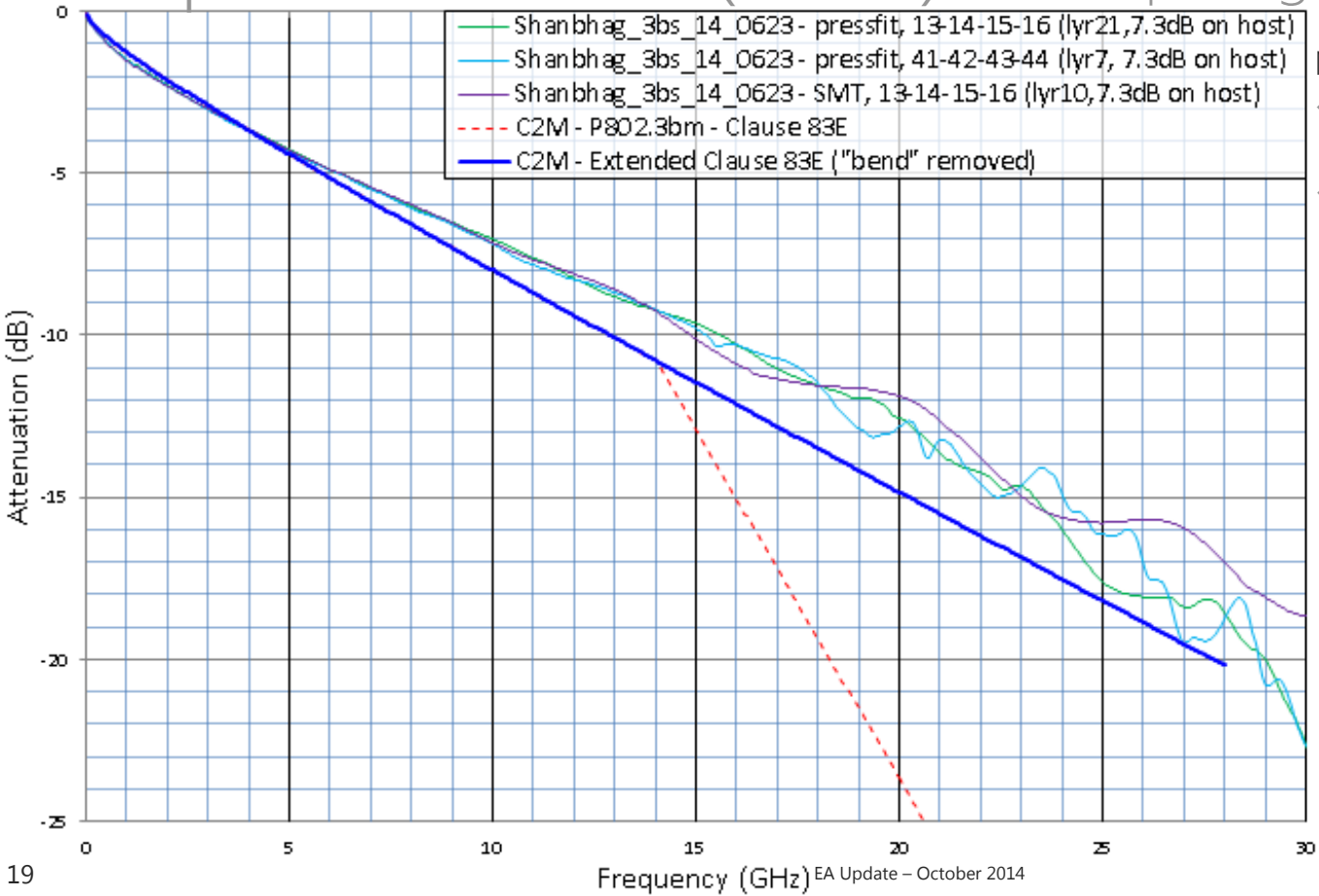
Knowing the reach definition allows us to begin understanding the next steps in the consensus building process

- System Architecture
- Channel Loss
- Modulation
- Equalization
- Error Correction
- Power

Sandy Limit Lines

Looking at some possible limit lines to guide channel definitions for modulation simulation

Chip-to-Module (C2M) – Comparing channel data

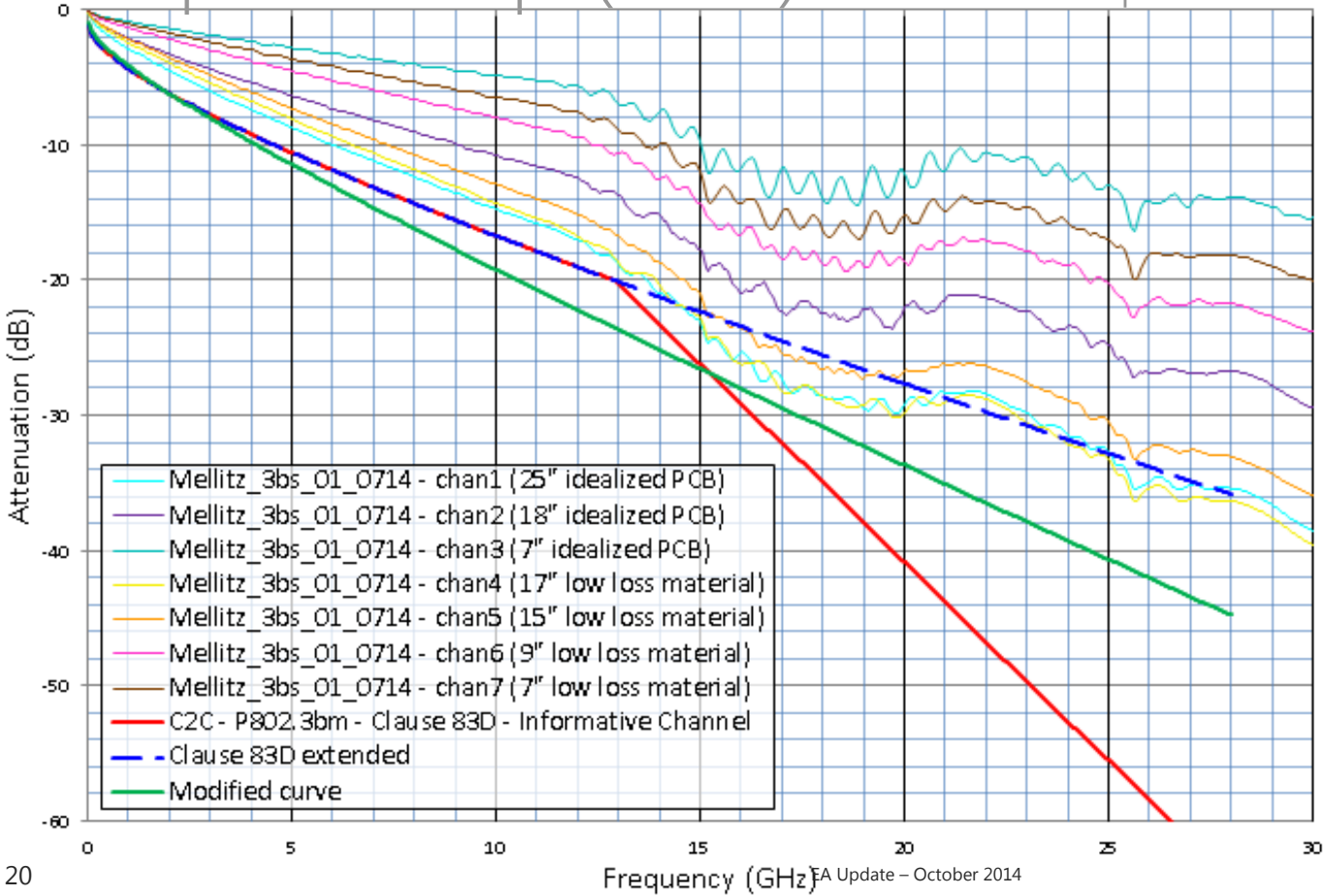


Notes:

- TE Channels developed using HFSS/ADS modeling tools.
- The 4″ host trace is and should be supported at mid-loss materials by 100G standards… 7″ is certainly seen in designs, but industries seem to recognize and adjust with material and design tradeoffs.

Propose: Use extended CAUI4 C2M–like channels for Modulation discussion/comparison

Chip-to-Chip (C2C) – Let's compare to channel data.



Notes:

← Channels are public on the .3bs webpage… all channels include connector and an 8% impedance variation from motherboard to daughtercard.

←Are these channels right to use for modulation discussion?

←Is ILD pessimistic for educated 50G channel design?

Sandy Line
Equations plotted for C2C and C2M

802.3bm draft – C2M equation (red curve)

$$Insertion\_loss(f) \le \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.076(-18 + 2f) & 14 \le f < 18.75 \end{cases} \text{ (dB)} \qquad \text{(83E–1)}$$

802.3bm draft – c2C equation (red curve) *although, standard uses COM as the normative spec, the following is offered as the informative "limit" line

$$Insertion\_loss(f) \le \begin{cases} 1.083 + 2.543\sqrt{f} + 0.761f & 0.01 \le f < 12.89 \\ -17.851 + 2.936f & 12.89 \le f < 25.78 \end{cases} \text{ (dB)} \qquad \text{(83D–1)}$$

C2M and C2C "extended curve" (blue curves)

Simply extend first portion of above curves for full frequency range; omit 14-18.75G and 12.89-25.78G equations, respectively.

Suggested/modified curve drawn in C2C (green curve)

$$0.9 + 2.1\sqrt{f} + 1.17f$$

Next Steps

Next Steps to Nov 2014 Proposals

- Use the C2C and C2M channels submitted to the P802.3bs and provide a modulation scheme.
- Reach consensus on which channel groupings (LR/MR-C2C/VSR-C2M/XSR/USR) make sense from power/performance tradeoffs based on simulations

Thank you!

From:
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