Draft Baseline Proposal for CDAUI-8 Chip-to-Module (c2m) Electrical Interface

CDAUI-8 c2m Baseline Document Supporters *

Contributors and Supporters

- David Brown, Semtech
- Philip Fisher, Avago Technologies
- Ed Frlan, Semtech
- Adam Healey, Avago Technologies
- Cathy Liu, Avago Technologies
- Mike Peng Li, Altera

Supporters†

Sudeep Bhoja, InPhi
Will Bliss, Broadcom
Matt Brown, Applied Micro
Sacha Corbeil, JDSU
Mike Furlong, Clariphy
Mark Gustlin, Xilinx
Zhensheng Jia, ZTE
Scott Kipp, Brocade
Elizabeth Kochuparambil, Cisco
Ryan Latchman, MACOM
Greg LeCheminant, Keysight
David Lewis, JDSU
Jeff Maki, Juniper
David Ofelt, Juniper
Vineet Salunke, Cisco
Jeff Slavick, Avago
Bharat Tailor, Semtech
Vivek Telang, Broadcom
Alan Tipper, Semtech
Pirooz Tooyserkani, Cisco
Francois Tremblay, Semtech
Michael Vitic, JDSU
Xinyuan Wang, Huawei
Helen Xu, Huawei
Pavel Zivny, Tektronix

† Supporters of brown_3bs_01b_1114

* Changes shown in red

Purpose

- Present a baseline specification proposal for CDAUI-8 c2m electrical interface in support the 400 GbE to fulfill its objective of:

  Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications

*

Technology Choice Highlights 1

- Channel target/requirement based on that of “informative insertion loss budget” from the electrical interface ad hoc
  - PAM4 signaling and system is intended to work over existing CAUI-4 c2m infrastructures
- Channel equalization based on a transceiver having autonomous Rx CTLE
  - Tx FIR or Rx DFE not specified in host or module transceivers

Technology Choice Highlights 2

- Raw BER of CDAUI-8 c2m link to be < 1e-6; FEC brings link system BER to < 1e-15

Technology Choice Highlights 3 *

- Leverage the CEI-56G-VSR-PAM4 specification[1] using two data rates:
  - 25.78 GBd, for links without overclocking
  - ~28 GBd, final value depending on the final FEC choice
- Gray-code specified, FEC assumed but not specified, no pre-coding
- Reuse KP4 test patterns
- Reuse CAUI-4 c2m Tx and Rx methodologies for specifying electrical characteristics and corresponding tests
  - Diff and CM RLs and compliance point definitions
  - HCB/MCB method for channel compliance, adapted for PAM-4 signaling
  - Remove “recommended CTLE” mechanism

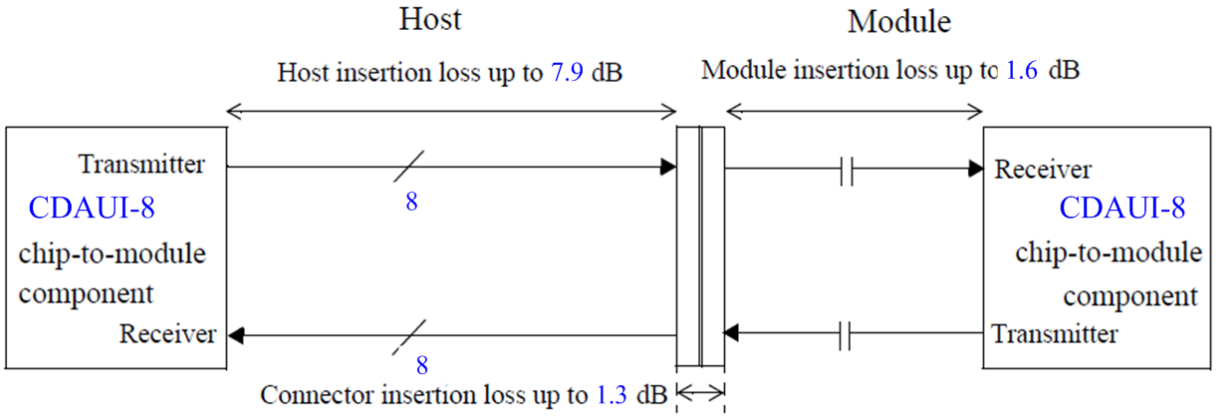
CDAUI-8 Chip-to-Module Link *

	CAUI-4 (83E.3.1 TP1a)	VSR 56G (15.3.2, TP1a)	CDAUI-8 Chip-Module Potential
Modulation	NRZ	PAM-4 (Gray coded)	PAM-4 (Gray coded)
Nominal Signaling Rate (each lane)	25.78125 Gb/s +/- 100 ppm	19.6 ≤ fb ≤ 30 GBd	25.78125 GBd +/- 100 ppm, 28 GBd (TBD)[a] +/- 100 ppm
Unit Interval	38.787879 ps	33.33 ps - 51 ps	38.78789 ps, 35.65 ps (TBD)[a]
Loss Budget, max[b]	10 dB	10.8 dB[c]	10.8 dB
Uncorrected BER	< 1e-15	< 1e-6	< 1e-6
Corrected BER	n/a	n/a	< 1e-15

[a] Two operating signaling rates, with choice of higher rate pending PMA FEC selection.

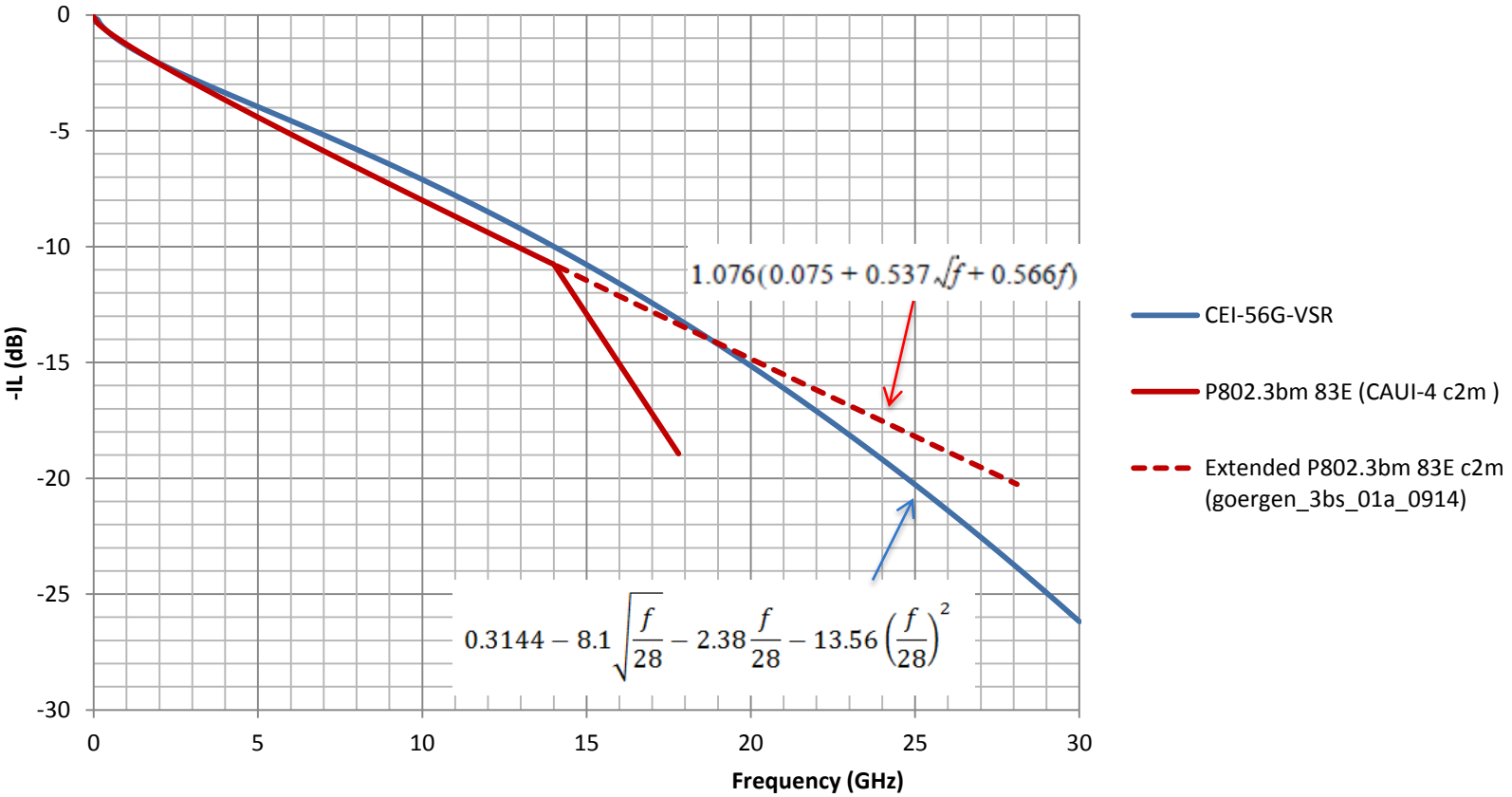
[b] At 1/2 symbol rate, comprising host PCB trace, module PCB trace, AC-coupling capacitors and one connector.

[c] Informative.



Chip-to-module insertion loss budget at 14 GHz

CDAUI-8 c2m PAM4 Channel Insertion Loss *



- Target IL curve TBD, pending 56Gb/s channel modeling and measurements
  - All curves shown can accommodate PAM4 signaling at 28GBd
  - Lower CAUI-4 c2m curve enables reuse of legacy 25G NRZ channels

CDAUI-8 Host Transmitter

	CAUI-4 (83E.3.1 TP1a)	VSR 56G (15.3.2, TP1a)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak output voltage (max) with Tx enabled	900 mV	900 mV	900 mV
AC common-mode output voltage (max)	17.5 mVrms	17.5 mVrms	17.5 mVrms
Differential peak-to-peak output voltage (max) with Tx disabled	35 mV	-	35 mV
Differential termination mismatch (max)	10 %	10 %	10 %
Differential output return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Common-mode to differential output return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Common-mode output return loss (min)	-	2 dB	2 dB
DC common-mode output voltage (max)	2.8 V	2.8 V	2.8 V
DC common-mode output voltage (min)	-0.3 V	-0.3 V	-0.3 V
Eye Width (min)	0.46 UI at 1e-15	0.25 UI at 1e-6 applicable to all three PAM4 eyes	0.25 UI at 1e-6 applicable to all three PAM4 eyes
Output total jitter (max)	TJ: 0.54UIpp @ 1e-15 Measured using CTLE	TJ: 0.75UIpp @ 1e-6 Measured using CTLE	TJ: 0.75UIpp @ 1e-6 Measured using CTLE
Signal-to-noise-and-distortion ratio	-	-	-
Eye Height (min)	95 mV at 1e-15	50 mV at 1e-6 applicable to all three PAM4 eyes	50 mV at 1e-6 applicable to all three PAM4 eyes
Transition time (min, 20/80%)	10 ps	-	-

CDAUI-8 Module Receiver

	CAUI-4 (83E.3.1 TP1)	VSR 56G (15.3.2, TP1)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak input voltage tolerance (min)	900 mV	900 mV	900 mV
Single-ended voltage tolerance range (min)	-0.4 to 3.3 V	-	-
DC common-mode input voltage (max)	2.85 V	2.85 V	2.85 V
DC common-mode input voltage (min)	-0.35 V	-0.35 V	-0.35 V
Differential termination mismatch (max)	10 %	10 %	10 %
Differential input return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Differential to common mode input return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Module stressed input test	83E.3.4.1	15.3.10.2.1	Same as VSR

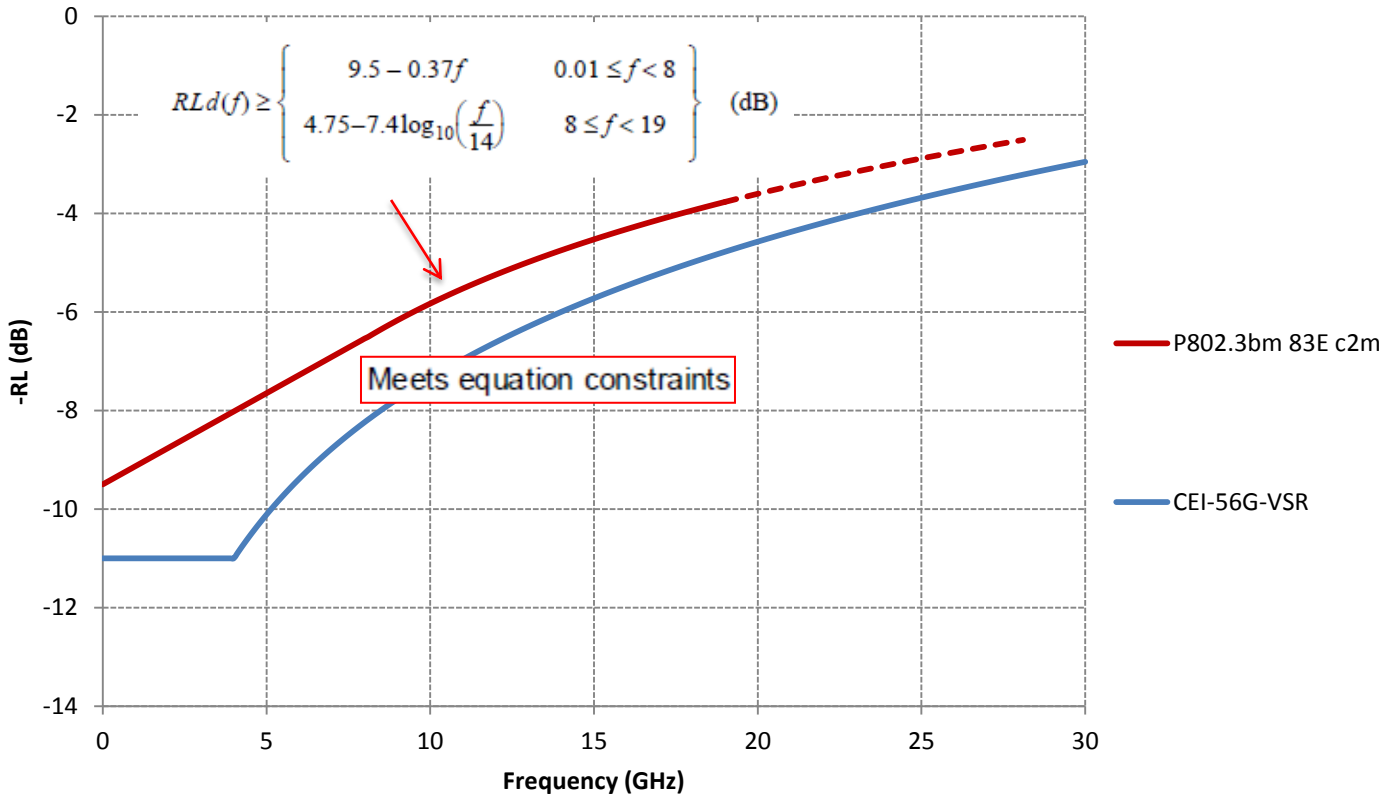
CDAUI-8 Module Transmitter

	CAUI-4 (83E.3.2 TP4)	VSR 56G (15.3.3, TP4)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak output voltage (max) with Tx enabled	900 mV	900 mV	900 mV
AC common-mode output voltage (max)	17.5 mVrms	17.5 mVrms	17.5 mVrms
Differential termination mismatch (max)	10 %	10 %	10 %
Differential output return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Common-mode to differential mode output return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Common-mode output return loss (min)	-	2 dB	2 dB
DC common-mode output voltage (max)	2.85 V	2.85 V	2.85 V
DC common-mode output voltage (min)	-0.35 V	-0.35 V	-0.35 V
Eye Width (min)	0.57 UI at 1e-15	0.4 UI at 1e-6 applicable to all three PAM4 eyes	0.4 UI at 1e-6 applicable to all three PAM4 eyes
Output total jitter (max)	TJ: 0.43UIpp @ 1e-15 Measured using CTLE	TJ: 0.6UIpp @ 1e-6 Measured using CTLE	TJ: 0.6UIpp @ 1e-6 Measured using CTLE
Signal-to-noise-and-distortion ratio (min)	-	-	-
Eye Height (min)	228 mV at 1e-15	120 mV at 1e-6 applicable to all three PAM4 eyes	120 mV at 1e-6 applicable to all three PAM4 eyes
Transition time (min, 20/80%)	12 ps	-	-

CDAUI-8 Host Receiver

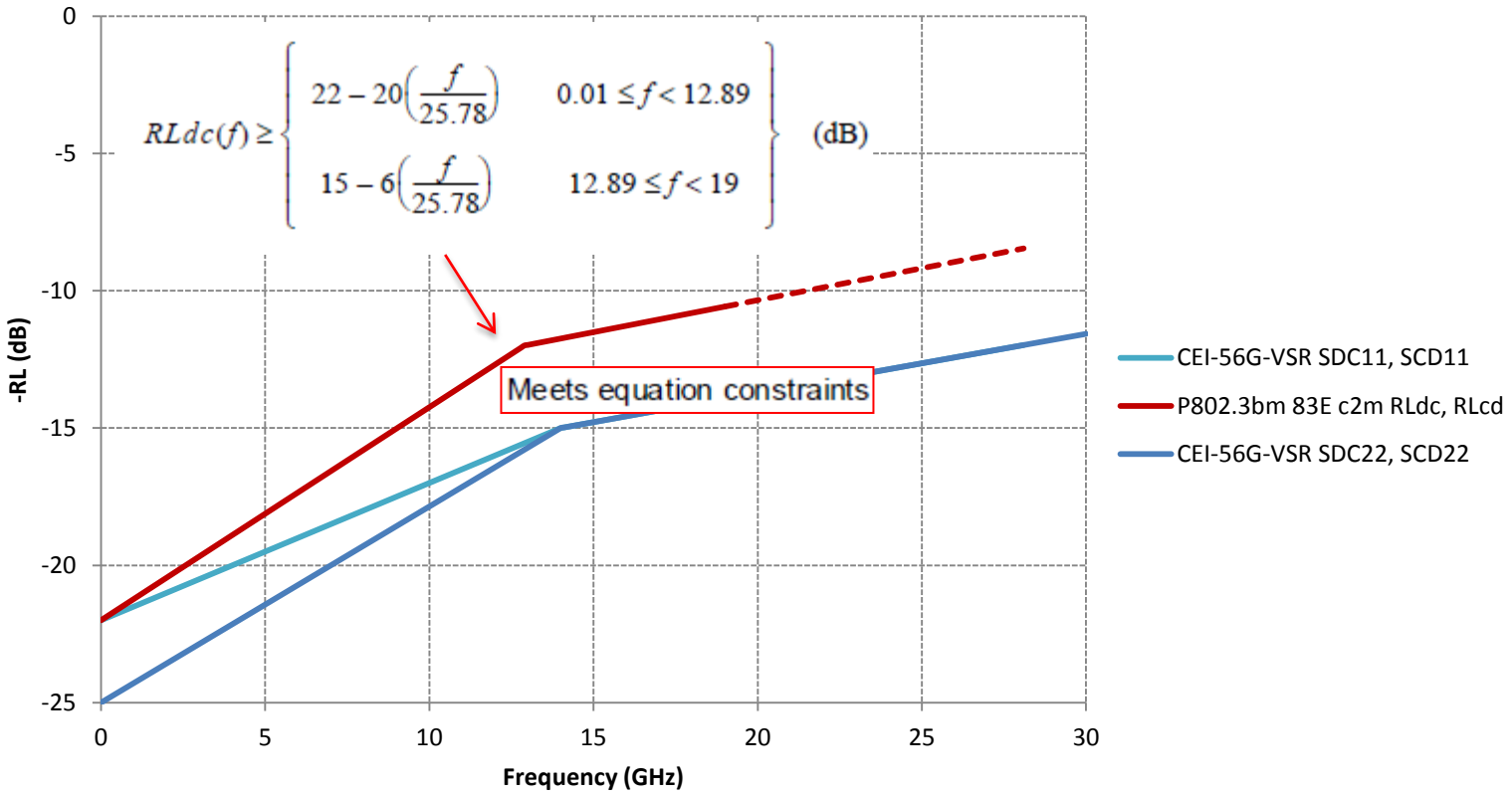
	CAUI-4 (83E.3.2 TP4a)	VSR 56G (15.3.2, TP4a)	CDAUI-8 Chip-Module Potential
Differential peak-to-peak input voltage tolerance (min)	900 mV	900 mV	900 mV
DC common-mode input voltage (max)	2.8 V	2.8 V	2.8 V
DC common-mode input voltage (min)	-0.3 V	-0.3 V	-0.3 V
Differential termination mismatch (max)	10 %	10 %	10 %
Differential input return loss (min)	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz	≥ 11, 0.05≤f≤fb/7 GHz ≥ 6-9.2log$_{10}$(2f/fb), fb/7≤f≤fb GHz	≥ 9.5-0.37f, 0.01≤f≤8 GHz ≥ 4.75-7.4log$_{10}$(f/14), 8≤f≤19 GHz
Differential to common-mode input return loss (min)	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz	≥ 22-14f/fb, 0.05≤f≤fb/2 GHz ≥ 18-6f/fb, fb/2≤f≤fb GHz	≥ 22-(20/25.78)f, 0.01≤f≤12.89 GHz ≥ 15-(6/25.78)f, 12.89≤f≤19 GHz
Host stressed input test	83E.3.3.2	15.3.10.2.1	Same as VSR
Jitter tolerance	-	-	-

CDAUI-8 c2m Tx & Rx Differential Return Loss Spec



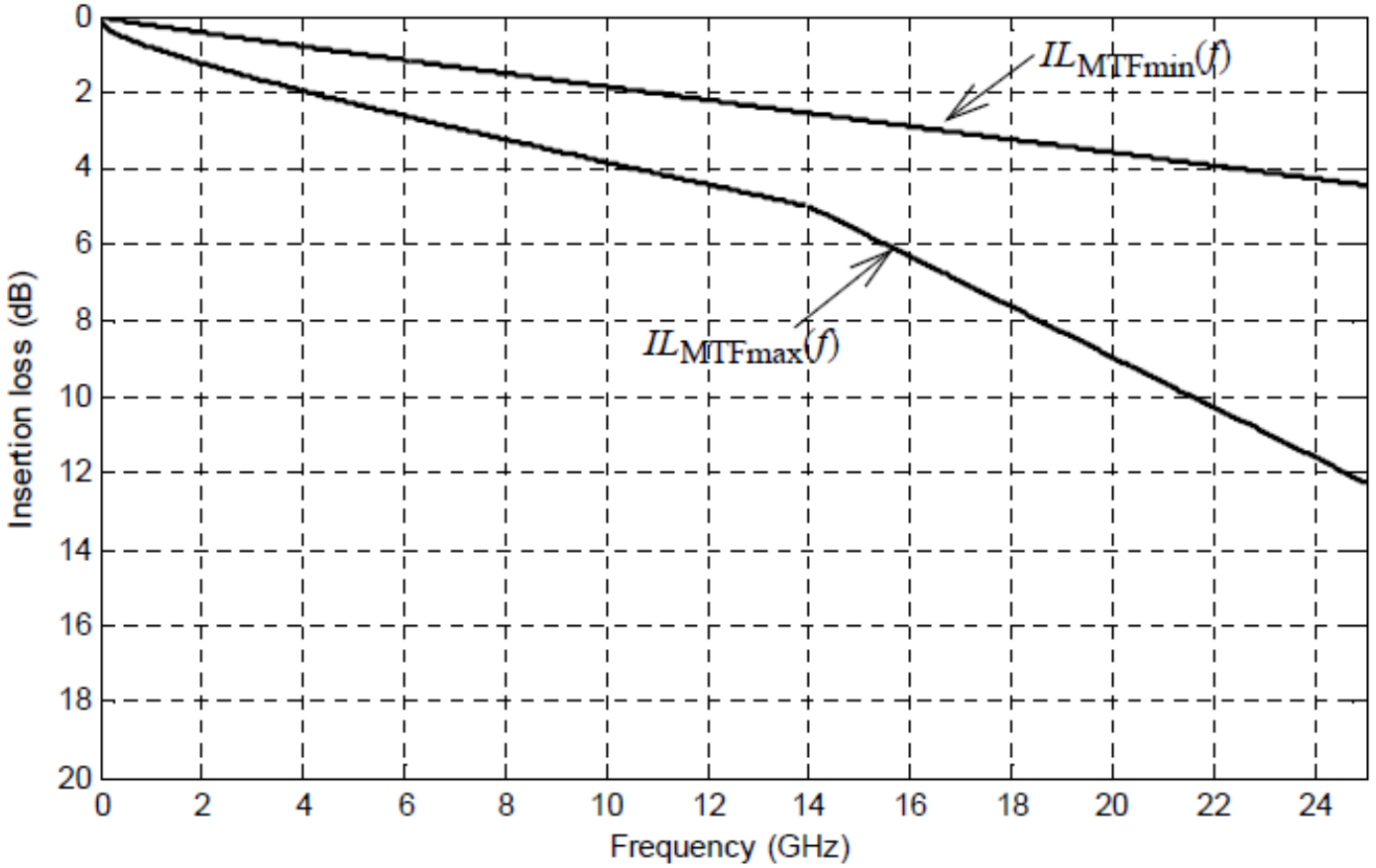
- Same as Annex 83E (CAUI-4 c2m)

CDAUI-8 c2m Tx Common-Mode to Differential & Rx Differential to Common-Mode Return Loss Specs



- Same as Annex 83E (CAUI-4 c2m)

Compliance Boards

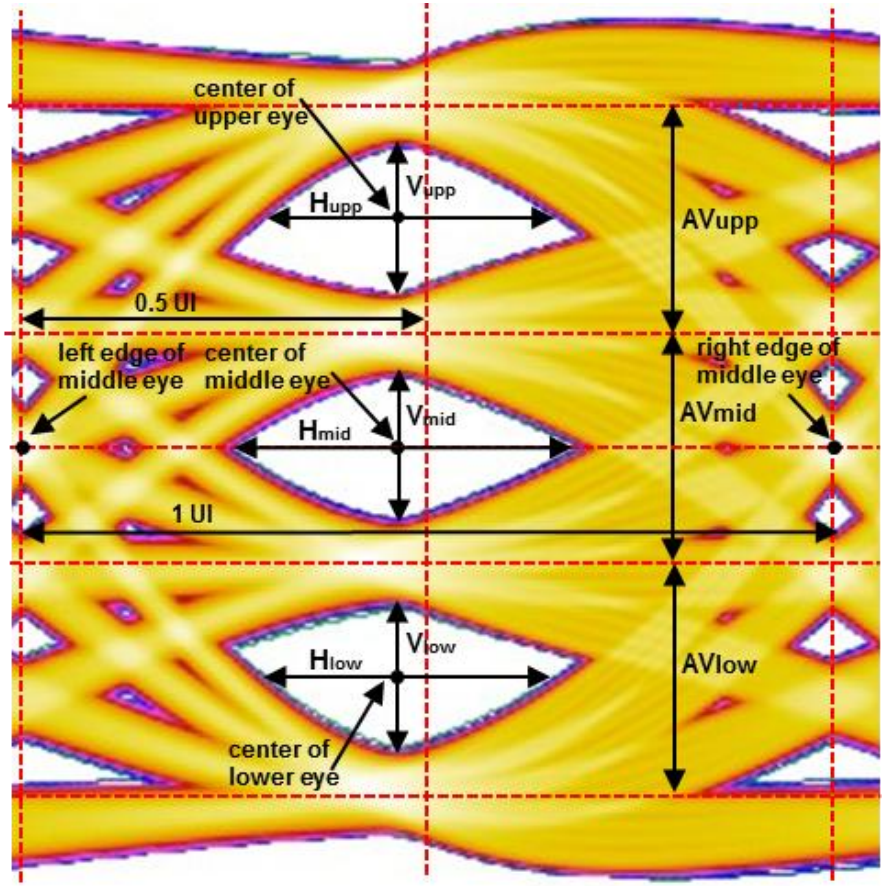


- Same as CR4 (Cl. 92)
  - No new compliance boards required

CDAUI-8 c2m Test Patterns

- CDAUI-8 PMA can reuse test patterns defined in clause 94.2.9 including:
  - JP03A test pattern
  - JP03B test pattern
  - Quaternary PRBS13 test pattern (if the termination block (i.e., 94.2.2.4) is removed, this will need to be changed accordingly)
  - Transmitter linearity test pattern

CDAUI-8 c2m PAM4 Jitter and Eye Height Parameters



See Appendix for measurement procedure

Module Stressed Receiver Test

- Same test configuration as Annex 83E
  - Modified for PAM4 testing consistent with 56G-VSR-PAM4

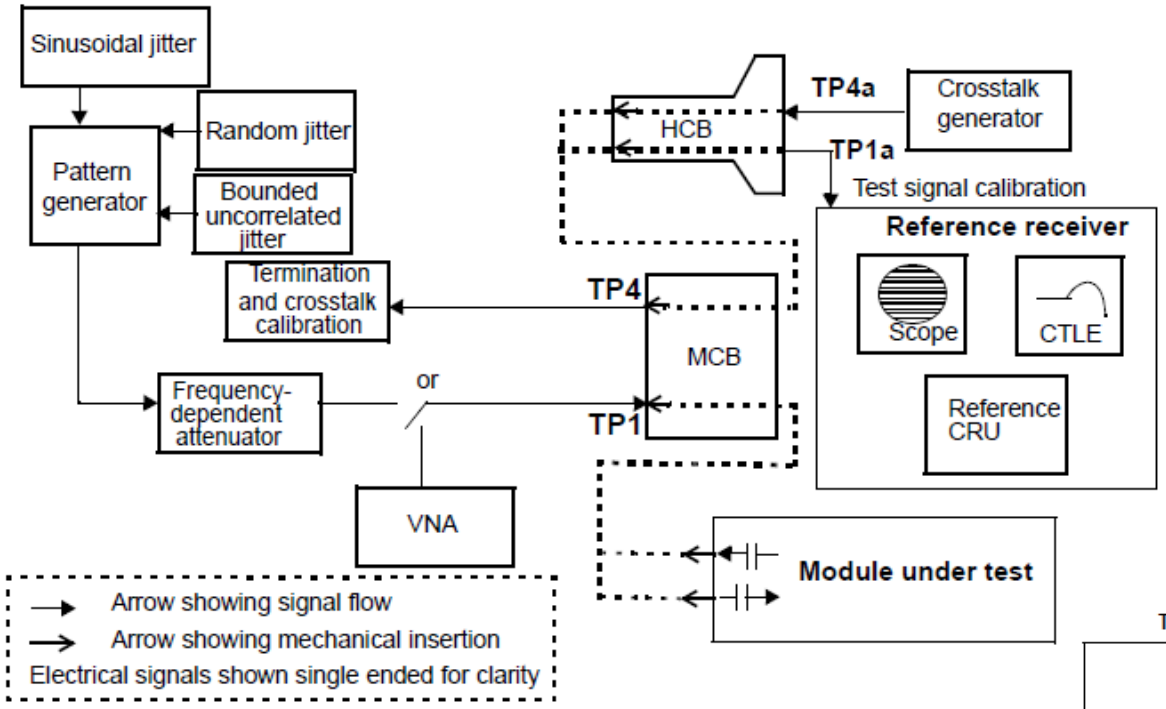


Figure 83E–15—Example module stressed input test

Table 15-7. Sinusoidal jitter frequency for TP4 and TP1 testing

Frequency Range (Hz)	Sinusoidal jitter, Peak to peak (UI)
f<fb/849600	*Not Specified*
fb/849600 < f ≤ fb/8496	*5*fb/(849600*f)*
fb/8496 < f ≤ 10xLB	*0.05*
NOTES:LB = Receiver Loop Bandwidth	

Host Stressed Receiver Test

- Same test configuration as Annex 83E
  - Modified for PAM4 testing consistent with 56G-VSR-PAM4

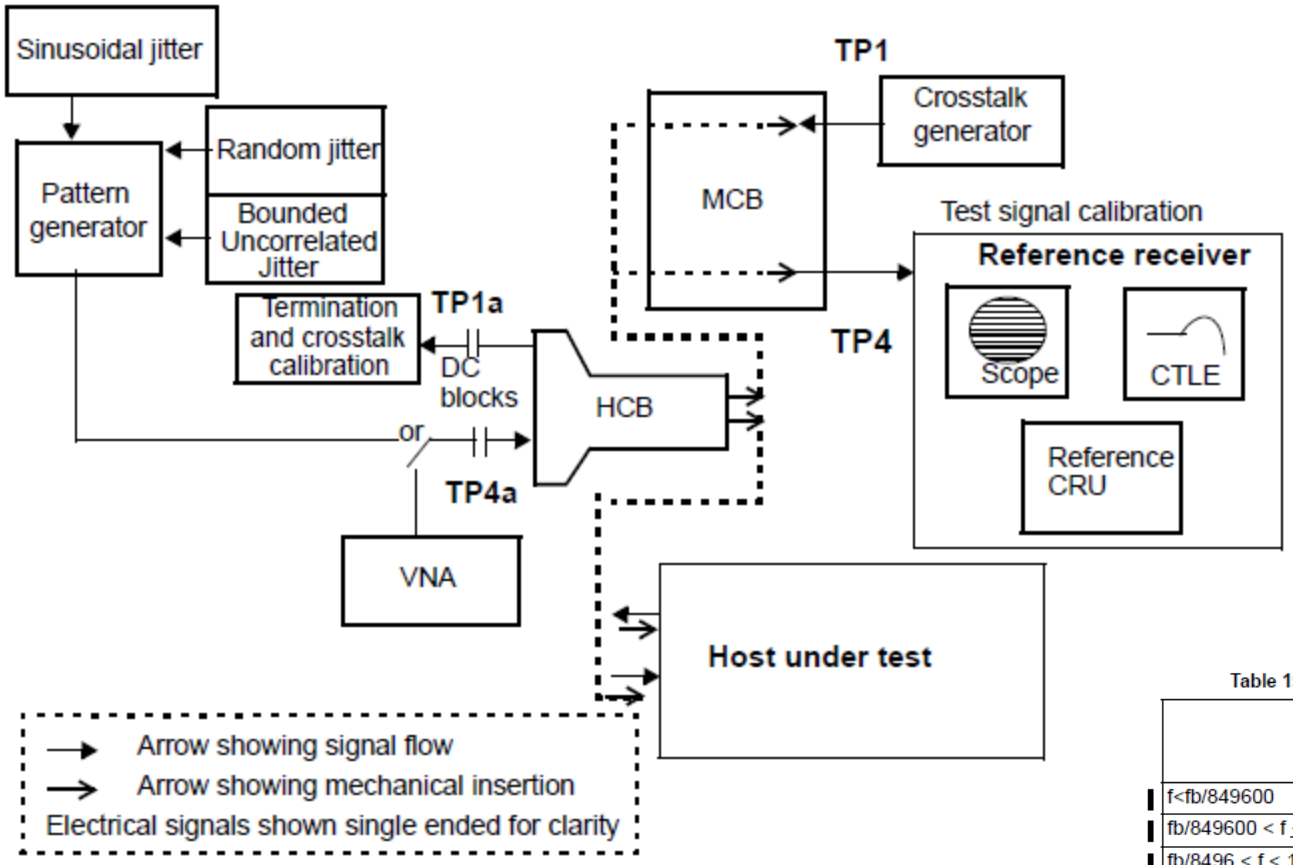


Figure 83E–14—Example host stressed input test

Table 15-7. Sinusoidal jitter frequency for TP4 and TP1 testing

Frequency Range (Hz)	Sinusoidal jitter, Peak to peak (UI)
f<fb/849600	*Not Specified*
fb/849600 < f ≤ fb/8496	*5*fb/(849600*f)*
fb/8496 < f ≤ 10xLB	*0.05*
NOTES:LB = Receiver Loop Bandwidth	

Host / Module Output Waveform Test

- Same test configuration as Annex 83E
  - Modified for PAM4 testing consistent with 56G-VSR-PAM4

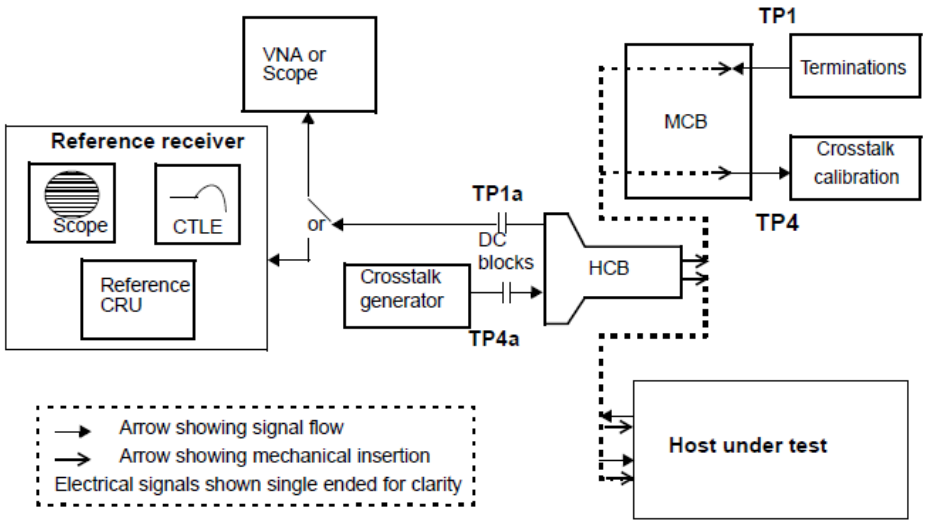


Figure 83E–9—Example host output test configuration

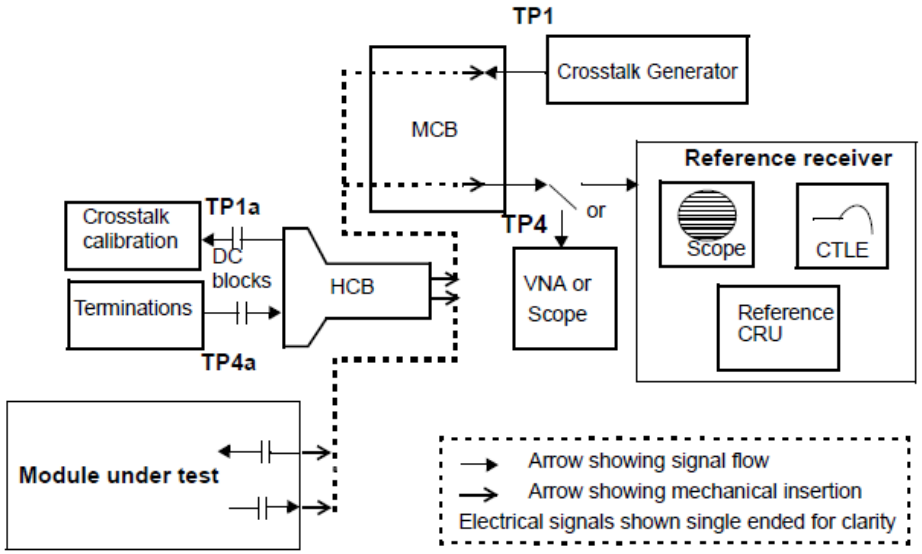


Figure 83E–11—Example module output test configuration

Summary

- Baseline proposal using PAM4 signaling for a CDAUI-8 c2m electrical interface specification:
  - Supports CAUI-4 c2m channel
  - Reuses test infrastructures and setup in Annex 83E
  - Is consistent with CEI-56G-VSR adopted baseline specification
    - Straightforward to extend/modify Annex 83E specification for PAM4 signaling

*

References

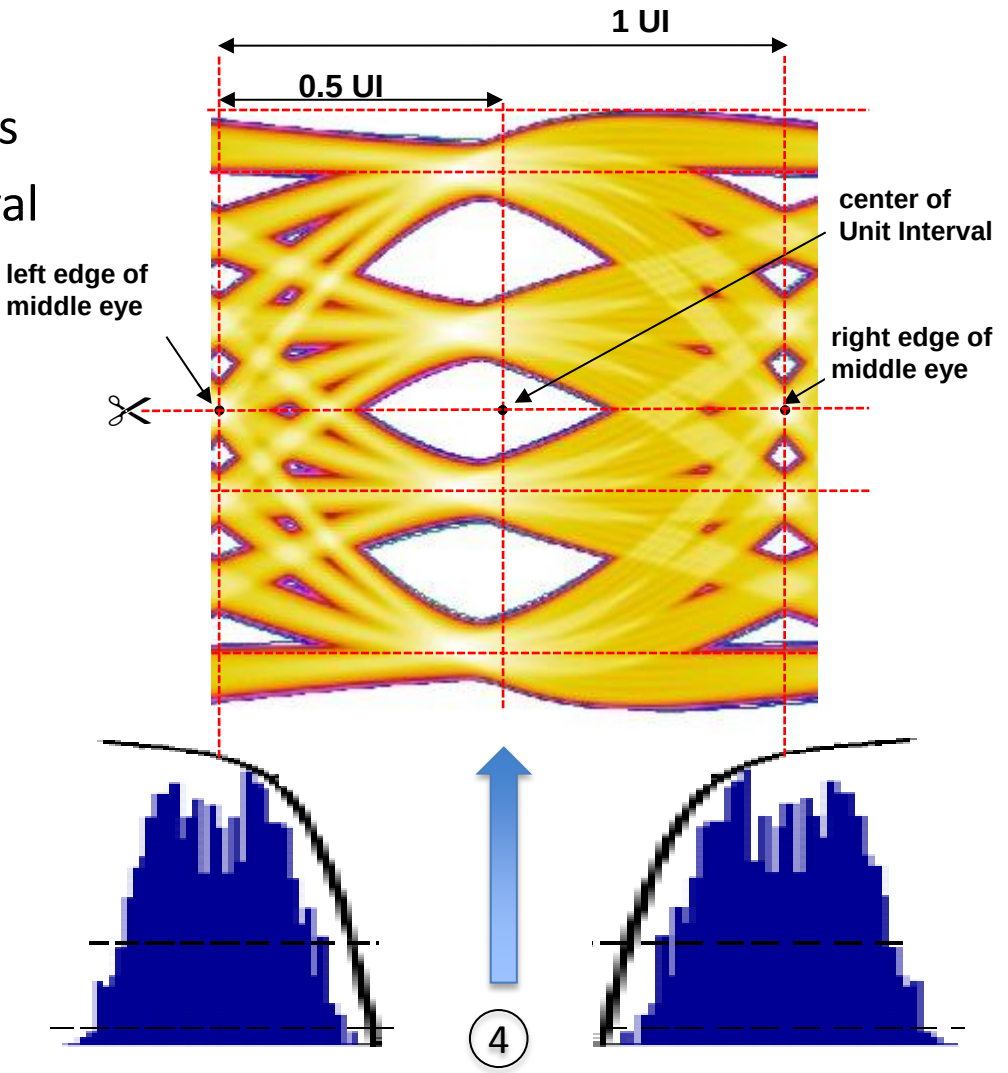
[1] oif.2014.230.01, www.oiforum.com

(This document has been made available to IEEE 802.3 by OIF via liaison)

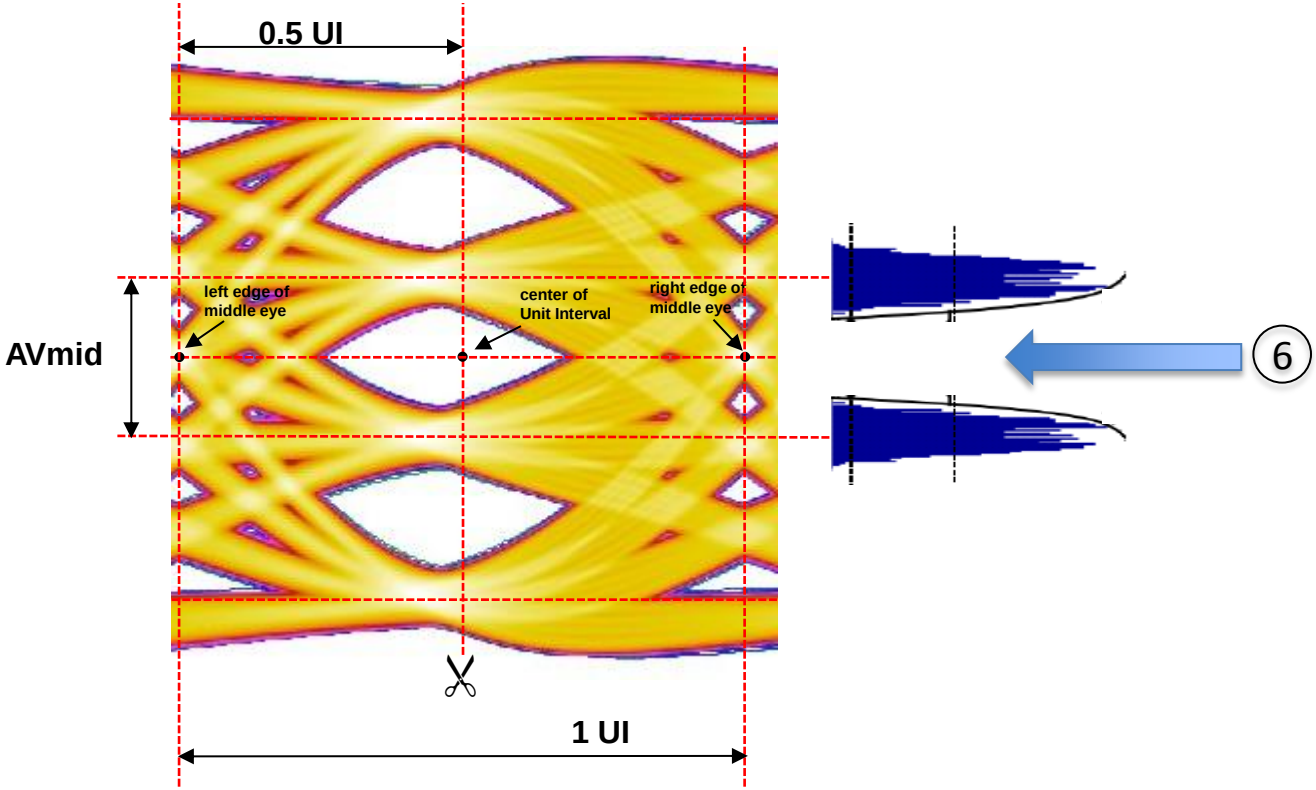
Appendix

Extracting PAM4 Eye Width and Height

- Reuse Annex 83E.4.2 method to:
  1. Capture QPRBS13 pattern (> 4 million symbols)
  2. Apply reference CTLE
  3. Construct CDFs of eye edges
  4. Locate center of Unit Interval

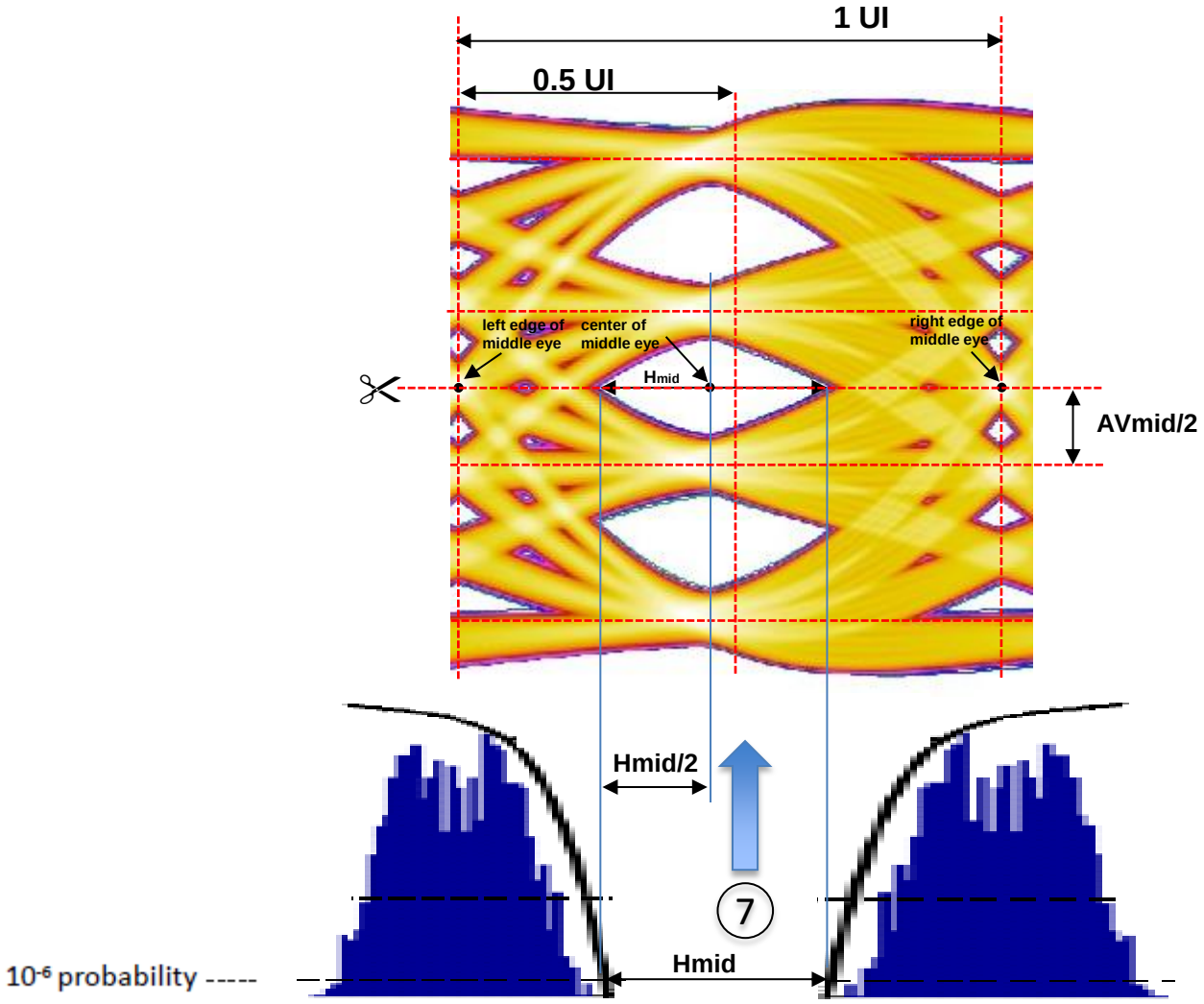


- Reuse Annex 83E.4.2 method to:
  5. Construct CDFs of signal voltages of middle eye at ½ UI
  6. Find mean amplitude of middle eye, AVmid, at ½ UI

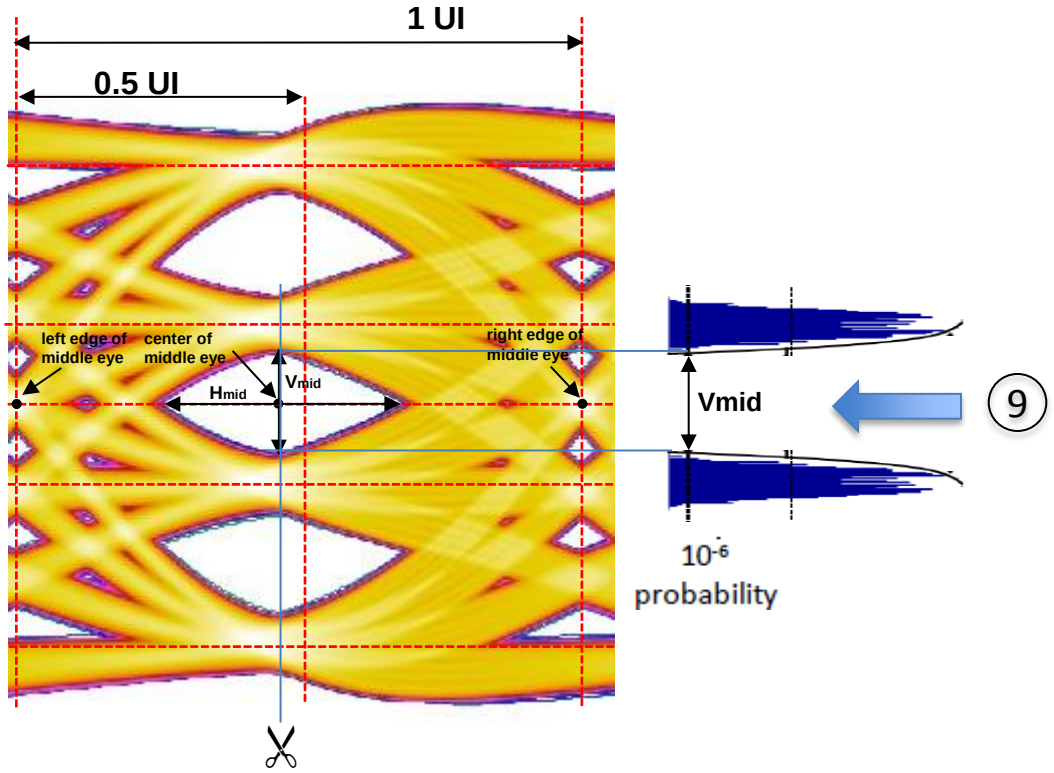


- Extract middle eye width (per A83E.4.2)

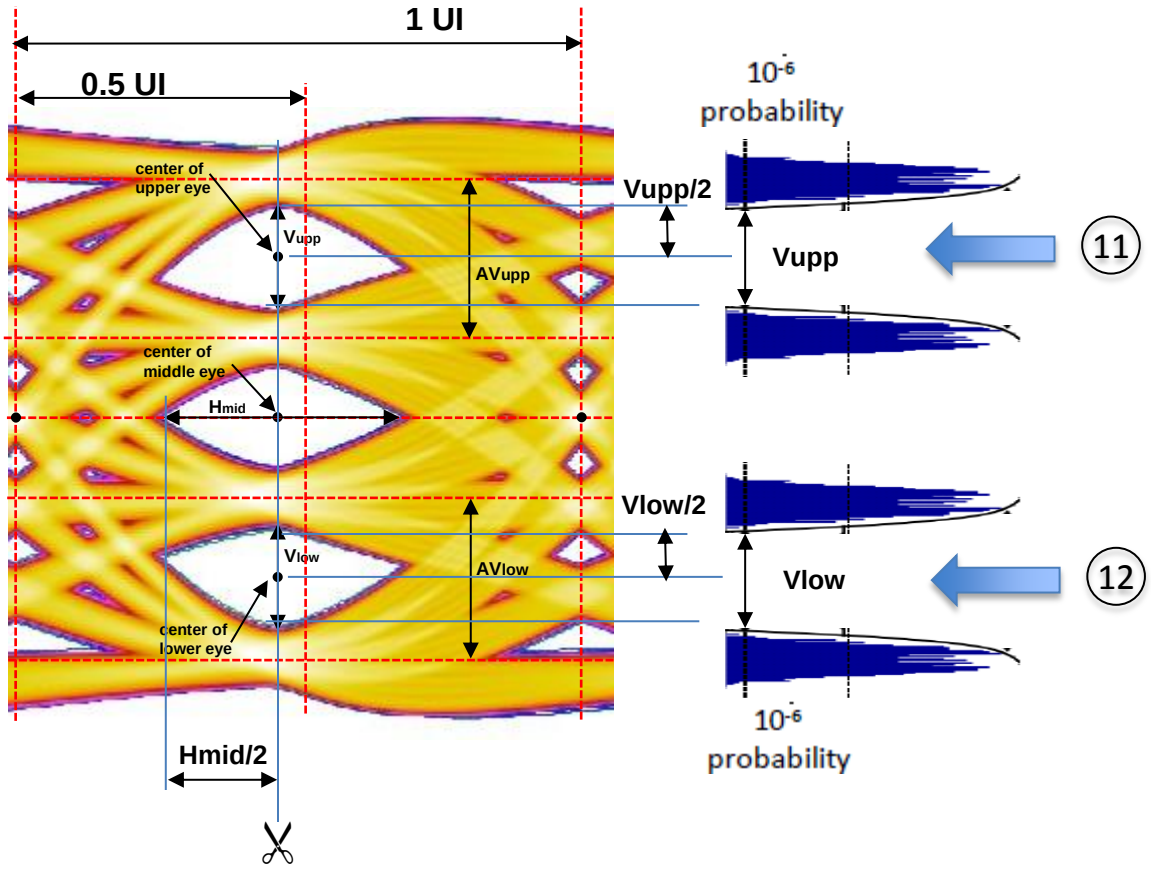
7. Hmid = 1e-6 inner eye width sliced at center of mean eye height



- Extract middle eye height (per A83E.4.2)
  8. Construct new CDFs of signal voltages of middle eye at Hmid/2
  9. Vmid = 1e-6 inner height of middle eye at Hmid/2



- Extract upper and lower eye heights
  10. Construct CDFs of signal voltages of upper and lower eyes at Hmid/2
  11. Vup = 1e-6 inner height of upper eye at Hmid/2
  12. Vlow = 1e-6 inner height of lower eye at Hmid/2



- Extract upper and lower eye widths
  13. Hupp = 1e-6 inner width of upper eye sliced at Vupp/2
  14. Hlow = 1e-6 inner width of lower eye sliced at Vlow/2