

Baseline Proposal for CDAUI-8 Chip-to-Chip (c2c)

For IEEE 802.3bs

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Purposes

- Present a baseline specification proposal for CDAUI-8 c2c electrical interface in support the 400 GbE to fulfill its objective of:

Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications

Technology Choice Highlights 1

- Channel target/requirement based on that of “informative insertion loss budget” from the electrical interface ad hoc
 - PAM-4 signaling and system is intended to work over existing CAUI-4 c2m and c2c infrastructures
- Channel equalization based on a transceiver having TX FIR, RX CTLE and DFE

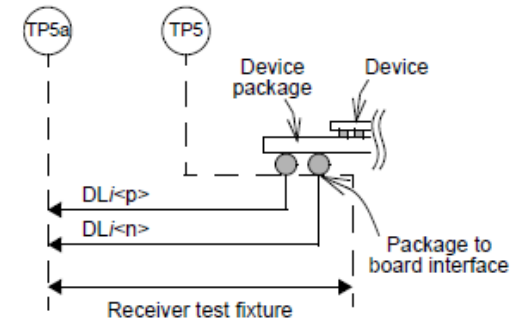
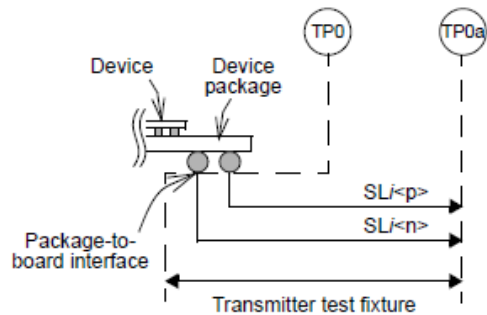
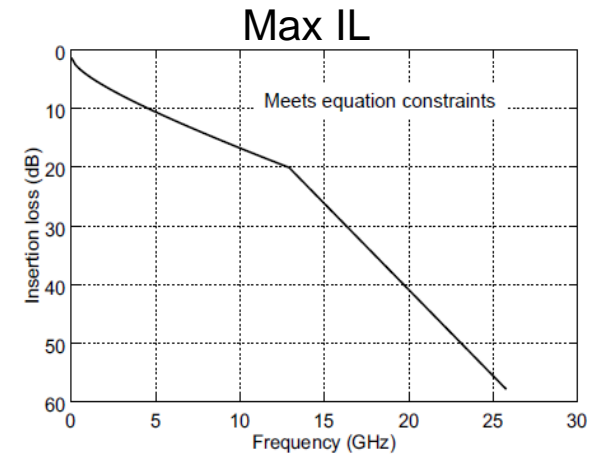
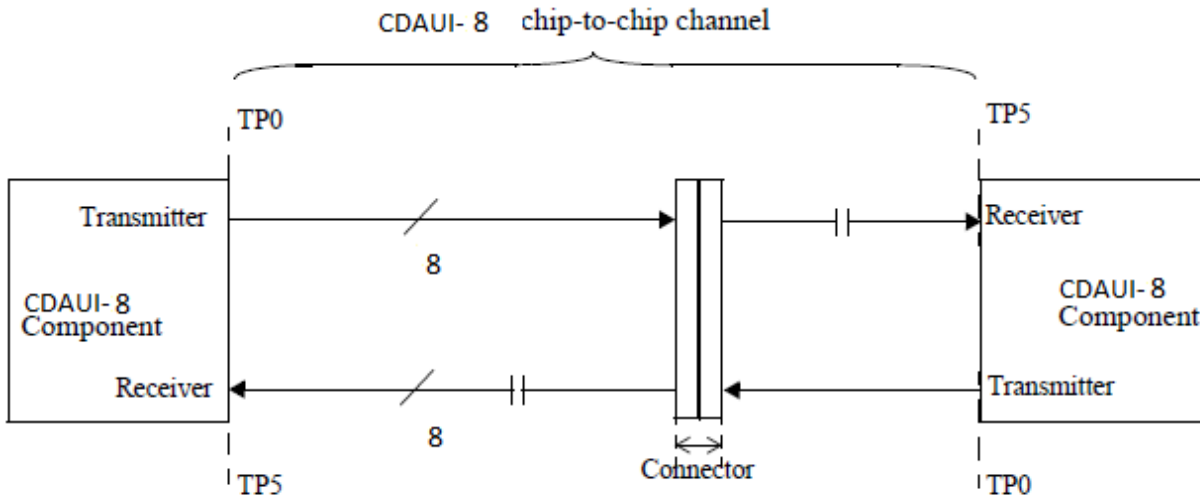
Technology Choice Highlights 2

- Raw BER of CDAUI-8 link to be $< 1E-6$; FEC brings link system BER to $< 1E-15$

Technology Choice Highlights 3

- Leverage the 100GBASE-KP4 (i.e., KP4) specification from 13.59 GBd to 25.78 - 28 GBd, and is consistent with CEI-56G-MR specification^[1]
 - Final GBd value depend on the final FEC choice
- Gray-code specified, FEC (capable of bringing raw BER from $1e-6$ to $< 1e-15$) assumed, but not specified, pre-coding TBD
- Reuse KP4 test patterns, TX and RX methodologies for specifying electrical characteristics and corresponding tests
- Reuse CAUI-4 TX and RX diff and CM RLs, compliance point definitions (i.e., TP0a and TP5a)
- Reuse 802.3bj COM method channel compliance with PAM-4 signaling

CDAUI-8 c2c Link Topology and IL Target



- CDAUI-8 c2c compliance point definition is the same as those defined in clause 83D.2 (CAUI-4)

CDAUI-8 c2c Functional Spec

- CDAUI-8 PMA functional spec will be largely reused, extended/modified from Clauses 94.2.2 (TX), 94.2.3 (RX), including
 - FEC interface
 - Pending on the final choice, with an intent of reducing the overhead to optimize it
 - Gray mapping
 - PAM4 encoding
 - Precoding (TBD)

CDAUI-8 c2c Test Patterns

- CDAUI-8 PMA will reuse test patterns defined in clause 94.2.9, including:
 - JP03A test pattern
 - JP03B test pattern
 - Quaternary PRBS13 test pattern (if the termination block (i.e., 94.2.2.4) is removed, this will need to be changed accordingly)
 - Transmitter linearity test pattern

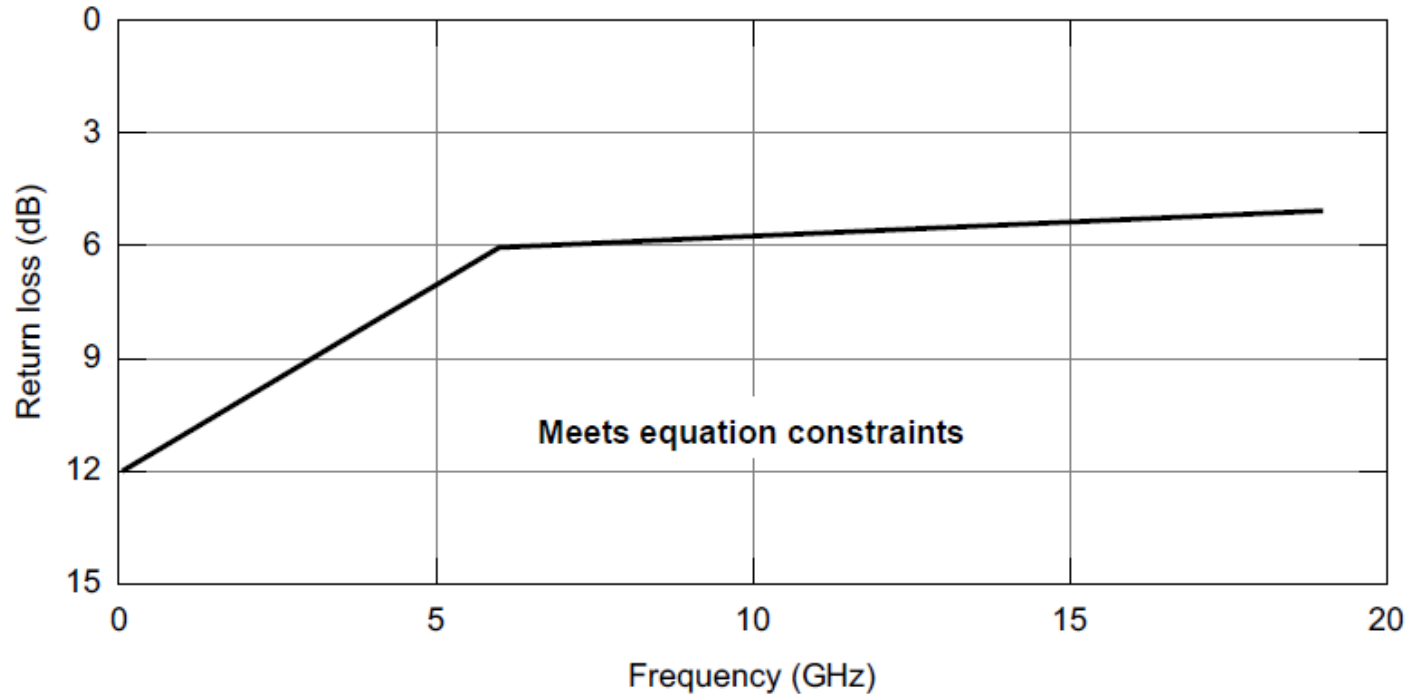
CDAUI-8 c2c TX Spec

Parameter	Subclause reference	Value	Units
Signaling rate		25.78 - 28	Gsym/s
Differential peak-to-peak output voltage (max.) Transmitter disabled Transmitter enabled		30 1200	mV mV
DC common-mode output voltage (max.)		1.9	V
DC common-mode output voltage (min.)		0	V
AC common-mode output voltage (RMS, max.)		30	mV
Differential output return loss (min.)		Slide 11	dB
Common-mode output return loss (min.)		Slide 12	dB
Output waveform Level separation mismatch ratio, R_{LM} (min.) Steady-state voltage V_{avg} (max.) Steady-state voltage V_{avg} (min.) Linear fit pulse peak (min.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)		0.92 0.6 0.4 $0.85 \times V_{\text{avg}}$ 0.0083 0.05 1.54 4	— V V V — — — —
Output jitter and linearity Clock random jitter, RMS (max.) Clock deterministic jitter, peak-to-peak (max.) Even-odd jitter (max.) Signal-to-noise-and-distortion ratio		0.005 0.05 0.019 31	UI UI UI dB

- TX output waveform definition and test method will reuse clause 94.3.12.5
- TX output jitter definition and test method will reuse clause 94.3.12.6
- TX output noise and distortion definition and test method will reuse clause 94.3.12.7

CDAUI-8 c2c TX Diff RL Spec

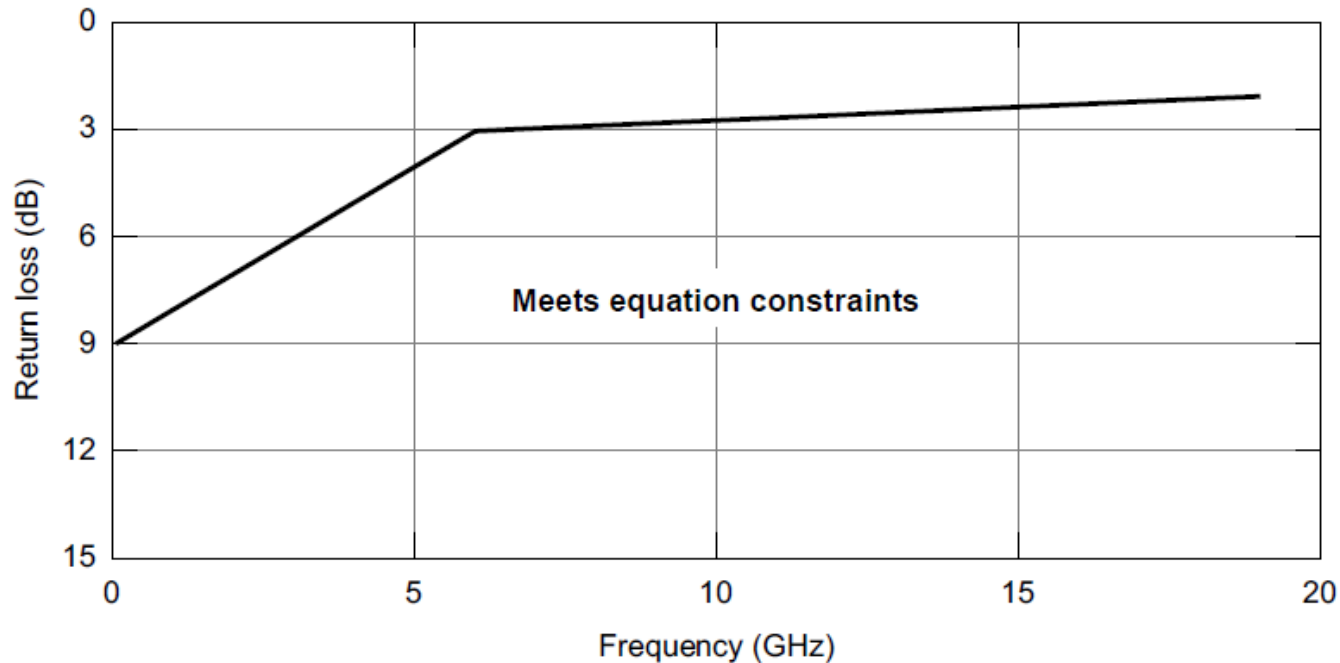
$$RL_d(f) \geq \left\{ \begin{array}{ll} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{array} \right\} \text{ dB}$$



- Reuse Eq. (93-3) and Fig (93-7)

CDAUI-8 c2c TX CM RL Spec

$$RL_{cm}(f) \geq \left\{ \begin{array}{ll} 9.05 - f & 0.05 \leq f \leq 6 \\ 3.5 - 0.075f & 6 < f \leq 19 \end{array} \right\} \text{ dB}$$



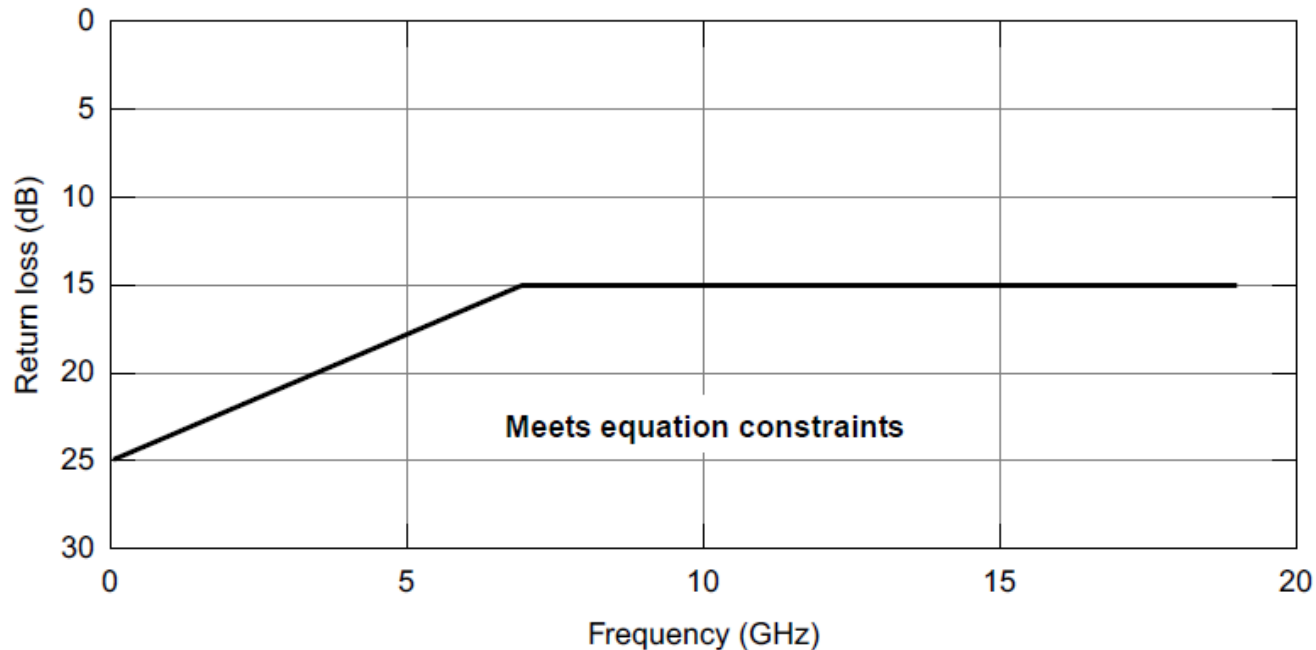
- Reuse Eq. (93-4) and Fig (93-8)

CDAUI-8 c2c RX Spec

Parameter	Symbol	Value	Units	Conditions
Differential Input Return Loss		Slide 11	dB	
Differential to Common-Mode Return Loss		Slide 14	dB	
Interference Tolerance		Slide 15	-	
Jitter Tolerance		Slide 16	-	

CDAUI-8 c2c RX D2C RL Spec

$$RL_{cd}(f) = \left\{ \begin{array}{ll} 25 - 1.44f & 0.05 \leq f \leq 6.95 \\ 15 & 6.95 < f \leq 19 \end{array} \right\} \text{ dB}$$



- Reuse Eq. (93-5) and Fig (93-11)

CDAUI-8 c2c RX Interference Tolerance Parameters

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
Bit Error Ratio (BER) ¹		10 ⁻⁸		10 ⁻⁸	
COM ² IL at Nyquist		3 10		3 20	dB dB
a ₀ ³	-1	1.5	-1	2	dB
a ₁	0	9.533	0	14.914	dB/√GHz
a ₂	0	30.855	0	41.228	dB/GHz
a ₄	0	14.162	0	19.728	dB/GHz ²
RSS_DFE4	0.05	—	0.05	—	—

NOTES:

1. Measured between Tx and RX package balls.
2. Test channel parameters: COM, including effects of BB noise, Insertion loss at Nyquist
3. Coefficients are determined from insertion loss measured between TX and RX package balls with f_{\min} of 0.05 GHz, f_{\max} of $f_b/2$, and maximum Δf of 0.01 GHz.

- Largely re-use of the method in 94.3.13.3

CDAUI-8 c2c RX Jitter Tolerance Parameters

Parameter	Case A values	Case B values	Units
Max Pre-FEC BER	1e-6	1e-6	
Jitter frequency	$fb/849600$	$fb/8496$	same as fb
Jitter Amplitude	5	0.05	UI

- Largely re-use method in 94.3.13.4
- fb is the BAUD rate

CDAUI-8 c2c Channel Spec: COM (I)

Parameter	Symbol	Value	Units
Signaling rate	f_s	25.78-28	GBd
Maximum start frequency	f_{max}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model			
Single-ended device capacitance	C_{**}	2.5×10^{-4}	nF
Transmission line length, Test 1	Z_{**}	12	mm
Transmission line length, Test 2	Z_{**}	30	mm
Single-ended package capacitance at package-to-board interface	C_{**}	1.8×10^{-4}	nF
Single-ended reference resistance	R_{**}	50	Ω
Single-ended termination resistance	R_{**}	55	Ω
Receiver 3 dB bandwidth	f_b	$0.75 \times f_s$	
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.62	—
Transmitter equalizer, pre-cursor coefficient	$c(-1)$		
Minimum value		-0.18	—
Maximum value		0	—
Step size		0.02	—
Transmitter equalizer, post-cursor coefficient	$c(1)$		
Minimum value		-0.38	—
Maximum value		0	—
Step size		0.02	—
Continuous time filter, DC gain	g_{***}		
Minimum value		-15	dB
Maximum value		0	dB
Step size		1	dB
Continuous time filter, zero frequency	f_{z**}	$f_{max}/4$	GHz
Continuous time filter, pole frequencies	f_{p***} f_{p***}	$f_{max}/4$ f_s	GHz
Transmitter differential peak output voltage			
Victim	A_{**}	0.4	V
Far-end aggressor	A_{***}	0.4	V
Near-end aggressor	A_{***}	0.6	V

CDAUI-8 c2c Channel Spec: COM (II)

Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.92	—
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	10	UI
Normalized DFE coefficient magnitude limit for $n = 1$ for $n = 2$ to N_b	$d_{max}(n)$	1 0.2	—
Random jitter, RMS	σ_{RJ}	0.005	UI
Dual-Dirac jitter, peak	A_{DD}	0.025	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V ² /GHz
Target detector error ratio	DER_0	10^{-6}	—

Summary

- A baseline proposal based PAM-4 signaling for CDAUI-8 c2c electrical interface specification has been developed
 - Intent is to support existing CAUI-4 c2c channel and testing infrastructures
 - Reuse/extended/modified from 100GBase-KP4 and CAUI-4 c2c specifications (i.e., clauses 94, 93A, and 83D)
 - Consistent with CEI-56G-MR adopted baseline specification

References

[1] oif2014.245.00, www.oiforum.com

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