Draft Baseline Proposal for CDAUI-8 Chip-to-Module (C2M) Electrical Interface (NRZ)

Authors:

Tom Palkert: MoSys

Jeff Trombley, Haoli Qian: Credo

Date: Dec. 4 2014

Presented: IEEE 802.3bs electrical interface ad hoc

References: IEEE 802.3bm, OIF-CEI-56G-VSR-NRZ

Purpose:

Present a baseline specification proposal for CDAUI-8 C2M electrical interface in support the 802.3bs to fulfill its objective of:

Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications

Table Of Contents

Table of Figures

Tables

Annex 99E

Chip-to-module 400 Gb/s eight-lane Attachment Unit Interface (CDAUI-8)

99E.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 400 Gb/s eight-lane Attachment Unit Interface (CDAUI-8). Figure 99E–1 shows the relationship of the CDAUI-8 chip-to-module interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-module interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with pluggable module interfaces.

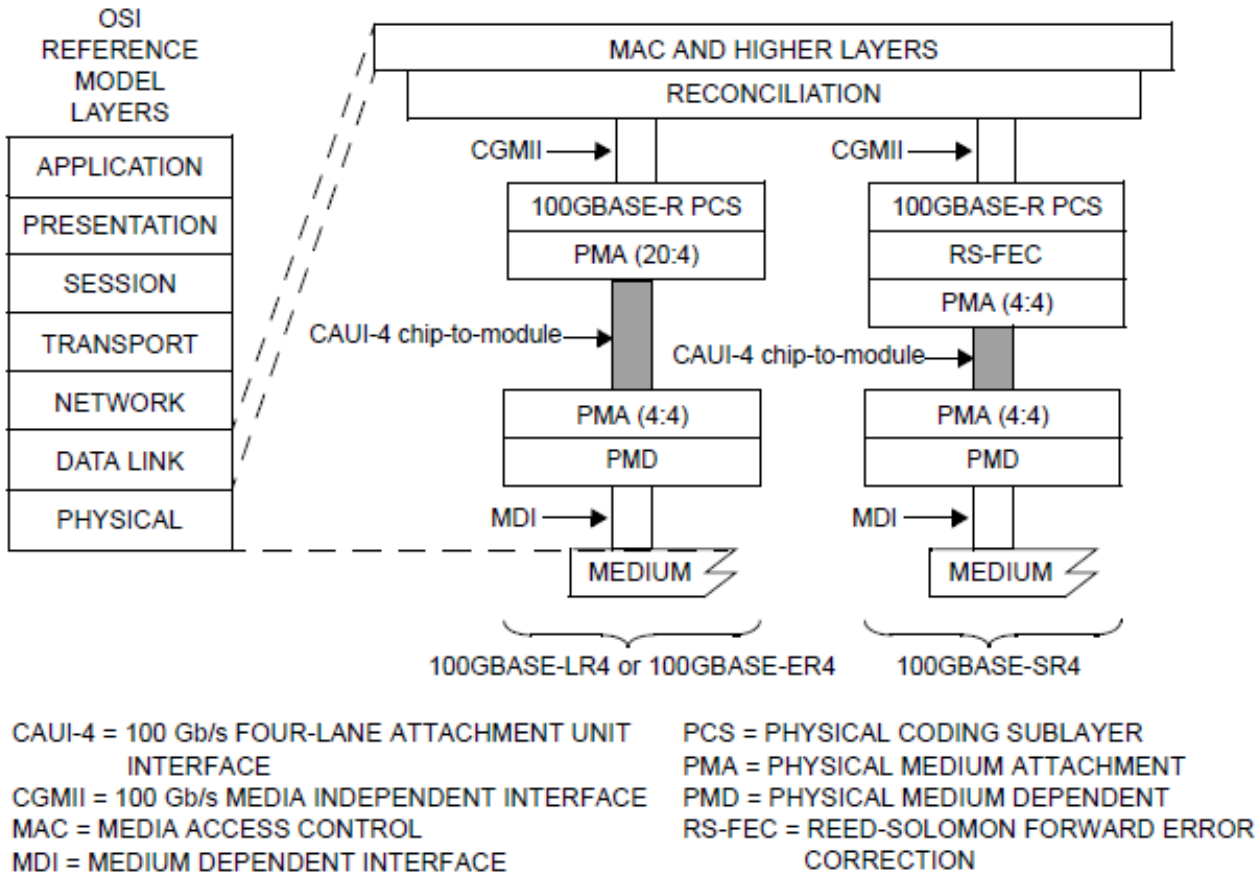

Figure 1 Example CDAUI-8 Chip to module relationship to the ISO/IEC Opent System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model:

The CDAUI-8 link is described in terms of a host CDAUI-8 component, a CDAUI-8 channel with associated insertion loss, and a module CDAUI-8 component. Figure 99E–2 and Equation (99E–1) depict a typical CDAUI-8 application,

and summarize the differential insertion loss budget associated with the chip-to-module application which is shown in Figure 99E–3. The CDAUI-8 chip-to-module interface comprises independent data paths in each direction. Each data path contains eight differential lanes which are AC coupled within the module. The nominal signaling rate for each lane is 51.5625 GBd. The chip-to-module interface is defined using a specification and test methodology that is similar to that used for CEI-56G-VSR defined in OIF-CEI Common Electrical Interface.

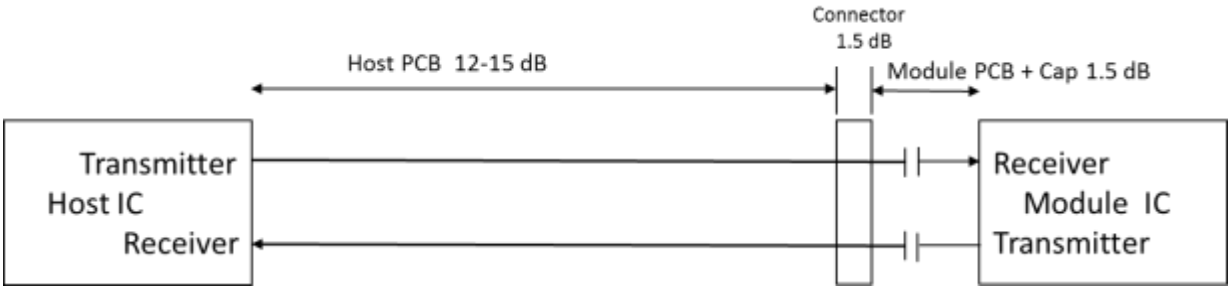

Figure 2: Chip to Module insertion loss budget at 25 GHz

$$Insertion\_loss(f) \leq 1.076\left(0.075 + 0.537\sqrt{f} + 0.566f\right) \qquad 0.01 \leq f < 56 \quad (dB)$$

where

f is the frequency in GHz

Insertion_loss(f) is the CDAUI-8 chip-to-module insertion loss

Equation 1

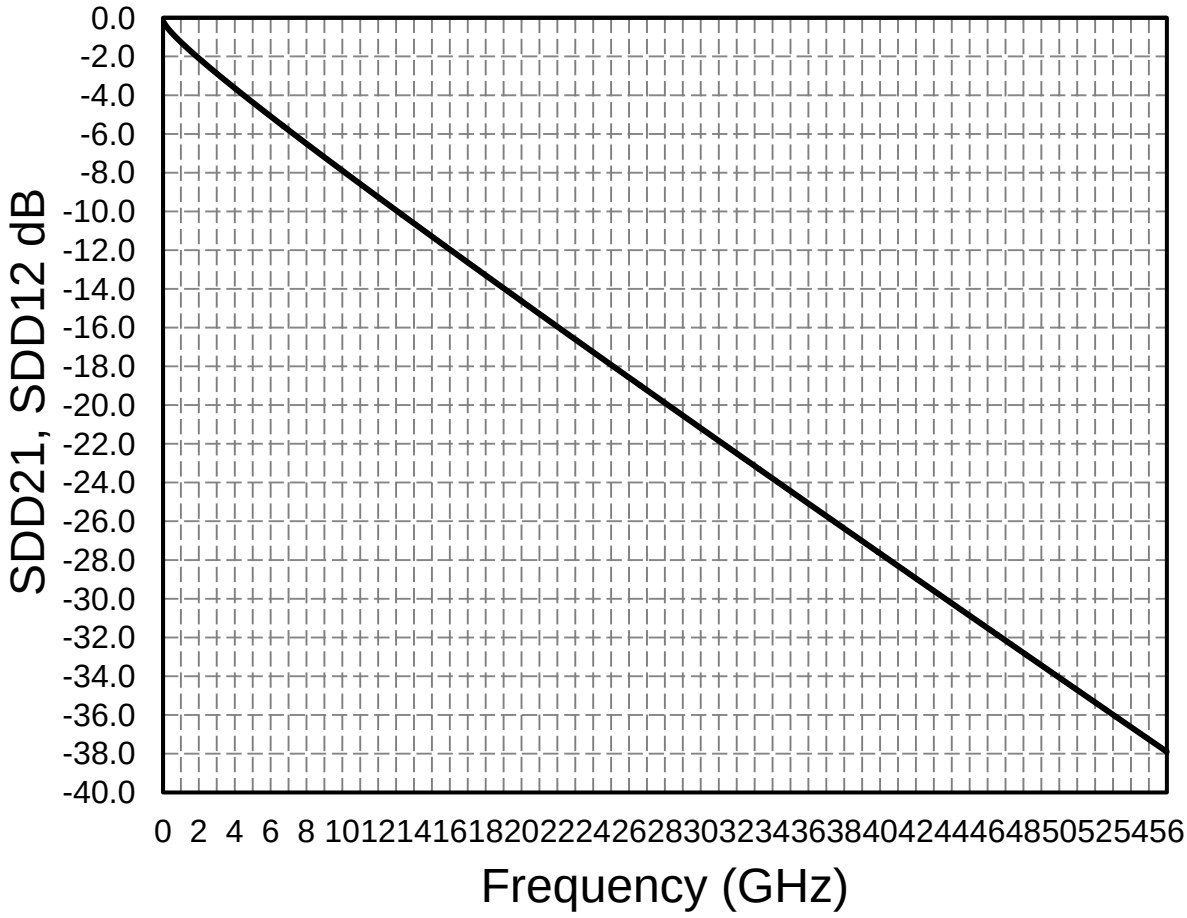

Figure 3: CDAUI-8 chip to module channel insertion loss

99E.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-6} with any errors sufficiently uncorrelated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding.

99E.2 CDAUI-8 chip to module compliance point definitions

The electrical characteristics for the CDAUI-8 chip-to-module interface are defined at compliance points for the host and module respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 99E–4 depicts the location of compliance points when measuring host CDAUI-8 compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at TP1a. Similarly, the input of the HCB at TP4a is used to verify the host input compliance. Figure 99E–5 depicts the location of compliance points when measuring module CDAUI-8 compliance. The output of the Module Compliance Board (MCB) is used to verify the module electrical output signal at TP4. Similarly, the input of the MCB at TP1 is used to verify the module input compliance. Additional details on the requirements for the MCB and HCB are given in 99E.4.1

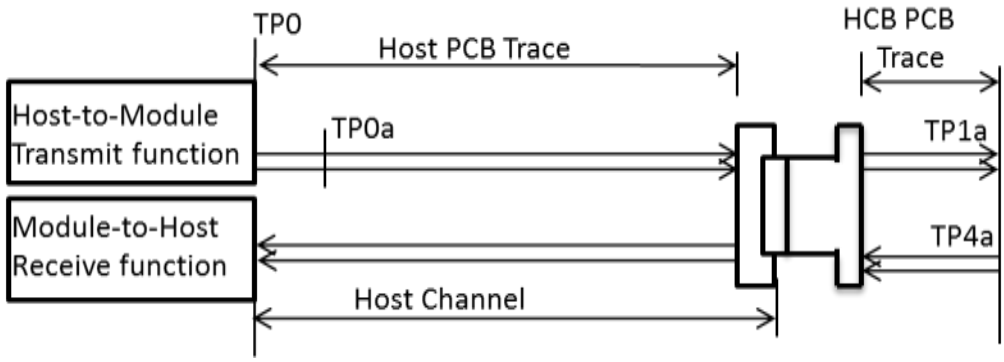

Figure 4: Host CDAUI-8 Compliance points

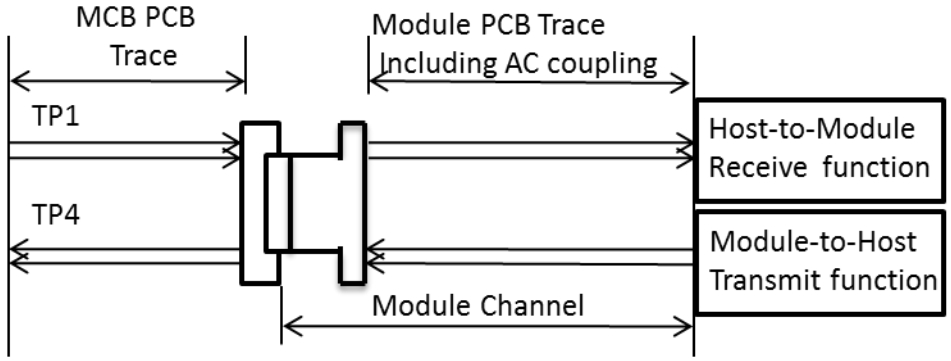

Figure 5: Module CDAUI-8 compliance points

Table 1: CDAUI-8 host output characteristics (at TP1a)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	3.1.1	51.5625 ±100ppm	GBd
DC common-mode output voltage (max)	3.1.2	2.8	V
DC common-mode output voltage (min)	3.1.2	-0.3	V
Single-ended output voltage (max)	3.1.2	3.3	V
Single-ended output voltage (min)	3.1.2	-0.4	V
AC common-mode output voltage (max, RMS)	3.1.2	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	3.1.2	 35 900	mV
Eye width (min)	3.1.6	0.46	UI
Eye height A, differential (min)	3.1.6	60	mV
Eye height B, differential (min)	3.1.6	60	mV
Differential output return loss (min)	3.1.3	Equation 2	dB
Common to differential mode conversion return loss (min)	3.1.3	Equation 3	dB
Differential termination mismatch (max)	3.1.4	10	%
Transition time (min, 20% to 80%)	3.1.5	9	ps

A test system with a fourth-order Bessel-Thomson low-pass response with 66 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

99E.3.1.1 Signaling rate and range

The CDAUI-8 signaling rate is 51.5625 GBd ± 100 ppm per lane. This translates to a nominal unit interval of 19.3939395 ps.

99E.3.1.2 Signal levels

The differential output voltage v_{di} is defined to be the difference between the single-ended output voltages, SL*i*<p> minus SL*i*<n>. The common-mode voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 6.

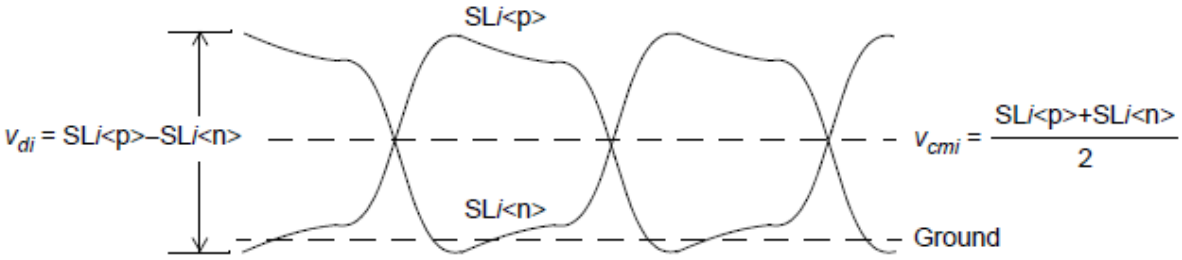

Figure 6: Voltage Definitions

The peak-to-peak differential output voltage is less than or equal to 900 mV. The peak-to-peak differential output voltage is less than or equal to 35 mV when the transmitter is disabled. The DC common-mode output voltage and AC common-mode output voltage are defined with respect to signal ground.

99E.3.1.3 Output return loss

The differential output return loss, in dB, of the output is shown in Equation (99E–2) and illustrated in Figure 99E–7. This output requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 ohms.

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \quad \text{(dB)}$$

where

f is the frequency in GHz

RLd is the CAUI-4 chip-to-module host output differential return loss

Equation 2

Note: Values to be adjusted after compliance board design complete

$$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \quad \text{(dB)} \qquad \text{(83E–3)}$$

where

f	is the frequency in GHz
$RLdc$	is the CAUI-4 chip-to-module output common to differential mode conversion return loss

Note: Values to be adjusted after compliance board design complete

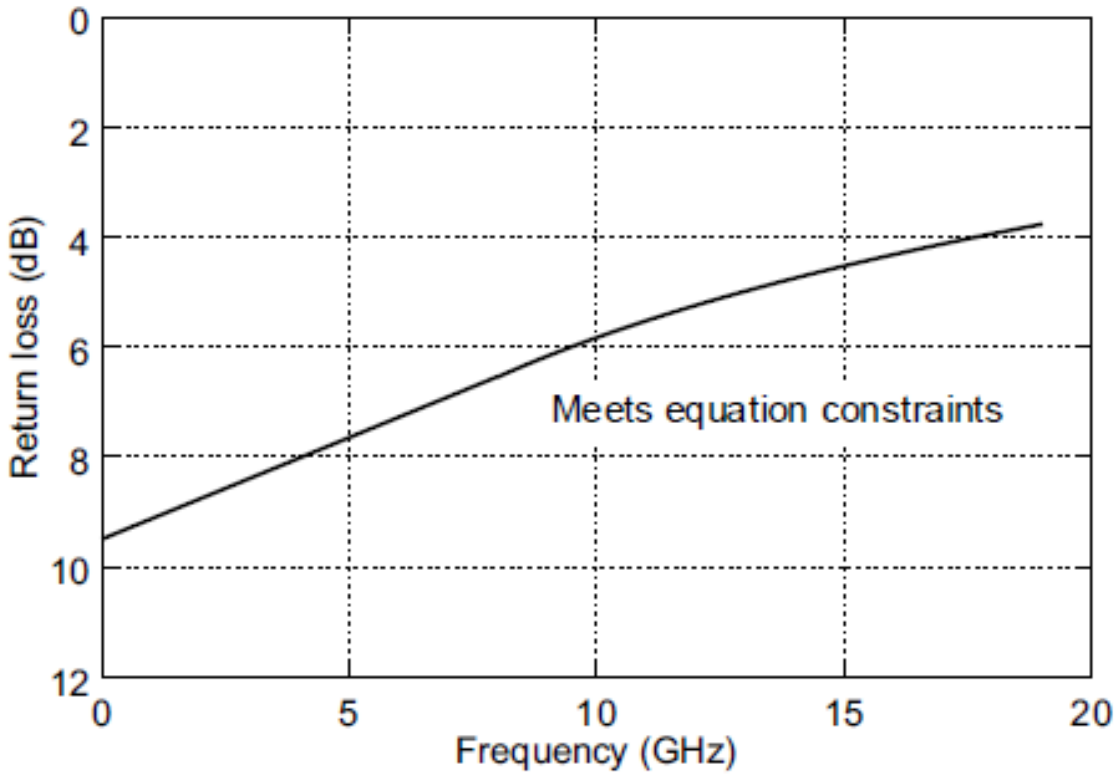

Figure 7: Output differential return loss

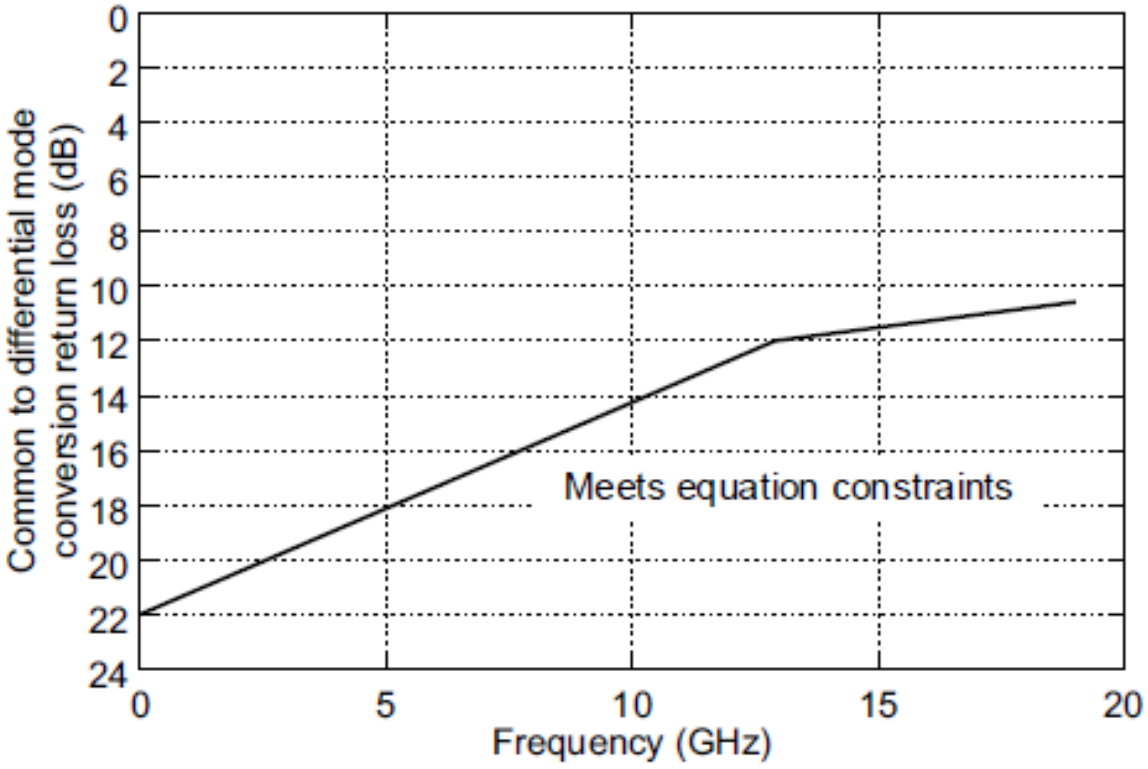

Figure 8: Output common to differential mode conversion return loss

99E.3.1.4 Differential termination mismatch

Differential termination mismatch is defined in 86A.5.3.2.

99E.3.1.5 Transition time

The transition times (rise and fall times) are defined in 86A.5.3.3 with the exception that the observation is through a 66 GHz low-pass filter response.

99E.3.1.6 Host output eye width and eye height

Figure 99E–9 depicts an example host output eye width and eye height test configuration. Host output eye width and eye height are measured at TP1a using compliance boards defined in 99E.2. The host output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 99E.3.1.6.1 and a Decision Feedback Equalizer (DFE). The optimum CTLE peaking value is used for host output eye measurements. Eye width and eye height measurement methodology is described in 99E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86-11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP4 with target differential peak-to-peak amplitude of 900 mV and target transition time of 9 ps.

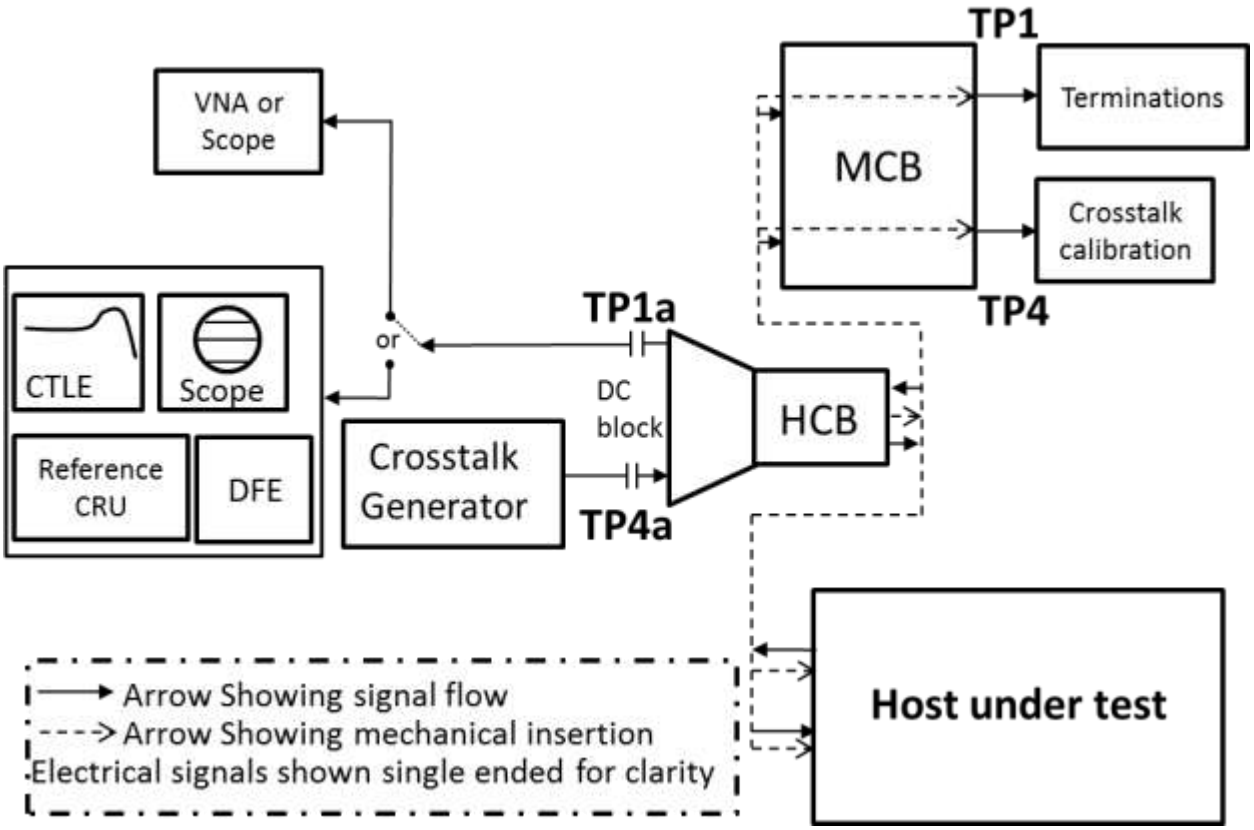

Figure 9: Example host output test configuration

99E.3.1.6.1 Reference receiver for host output eye width and eye height evaluation

The reference receiver is used to measure host eye width and eye height. The reference receiver includes a Decision Feedback Equalizer (DFE) and a selectable continuous time linear equalizer (CTLE) which is described by Equation (99E–4) with coefficients given in Table 99E–2 and illustrated in Figure 99E–10. The equalizer may be implemented in software; however the measured signal is not averaged.

$$H(f) = \frac{GP_1P_2}{Z_1} \times \frac{j2\pi f + Z_1}{(j2\pi f + P_1)(j2\pi f + P_2)}$$

where

$H(f)$	is the CTLE transfer function
G	is the CTLE gain

Equation 4

Note: Needs to be scaled to 28GHz

Table 2: Reference CTLE Coefficients

Peaking (dB)	G	P1/(GHz)	P2/(GHz)	Z1/(GHz)
1	0.891	18.6	14.1	8.31
2	0.794	18.6	14.1	7.10
3	0.708	15.6	14.1	5.68
4	0.631	15.6	14.1	4.98
5	0.562	15.6	14.1	4.35
6	0.501	15.6	14.1	3.82
7	0.447	15.6	14.1	3.43
8	0.398	15.6	14.1	3.00
9	0.335	15.6	14.1	2.67

Note: Add peaking values up to 12dB and shift frequency to 25GHz

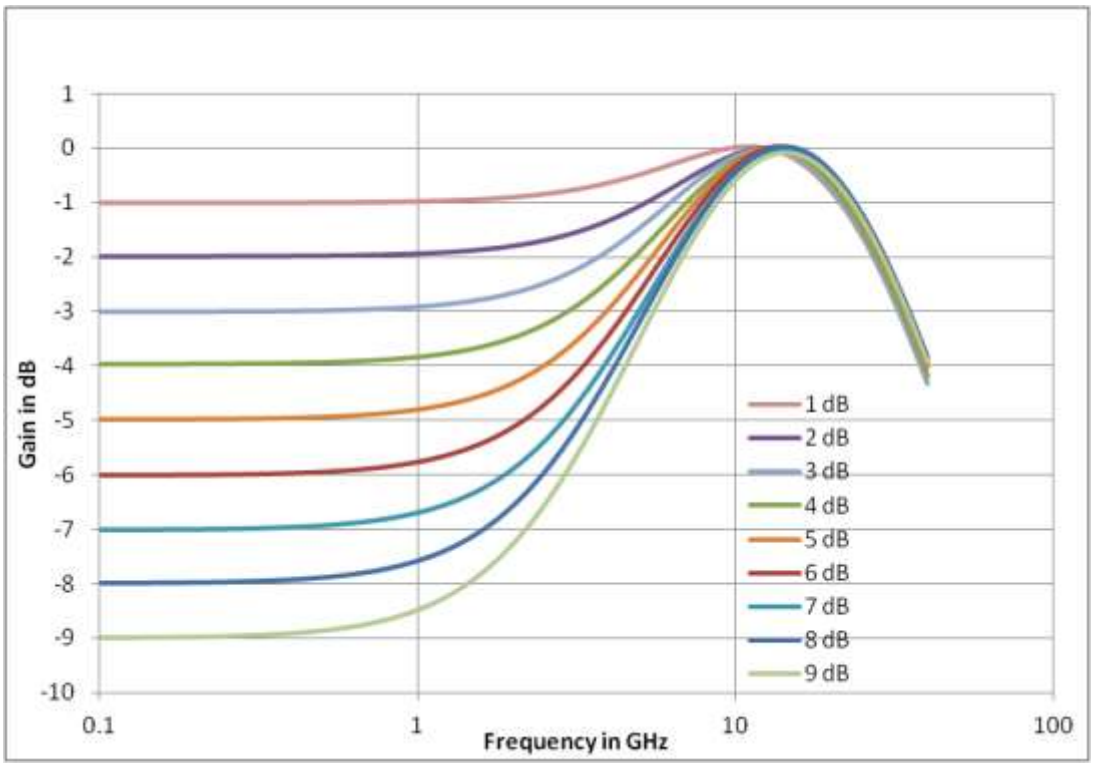

Figure 10: Selectable continuous time linear equalizer (CTLE) Characteristic

99E.3.2 CDAUI-8 module output characteristics

A CDAUI-8 module output shall meet the specifications defined in Table 99E–3 if measured at TP4. A test system with a fourth-order Bessel-Thomson low-pass response with 66 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

Table 3: CDAUI-8 module output characteristics (at TP4)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	3.1.1	51.5625 ±100ppm	GBd
AC common-mode output voltage (max, RMS)	3.1.2	17.5	mV
Differential output voltage (max)	3.1.2	900	mV
Eye width (min)	3.2.1	.57	UI
Eye height, differential (min)	3.2.1	228	mV
Vertical eye closure (max)	4.2.1	5.5	dB
Differential output return loss (min)	3.1.3	Equation 2	dB
Common to differential mode conversion return loss (min)	3.1.3	Equation 3	dB
Differential termination mismatch (max)	3.1.4	10	%
Transition time (min, 20% to 80%)	3.1.5	9	ps
DC common mode voltage (min)[a]	3.1.2	-350	mV
DC common mode voltage (max)[a]	3.1.2	2850	mV

[a]DC common mode voltage is generated by the host. Specification includes effects of ground offset

99E.3.2.1 Module output eye width and eye height

Module output eye width is greater than 0.57 UI. Module output eye height is greater than 228 mV. Figure 99E–11 depicts an example module output eye width and eye height test configuration. Module output eye width and eye height are measured at TP4 using compliance boards defined in 99E.2. The module output eye is measured using a reference receiver with a Decision Feedback Equalizer (DFE) and a continuous time linear equalizer (CTLE) defined in 99E.3.2.1.1. Eye width and eye height measurement methodology is described in 99E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86-11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP1a with target differential peak-to-peak amplitude of 900 mV and target transition time of 10 ps.

99E.3.2.1.1 Reference receiver for module output eye width and eye height evaluation

A reference receiver is used to measure module eye width and eye height. The reference receiver includes a Decision Feedback Equalizer (DFE) and a selectable continuous time linear equalizer (CTLE) which is described by Equation (99E–4) with coefficients given in the first three rows of Table 99E–2. The equalizer may be implemented in software, however the measured signal is not averaged. Any of the three equalizer settings may be used to meet the output eye width and eye height requirement.

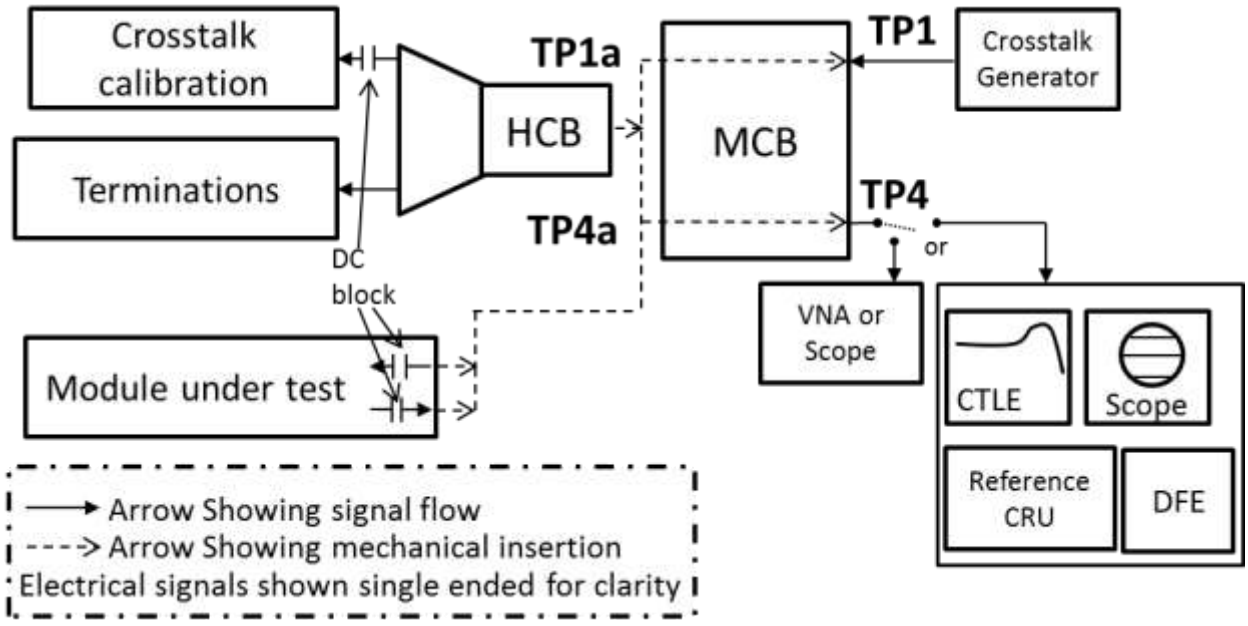

Figure 11: Example module output test configuration

99E.3.3 CDAUI-8 host input characteristics

A CDAUI-8 host input shall meet the specifications defined in Table 99E–4 if measured at the appropriate test point.

Table 4: CDAUI-8 host input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate, per lane (range)	3.1.1	TP4a	51.5625 ±100	GBd
Differential pk-pk input voltage tolerance (min)	3.1.2	TP4	900	mV
Differential input return loss (min)	3.3.1	TP4a	Equation 5	dB
Differential to common mode input return loss (min)	3.3.1	TP4a	Equation 6	dB
Host stressed input testa	3.3.2	TP4	See 99E.3.3.2	
Differential termination mismatch (max)	3.1.4	TP4a	10	%
Common-mode voltage[b] Min Max	3.1.2	TP4a	 -0.3 2.8	V

[a]Meets BER specified in E.1.1
[b]Generated by host, referred to host ground

99E.3.3.1 Input return loss

The differential input return loss, in dB, of the input is shown in Equation (99E–5) and illustrated in Figure 99E–12. The reference impedance for differential return loss measurements is 100 ohms.

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \quad \text{(dB)}$$

where

f	is the frequency in GHz
RLd	is the CAUI-4 chip-to-module input differential return loss

Equation 5: Note: Values to be adjusted after compliance board design complete

Differential to common mode input return loss, in dB, of the input is shown in Equation (99E–6) and illustrated in Figure 99E–13.

$$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \quad \text{(dB)} \qquad \text{(83E–6)}$$

where

f	is the frequency in GHz
$RLcd$	is the CAUI-4 chip-to-module input differential to common mode input return loss

Note: Values to be adjusted after compliance board design complete

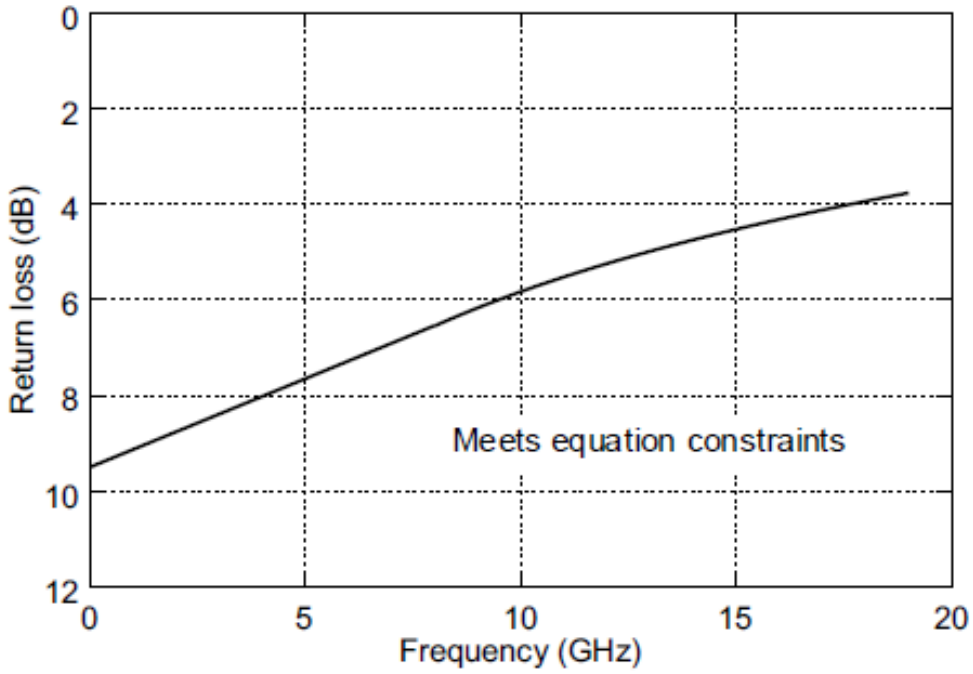

Figure 12: Differential input return loss

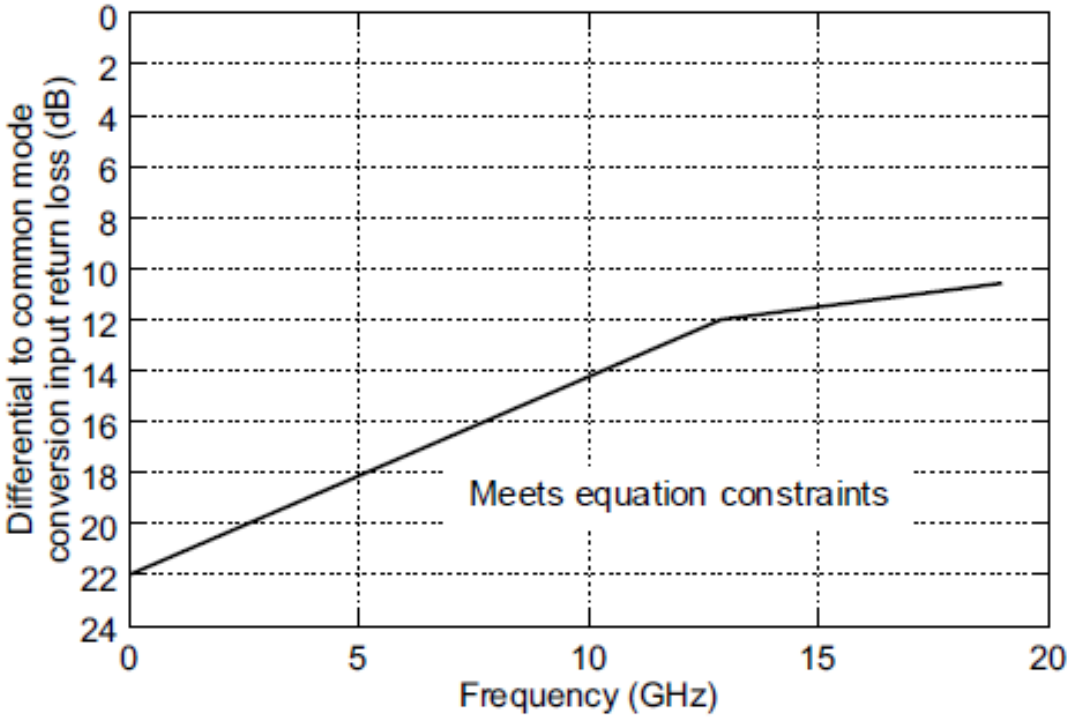

Figure 13: Differential to common mode conversion input return loss

99E.3.3.2 Host stressed input test

The host stressed input tolerance is measured using the procedure defined in 99E.3.3.2.1. The input shall satisfy the input tolerance defined in Table 99E–5.

Table 5: Host stressed input parameters

Parameter	Value
Eye width	0.57 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye Height	228 mV

99E.3.3.2.1 Host stressed input test procedure

The host stressed input test is summarized in Figure 99E–14. The stress signal is applied at TP4a, and is calibrated at TP4. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4 (PRBS9, see Table 86-11 and Table 68-6). The reference receiver includes a Decision Feedback Equalizer (DFE) and a selectable CTLE given by Equation (99E–4) and the first two rows of Table 99E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern. The amount of applied peak-to-peak sinusoidal jitter used for the host stressed input test is given in Table 99E–5. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9. The data rate should be approximately 1/10th of the stressed pattern data rate (5.156 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 99E–6.

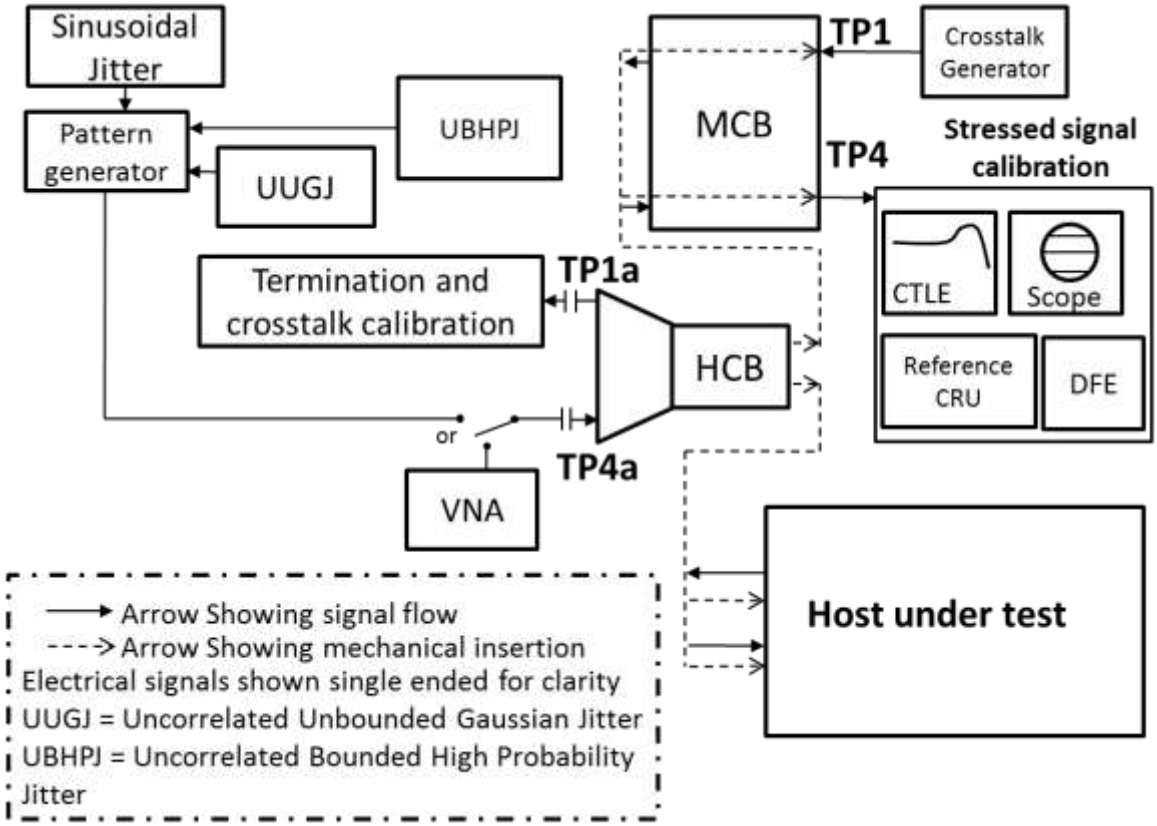

Figure 14: Example host stressed input test

Table 6: Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI
[a] Total Jitter at BER of 10^{-6} [b] Random jitter at BER of 10^{-6} [c] As defined in 92.8.3.8.1	

The counter propagating crosstalk channels during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 10 ps as measured at TP1a. The crosstalk signal transition time is calibrated with Pattern 4. The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for amplitude calibration and the stressed input test. Patterns 3, 4 and 5 are described in Table 86-11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test. Eye height and eye width are measured at TP4 based on the eye measurement methodology given in 99E.4.2. Random jitter and the pattern generator output amplitude are adjusted (without exceeding the differential pk-pk input voltage tolerance

specification as shown in Table 99E–4) to result in the eye height and eye width given in Table 99E–5 using the reference receiver with the setting of the Decision Feedback Equalizer (DFE) and CTLE that maximizes the product of eye height and eye width.

A host input test signal should have a vertical eye closure in the range of 4.5 dB to 5.5 dB with a target value of 5 dB. The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the input test which is conducted by inserting the HCB into the host under test.

99E.3.4 CDAUI-8 module input characteristics

A CDAUI-8 module input shall meet the specifications defined in Table 99E–7 if measured at the appropriate test point.

Table 7: CDAUI-8 Module input Characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate per lane (range)	3.1.1	TP1	51.5625 ±100	GBd
Differential pk-pk input voltage tolerance (min)	3.1.2	TP1a	900	mV
Differential input return loss (min)	3.3.1	TP1	Equation 5	dB
Differential to common mode input return loss (min)	3.3.1	TP1	Equation 6	dB
Differential termination mismatch (max)	3.1.4	TP1	10	%
Module stressed input test[a]	3.4.1	TP1a	See 3.4.1	
Single-ended voltage tolerance range (min)	3.1.2	TP1a	-0.4 to 3.3	V
DC common mode voltage (min)[b]	3.1.2	TP1	-350	mV
DC common mode voltage (max)[b]	3.1.2	TP1	2850	mV

[a]Meets BER specified in 1.1

[b]DC common mode voltage generated by host. Specification includes effects of ground offset voltage.

99E.3.4.1 Module stressed input test

The module stressed input tolerance is measured using the procedure defined in 99E.3.4.1.1. The input shall satisfy the input tolerance defined in Table 99E–8.

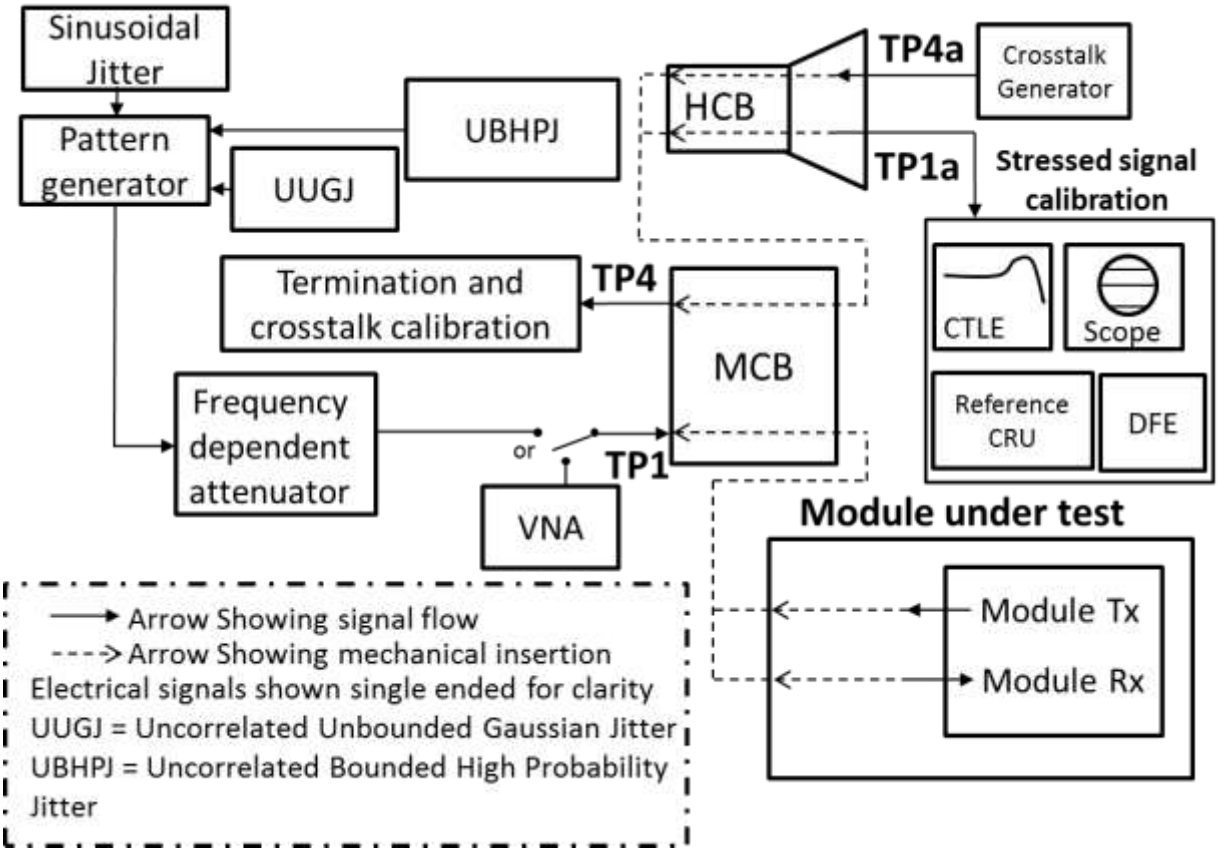

Figure 15: Example module stressed input test

Table 8: Module Stressed input parameters

Parameter	Value
Eye width	0.46 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye Height	60 mV

99E.3.4.1.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 99E–15. The stress signal is applied at TP1, and is calibrated at TP1a. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stress signal using Pattern 4. The reference receiver includes a selectable CTLE given by Equation (99E–4) and Table 99E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel, and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 99E–8. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be

between PRBS7 and PRBS9. The data rate should be approximately 1/10th of the stressed pattern data rate (5.156 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value must also be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 99E–9. The target pattern generator 20% to 80% transition time in the module stressed input test is 9.5 ps. The return loss of the test system as measured at TP1 meets the specification given in Equation (99E–2).

Table 9: Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI
[a] Total Jitter at BER of 10^{-6} [b] Random jitter at BER of 10^{-6} [c] As defined in 92.8.3.8.1	

The counter propagating crosstalk channels during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 12 ps as measured at TP4. The crosstalk signal transition time is calibrated with Pattern 4. The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for amplitude calibration and the stressed input test. Patterns 3, 4 and 5 are described in Table 86-11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes being active during the stressed input test. Two levels of frequency dependent attenuation are used for the module stressed input test: high loss, and low loss. For the high loss case, frequency dependent attenuation is added such that the loss at 25 GHz from the output of the pattern generator to TP1a is 18 (15?) dB. Eye height and eye width, extrapolated to a probability of 10-6, are then measured at TP1a based on the eye measurement methodology given in 99E.4.2. Random jitter and the pattern generator output amplitude are adjusted (without exceeding the differential pk-pk input voltage tolerance specification as shown in Table 99E–7) to result in the eye height and eye width given in Table 99E–8 using the reference receiver with the setting of the CTLE that maximizes the product of eye height and eye width. For the low loss case, discrete frequency dependent attenuation is removed such that from the output of the pattern generator to TP1a comprises the mated HCB/MCB pair as described in 99E.4.1. Eye height and eye width at TP1a are then adjusted in the same way as described for the high loss case. The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3 or a valid 100GBASE-R signal for the input test which is conducted by inserting the module into the MCB. The module CDAUI-8 receiver under test shall meet the BER requirement as described in 99E.1.1 for both the high loss test and low loss test.

99E.4 CDAUI-8 measurement methodology

This subclause describes common measurement tools and methodologies to be used for the CDAUI-8 chip-to-module interface. Details of HCB and MCB characteristics are given in 99E.4.1 and details of the eye diagram measurement methodology are given in 99E.4.2.

99E.4.1 HCB / MCB characteristics

HCB characteristics are described in 92.11.1 where the HCB performs the equivalent function as the TP2 or TP3 test fixture. The MCB characteristics are described in 92.11.2 where the MCB performs the equivalent functionality as the cable assembly test fixture. Note: Compliance board values to be adjusted after compliance board design complete

99E.4.2 Eye width and eye height measurement method

Eye diagrams in CDAUI-8 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 66 GHz 3 dB bandwidth, and a selectable continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is Pattern 4. The following procedure should be used to obtain eye height and eye width parameters:

1) Capture Pattern 4 using a clock recovery unit with a corner frequency of 10 MHz and slope of 20 dB/decade and a minimum sampling rate of 3 samples per bit. Collect sufficient samples equivalent to at least 4 million bits to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-6} without extrapolation.

2) Apply the reference receiver including the appropriate CTLE to the captured signal. Any single CTLE setting as described in 99E.3.2.1.1 which meets both eye width and eye height requirements is acceptable. A compliant host passes both the eye width and eye height A limit specified in Table 99E–1.

3) Use the differential equalized signal from step 2 to construct the CDF of the jitter zero crossing for both the left edge (CDFL) and right edge (CDFR), as a distance from the center of the eye. Calculate the eye width (EW6) as the difference in time between CDFR and CDFL with a value of 10^{-6}. CDFL and CDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the eye normalized by the total number of sampled bits. For a pattern with 50% transition density the maximum value for the CDFL and CDFR would be 0.5. The CDFL and CDFR are equivalent to bath tub curves where the BER is plotted versus sampling time.

5) Use the differential equalized signal from step 2 to construct the CDF of the signal voltage in the central 5% of the eye, for both logic 1 (CDF1) and logic 0 (CDF0), as a distance from the center of the eye. Calculate the eye height (EH6) as the difference in voltage between CDF1 and CDF0 with a value of 10^{-6}. CDF0 and CDF1 are calculated as the cumulative sum of histograms of the voltage at the top and bottom of the eye normalized by the total number of sampled bits. For a well balanced number of ones and zeros the maximum value for CDF0 and CDF1 will be 0.5.

99E.4.2.1 Vertical eye closure

Vertical eye closure is calculated using Equation (99E–9)

$$VEC = 20\log\left(\frac{AV}{EH6}\right)$$

Where

VEC is the vertical eye closure in dB

AV is the eye amplitude of the equalized waveform. Eye amplitude is defined as the mean Value of logic one minus the mean value of logic zero in central 5% of the eye