CDAUI-8 Chip-Chip

Tom Palkert

MoSys

12/16/2014

Proposes baseline text for an 8 lane 400G Ethernet electrical chip to chip interface (CDAUI-8) using NRZ modulation. The specification leverages 100G-Base-CR4, KR4 and CAUI-4 chip to chip.

Table of Figures

Tables

Annex 98D

(normative)

Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CDAUI-8)

98D.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CDAUI-8). Figure 98D–1 shows an example relationship of the CDAUI-8 chip-to-chip interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-chip interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

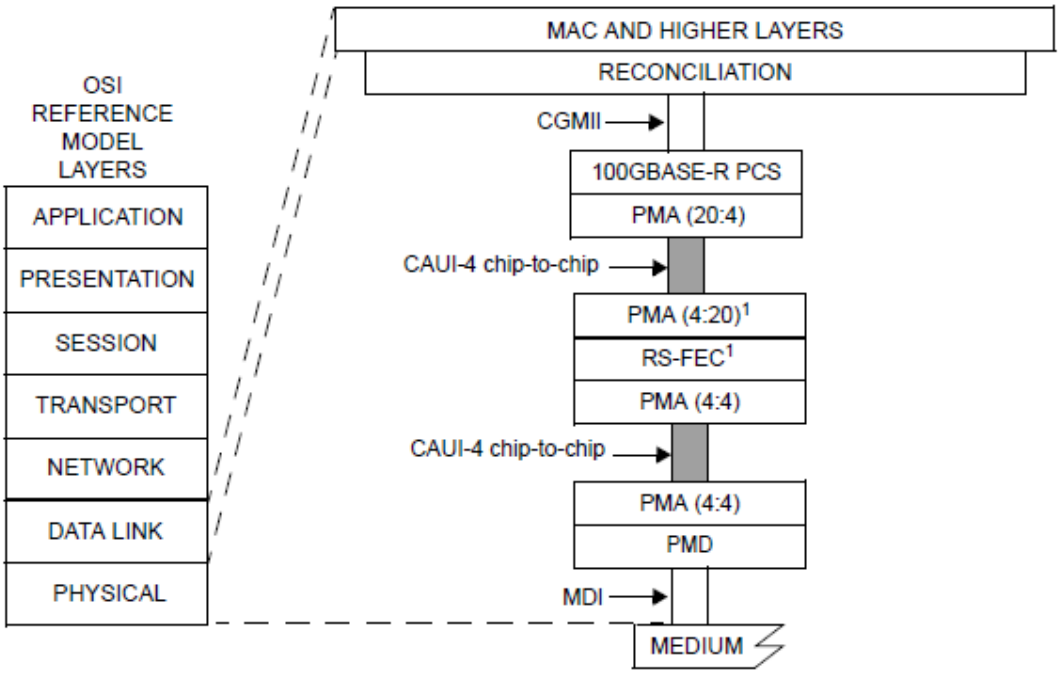

Figure 1: Example CDAUI-8 chip-to-chip relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model

The CDAUI-8 bidirectional link is described in terms of a CDAUI-8 transmitter, a CDAUI-8 channel, and a CDAUI-8 receiver. Figure 98D–2 depicts a typical CDAUI-8 application, and Equation (98D–1) (illustrated in Figure 98D–3) summarizes the informative differential insertion loss budget associated with the chip-to-chip application. The CDAUI-8 chip-to-chip interface comprises independent data paths in each direction. Each data path contains eight differential lanes which are AC coupled. The nominal signaling rate for each lane is 51.5625 GBd. The CDAUI-8 transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 98D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

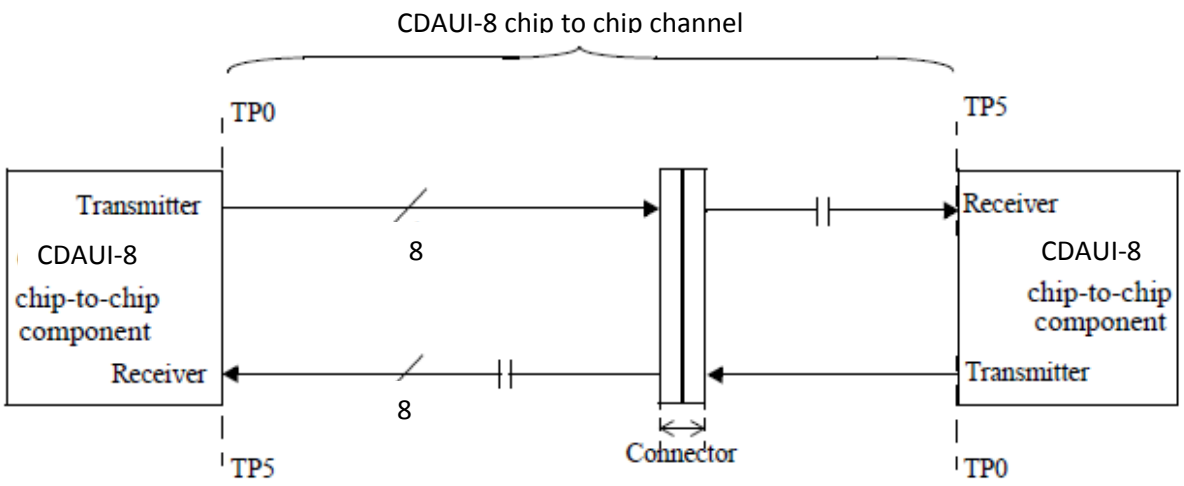

Figure 2: Typical CDAUI-8 chip-to-chip application

The normative channel compliance is through CDAUI-8 COM as described in 98D.4. Actual channel loss could be higher or lower than that given by Equation (98D–1) due to the channel ILD, return loss, and cross-talk.

$$Insertion\ Loss(f) \leq 1.083 + 2.543\sqrt{f} + 0.761f \qquad 0.01 \leq f < 50$$

Where

f	Is the frequency in GHz
Insertion Loss(f)	Is the informative CDAUI-8 chip-to-chip insertion loss

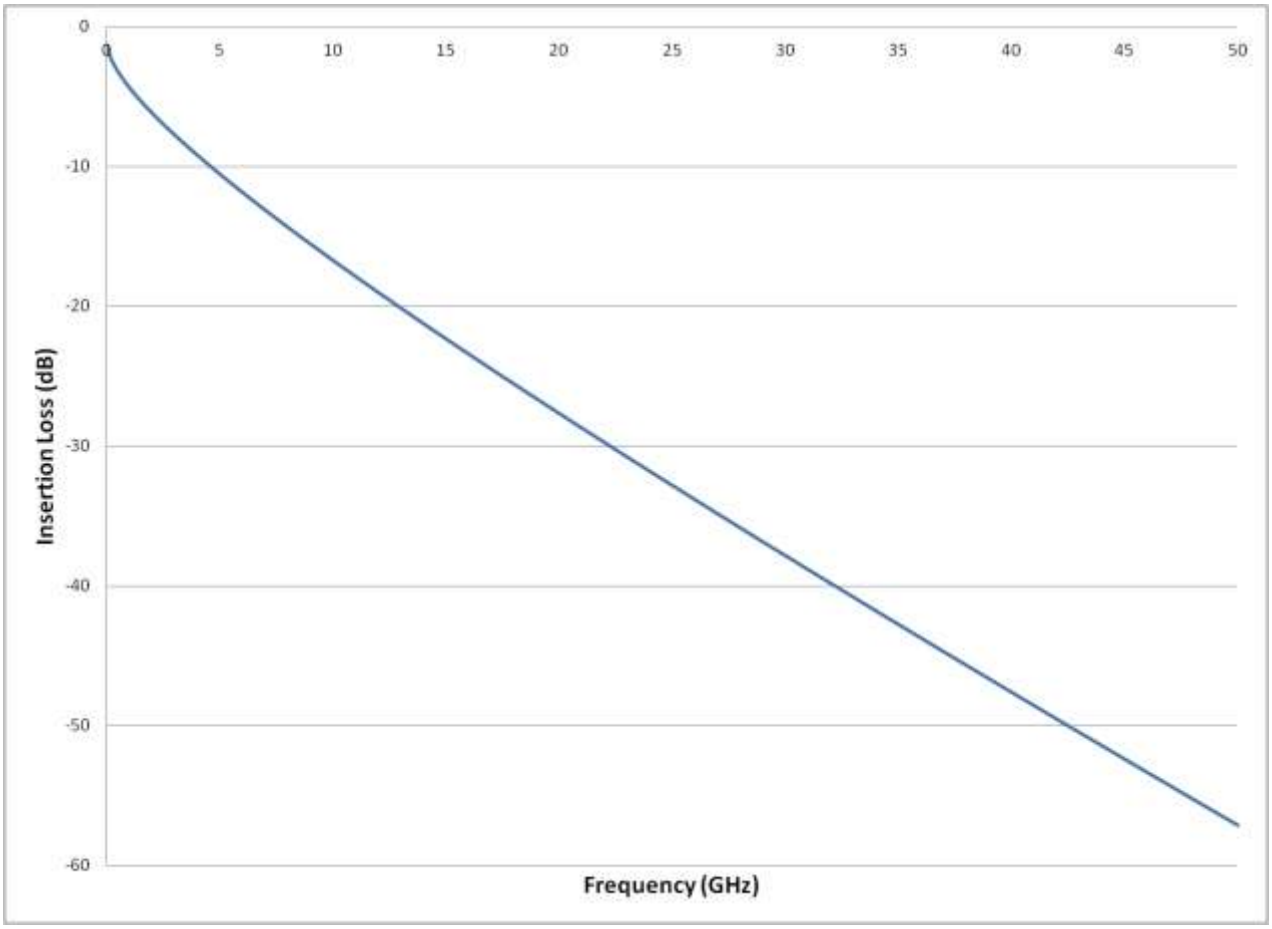

Figure 3: CDAUI-8 chip-to-chip channel insertion loss

98D.2 CDAUI-8 chip-to-chip compliance point definition

The electrical characteristics for the CDAUI-8 chip-to-chip interface are defined at compliance points for the transmitter (TP0a) and receiver (TP5a) respectively. The location of TP0a and electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93-5 and 93.8.1.1 respectively. The location of TP5a and electrical characteristics of the test fixture used to measure the receiver are defined in Figure 93-10 and 93.8.2.1 respectively.

98D.3 CDAUI-8 chip-to-chip electrical characteristics

98D.3.1 CDAUI-8 transmitter characteristics

A CDAUI-8 chip-to-chip transmitter shall meet the specifications defined in Table 98D–1 if measured at TP0a. While the CDAUI-8 chip-to-chip transmitter requirements are similar to those in Clause 93, they differ in that they do not assume transmitter training or a back-channel communications path. Also, the transmit output waveform is not manipulated via the PMD control function described in 93.7.12, but may optionally be manipulated via the feedback mechanism described in 98D.3.3.2. A test system with a fourth-order Bessel-Thomson low-pass response with 60 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

98D.3.1.1 Transmitter equalization settings

The CDAUI-8 chip-to-chip transmitter includes programmable equalization to compensate for the frequency dependent loss of the channel and to facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 98D–4.

Table 1: CDAUI-8 transmitter characteristics at TP0a

Parameter	Reference	Value	Units
Signaling rate per lane (Range)		51.5625 ± 100 ppm	GBd
Differential peak to peak output voltage (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage (max)	93.8.1.3	1.9	V
Common-mode voltage (min)	93.8.1.3	0	V
AC common-mode output voltage (mas, RMS)	93.8.1.3	12	mV
Differential output return loss (min)		TBD	dB
Common-mode output return loss (min)		TBD	dB
Output waveform[a] Steady state voltage *vf* (max) Steady state voltage *vf* (min) Linear fit pulse peak (min) Pre-cursor equalization Post-cursor equalization	 93.8.1.5.2[b] 93.8.1.5.2[b] 93.8.1.5.2[b] 98D.3.1.1 98D.3.1.1	 0.6 0.4 0.71 x v_f Table 98D–2 Table 98D–3	 V V V - -
Signal-to-noise-and-distortion ratio (min)	93.8.1.6[b]	27	dB
Output Jitter (max) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak[c] Effective total uncorrelated jitter, peak-to-peak[cd]	92.8.3.8	 0.035 0.1 0.22	 UI UI UI

[a]The state of the transmit equalizer is controlled by management interface.

[b]The values of the parameters are measured as defined in the referenced subclause except that the values of N_p and N_w are 5.

[c]Effective bounded uncorrelated jitter and effective total uncorrelated jitter are measured as defined in 92.8.3.8.2.

The transmitter output equalization is characterized using the linear fit method described in 93.8.1.5.1 where the state of the CDAUI-8 transmit output is manipulated via management.

The variable *Local_eq_cm1* controls the weight of the pre-cursor tap c(–1), by changing the ratio c(–1)/(|c(–1)|+|c(0)|+|c(1)|). The valid values of *Local_eq_cm1* and the corresponding ratios are specified in Table 98D–2. The variable *Local_eq_c1* controls the weight of the post-cursor tap c(1), by changing the ratio c(1)/(|c(–1)|+|c(0)|+|c(1)|). The valid values of *Local_eq_c1* and the corresponding ratios are specified in Table 98D–3. *Local_eq_cm1* and *Local_eq_c1* are independent of each other and independent on each lane. Each successive step in *Local_eq_cm1* and *Local_eq_c1* value shall result in a monotonic change in transmitter equalization.

If a Clause 45 MDIO is implemented, *Local_eq_cm1* and *Local_eq_c1* for each lane (0 through 3) and direction (transmit and receive) are accessible through registers 1.180 through 1.187 (see 45.2.1.92ab through 45.2.1.92ae).

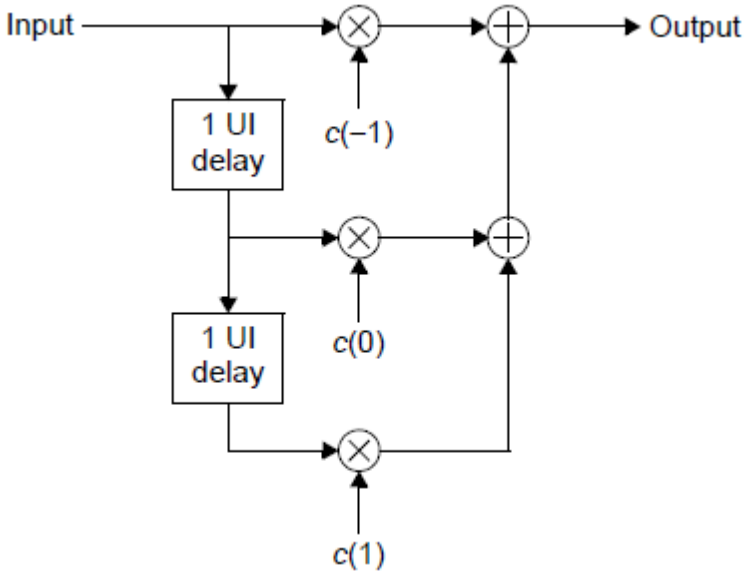

Figure 4: Transmit equalizer functional model

Table 2: Pre-cursor equalization

Local_eq_cm1 **value**	$\boldsymbol{c(-1)}$ **ratio** $\left(\frac{\boldsymbol{c(-1)}}{\boldsymbol{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}}\right)$
0	0±0.04
1	-0.05±0.04
2	-0.1±0.04
3	-0.15±0.04

Table 3:Post-cursor equalization

Local_eq_c1 **value**	$\boldsymbol{c(1)}$ **ratio** $\left(\frac{\boldsymbol{c(1)}}{\boldsymbol{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}}\right)$
0	0±0.04
1	-0.05±0.04
2	-0.1±0.04
3	-0.15±0.04
4	-0.2±0.04
5	-0.25±0.04

98D.3.2 Optional EEE operation

98D.3.3 CDAUI-8 receiver characteristics

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78 and 78.3) then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CDAUI-8 shutdown.

If the EEE capability includes CDAUI-8 shutdown (see 78.5.2) then when aui_tx_mode (see 83.5.11.3) is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the CDAUI-8. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When aui_tx_mode is QUIET, the transmit direction CDAUI-8 transmitter is disabled as specified below. Similarly when the received aui_tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00 which is transmitted across the CDAUI-8. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the MA:IS_UNITDATA_i.indication primitive. When the received aui_tx_mode is QUIET, the receive direction CDAUI-8 transmitter is disabled as specified below.

For EEE capability with CDAUI-8 shutdown, the CDAUI-8 transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of aui_tx_mode changing to QUIET in the relevant direction. Furthermore, the CDAUI-8 transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of aui_tx_mode ceasing to be QUIET in the relevant direction.

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction CDAUI-8 if PEASE is asserted and aui_tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction CDAUI-8 if PIASE is asserted and the received aui_tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction aui_tx_mode changes to any state other than QUIET within a time and voltage level specified in this section.

98D.3.3 CDAUI-8 receiver characteristics

A CDAUI-8 chip-to-chip receiver shall meet the specifications defined in Table 98D–4 if measured at TP5a.

Table 4: CDAUI-8 receiver characteristics at TP5a

Parameter	Subclause Reference	Value	Units
Differential input return loss (min)		TBD	dB
Differential to common mode input return loss		TBD	dB
Interference tolerance	98D.3.3.1	Table 98D-5	-

98D.3.3.1 Receiver interference tolerance

The receiver shall satisfy the requirements for interference tolerance defined in Table 98D–5. The interference tolerance test uses the method described in Annex 93C as specified by 93.8.2.3, with the following exceptions:

a) The parameters in Table 98D–5 replace the parameters in Table 93-6.

b) The transmitter taps are set via management (see 98D.3.1.1) to the settings that provide the lowest BER.

c) Sinusoidal jitter is added to the test transmitter by modulating the clock source.

Table 5: Receiver interference tolerance parameters

Parameter	Test 1 Values			Test 2 Values			Units
	Min	Max	Target	Min	Max	Target	
Bit error ratio[ab]	-	10^{-6}		-	10^{-6}		-
Applied pk-pk sinusoidal jitter			Table 88-13			Table 88-13	
Insertion loss at 26 GHz[c]	31	32		10	11		dB
Coefficients of fitted insertion loss[d] a_0 a_1 a_2 a_4	 -1 0 0 0	 2 2.937 1.599 0.03		 -1 0.817 0.801 0.01			 dB $dB/GHz^{1/2}$ dB/GHz dB/GHz^2
RSS_DFE2[e]					-		-
COM including effects of broadband noise	-	-	2	-	-	2	dB

[a]Bit error ratio replaces the RS symbol error ratio measurement in 93.8.2.3

[b]Maximum BER assumes errors are not correlated to ensure sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard

[c]Measured between TPt and TP5 (see Figure 93C-4)

[d]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with f_{min} = 0.05 GHz, and f_{max} = 51.5625 GHz, and maximum Δf = 0.01 GHz

[e]RSS_DFE2 is equivalent to RSS_DFE4 described in 93A.2 except that n_1=2 and n_2=5.

98D.3.3.2 Transmitter equalization feedback (optional)

Transmitter equalization feedback is an optional capability for a CDAUI-8 chip-to-chip receiver. If implemented, it shall operate as described in this subclause.

Transmitter equalization feedback is generated for each lane (0 through 3) and direction (transmit and receive) independently. The variables that control transmitter equalization feedback are specific for each lane and direction.

A CDAUI-8 chip-to-chip receiver may generate a request to change the transmit equalization coefficients of the remote transmitter to new values by setting the *Request_flag* variable to 1. The variables *Request_eq_cm1* and *Request_eq_c1* indicate the request values of *Local_eq_cm1* and *Local_eq_c1*, respectively; in the remote transmitter (see Table 98D–2 and Table 98D–3). The requested setting may be generated from the remote CDAUI-8 chip-to-chip transmitter's equalization setting, which is stored in variables *Remote_eq_cm1* and *Remote_eq_c1*, and from information internal to the receiver, in an implementation specific manner.

When a CDAUI-8 chip-to-chip receiver does not request a change of the remote transmitter's transmit equal-ization setting, it sets the *Request_flag* variable to 0. A CDAUI-8 chip-to-chip receiver that does not implement transmitter equalization feedback always sets *Requests_flag* to 0. If a Clause 45 MDIO is implemented, the variables *Request_flag, Requested_eq_cm1, Requested_eq_c1, Remote_eq_cm1* and *Remote_eq_c1* for each lane and direction are accessible through registers 1.180 through 1.187 (see 45.2.1.92ab through 45.2.1.92ae).

98D.3.4 Global energy detect function for optional EEE operation

The global energy detect function is mandatory for EEE capability with the deep sleep mode option and CDAUI-8 shutdown. The global energy detect function indicates whether or not signaling energy is being received on the physical instantiation of the inter sublayer interface (in each direction as appropriate). The energy detection function may be considered a subset of the signal indication logic. If no energy is being received on the CDAUI-8 for the ingress direction SIGNAL_DETECT is set to FAIL following a transition from aui_rx_mode = DATA to aui_rx_mode = QUIET. When aui_rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that corresponds to an ALERT signal driven from the CDAUI-8 link partner. While aui_rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is received.

98D.4 CDAUI-8 chip-to-chip channel characteristics

The Channel Operating Margin (COM), computed using the procedure in Annex 93A and the parameters in Table 98D–6, shall be greater than or equal to 2 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization coefficients.

Table 6: Channel Operating Margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	51.5625	GBd
Maximum start frequency	F_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model			
Single-ended device capacitance	C_d	2.5×10^{-4}	nF
Transmission line length, Test 1	Z_p	12	mm
Transmission line length, Test 2	Z_p	30	mm
Single-ended board capacitance	C_b	1.8×10^{-4}	nF

Single-ended reference resistance	R_o	50	ohms
Single-ended termination resistance	R_d	55	Ohms
Reciever 3 dB bandwidth	f_r	0.75 x f_b	GHz
Transmitter equalizer, minimum cursor coefficient	c(0)	0.6	-
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	c(-1)	 -0.20 0 0.05	-
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	c(1)	 -0.40 0 0.05	-
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 -12 0 1	dB
Continuous time filter, zero frequency	f_z	$f_b/4$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/4$ f_b	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	-
Level seperation mismatch ratio	R_{LM}	1	
Transmitter signal-to-noise ratio	SNR_{TX}	27	dB
Number of samples per unit interval	M	32	-
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit, for n=1 to Nb	$B_{max}(n)$	1.0	-
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_o	5.2 x 10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	-

98D.5 Example usage of the optional transmitter equalization feedback

98D.5.1 Overview

If implemented, transmitter equalization feedback from a CDAUI-8 chip-to-chip receiver may be used to tune the equalization settings of the transmitter at the other end of the CDAUI-8 chip-to-chip link to the values requested by the receiver. An example of a possible transmitter equalization tuning process using transmitter equalization feedback is provided in this subclause.

In this example, two components, A and B, are connected by a CDAUI-8 chip-to-chip link, such that A is closest to the PCS and B is closest to the PMD. Clause 45 MDIO is implemented by both components, with component A at device address 11 and component B at device address 10. Transmitter equalization feedback is implemented by either component A, component B, or both. One Station Management (STA) controls both components.

Figure 98D–5 depicts the components of the CDAUI-8 chip-to-chip link and the registers used during the tuning procedure.

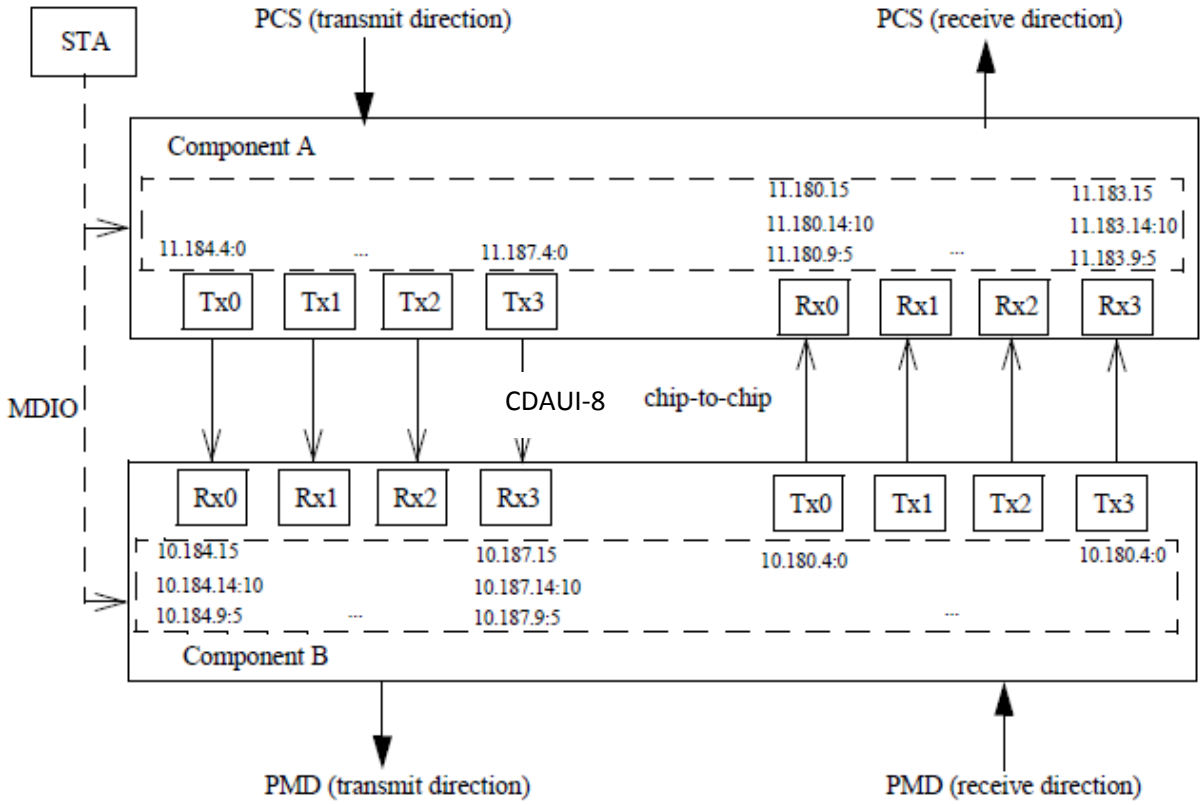

Figure 5:Example transmitter equalization feedback components and registers

The STA performs the procedures described in 98D.5.2 and 98D.5.3 to tune lane 0 equalization settings in both sides of the CDAUI-8 chip-to-chip link. When these procedures are completed, the STA uses similar procedures to tune equalization settings in lanes 1 through 7. When all lanes are tuned, the STA may repeat the process with another pair of components connected by CDAUI-8 chip-to-chip.

Note—Using non-optimal transmitter equalization settings (or changing them) during the tuning procedure may interrupt data communication. The CDAUI-8 bit error ratio is assumed to meet the requirements of 98D.3.3.1 upon completion of the tuning process.