CRU bandwidth for CDAUI-8 C2M and C2C

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Motivation

- D1.3 adopted CRU b/w for C2C and C2M to be 4MHz
- Does 4MHz b/w spec accommodate a wide range of implementations?
- Trade-offs for a lower bandwidth?

CRU loop latency

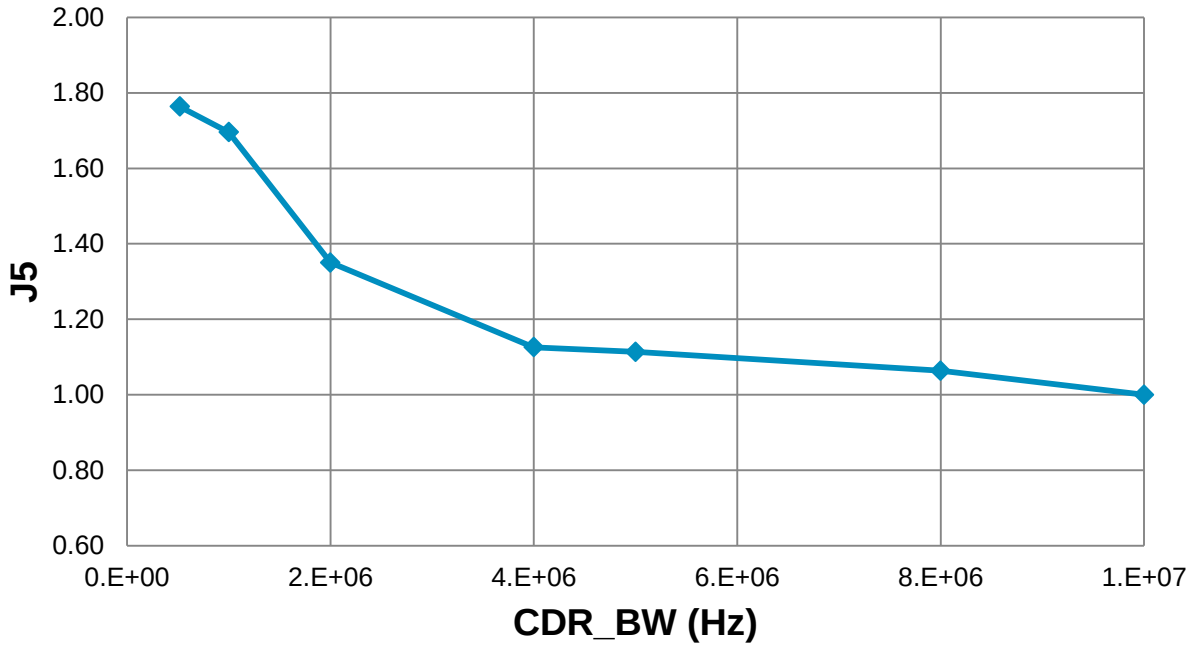
- The CRU bandwidth is a function of achievable loop latency
- Analog implementations can be built with relatively short loop latency
  - Shorter loop latency translates to a higher tracking b/w
- DSP based implementations inherently have longer loop latency
  - Larger number of processing blocks in the signal path
  - Can handle signal non-linearity in a much better way
  - Carry a much higher power and area penalty to improve the tracking b/w
- Higher CRU b/w spec skews the design space in favor of analog implementations for the RX
- Clause 94 CRU b/w is set to 1600kHz
  - Signaling rate = 13.59375 GBd
  - 13.59375 GBd/1600kHz = 8496
- CRU b/w in OIF CEI-56G drafts is fb/8496 = 3.13MHz

Impact on TX

- Should the jitter budgets be revised for the lower b/w CRUs?
- Lab measurements suggest this is may not be needed
  - Measurement on a large production ASIC with on-board clock source
  - TX jitter increases on lowering the CRU b/w to ~3MHz but still within the current limits

Current C2C Jitter Spec:

Jitter Type	Amount
CRJ max (RMS)	0.01 UI
CDJ max (pk-pk)	0.04 UI
Even-odd max	0.019 UI



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