C2M CDAUI-8: considerations towards first P802.3bs 400 Gb/s Ethernet draft.

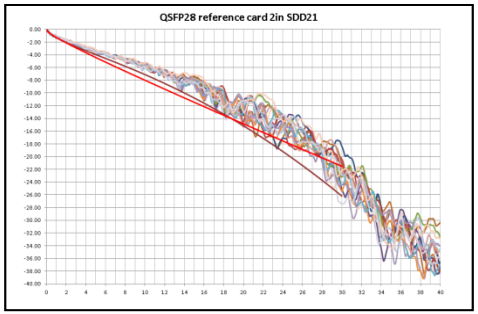
Overview

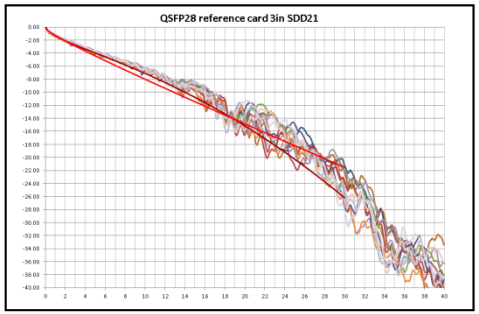
- CDAUI-8 C2M Baseline adopted in March.
- IEEE to OIF liason document in July 2015.
- P802.3bs 400 Gb/s Ethernet Draft 1.0 is expected to be adopted in September.

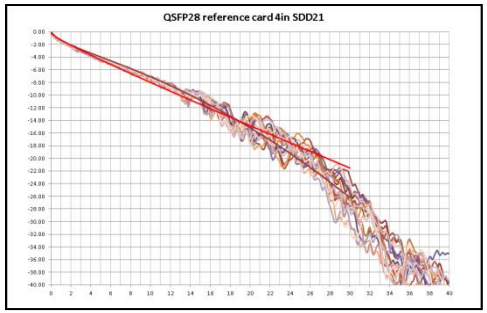
Current driving document about C2M is oif2014.230.
Previous contribution to IEEE CAUI-4 and recent OIF contributions (oif2015.237, oif2015.332 and oif2015.350) highlighted different items that will need to be addressed into CDAUI-8 (CEI-56G PAM) requirements as well.

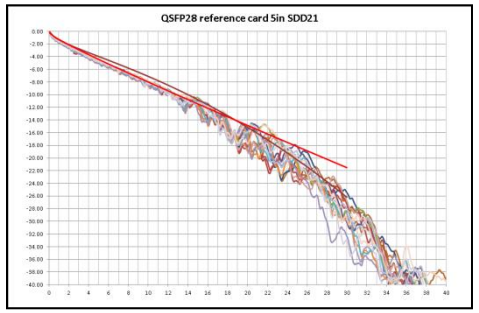
This presentation summarizes the above works, showing some potential options for changes into P802.3bs 400 Gb/s Ethernet Draft 1.0, CDAUI-8 C2M interface.

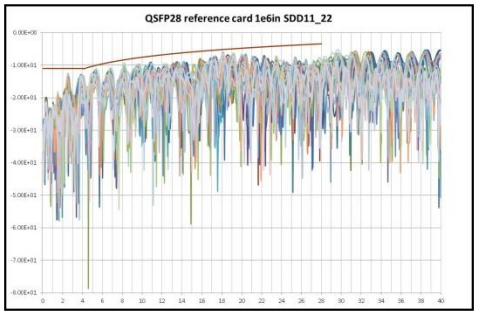
CDAUI-8 (CEI-56G-VSR) reference: Cisco QSFP28 card.

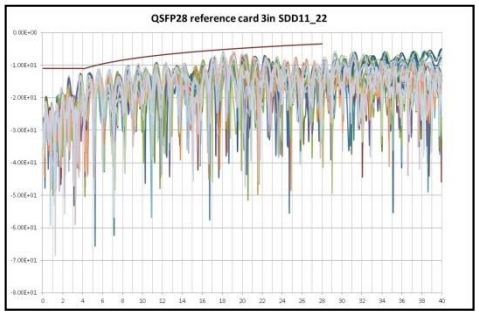


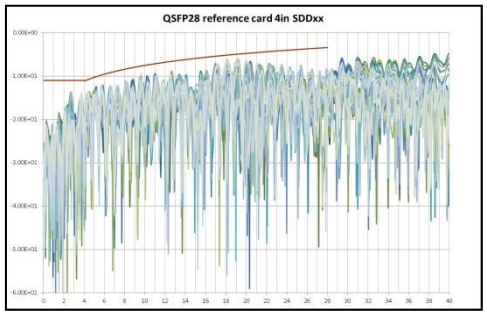


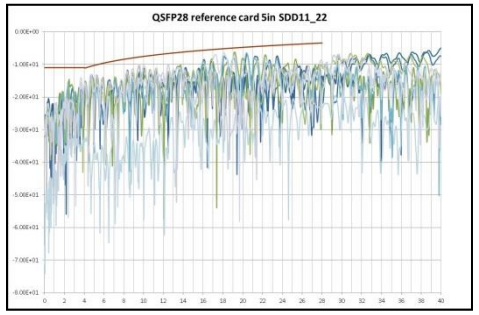


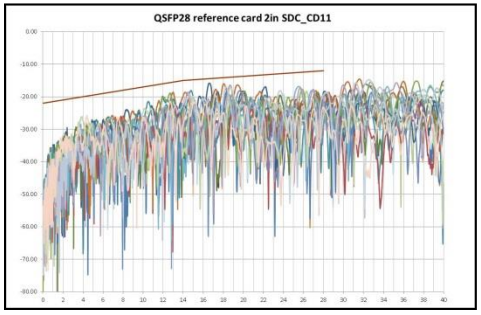


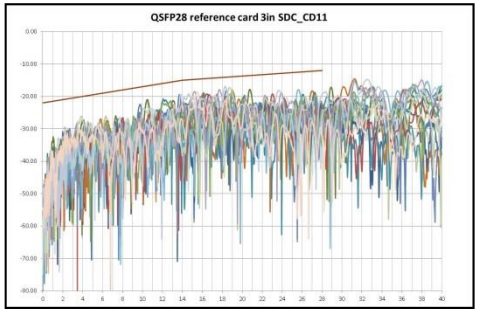


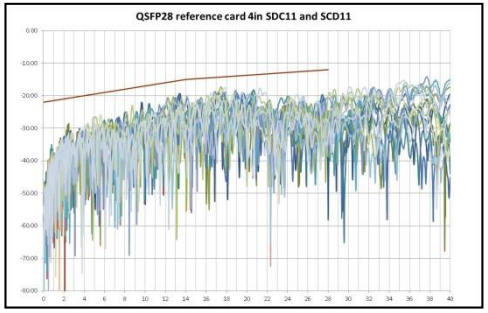


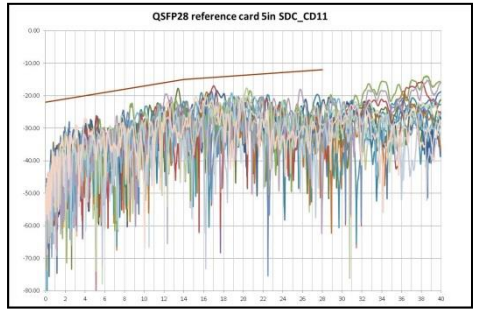








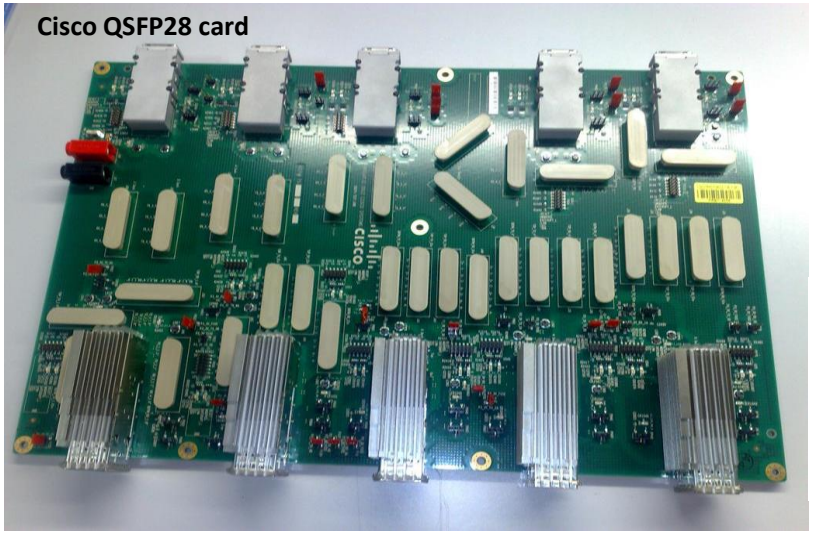


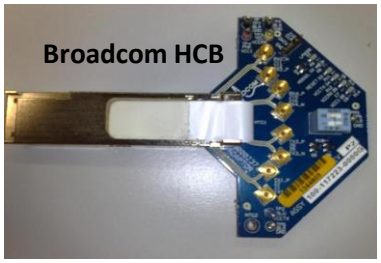


Most tests and simulations done based on Cisco QSFP28 reference card (EM888 material), which is below compared (2, 3, 4 and 5inches channels) to current CEI-56G-VSR PAM requirements (brown line) and current proposed CDAUI-8 channel loss (red line).

Currently OIF CEI-56G-VSR-PAM4 defines a reference receiver with a continuous time linear equalizer (CTLE, two-poles, one-zero) to measure Eye Width and Eye Height.

Our CDAUI-8 (CEI-56G-VSR) reference: Cisco QSFP28 card.



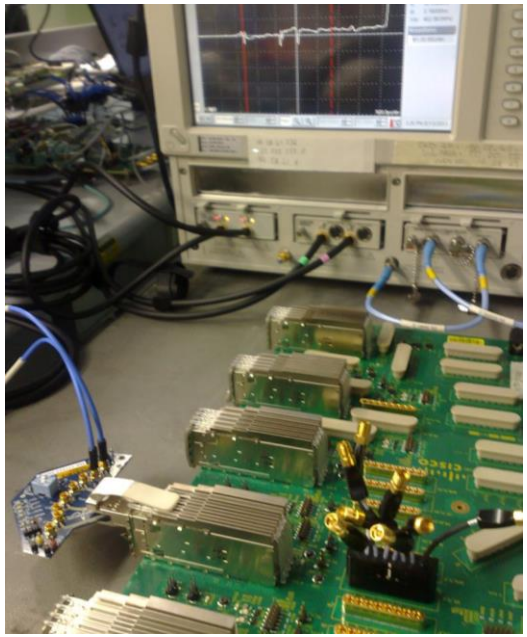


QSFP28 test card

Length	Cal trace	QSFP28 SMT	QSFP28 stacked
1.6	yes	yes	yes
2	yes	yes	yes
3		yes	yes
4	yes	yes	yes
5	yes	yes	yes

The QSFP28 test cards is comprehensive of QSFP28 SMT and stacked connector, terminated on the other side with MXP 1x8 connectors.

Presented S-parameters results over QSFP28 reference card (stacked connector) are comprehensive of MXP and SMT cables.



Highlights of oif2015.237 (Mazzini, Brooks, Reddy Kareti) and further work (Brooks).

a) Lab experiment @28GBaud with a PAM4 DAC.
- QSFP28 reference board 2, 3, 4 and 5" channels tested.
- Compared 14 and 6 T/2 spaced FFE taps, 6 Taps + CEI-56G-VSR CTLE (2p,1z) equalizer and CTLE (2p,1z).

b) Hspice models analysis based on:
- different TX inputs over 5" channel (same S-parameters as point 1).
- 3" and 4" QSFP28 Reference Board Rev 4 (better S-parameters).

c) QSFP28 reference board 5" channel (same S-parameters as point 1):
- Simulation with different combination of available serdes components with appropriate adaptation and optimization algorithms.

- **Both experiments and simulations shown 2p1z module's RX CTLE it's not enough to close the link at 1E-6 BER.**
- **Simulation showing that even a 3p2z RX CTLE equalizer can be tight for 1E-6 BER requirements.**
- **The PAM-4 EQ is much more critical than NRZ for the same symbol time.**
  - **Adjacent Eyes ➔ Very Little Over or Under EQ Allowed!**
  - **Channel variations: worse impact than NRZ ➔ Need of slow (but continuous) adaptation.**

d) Investigation on long data pattern over 5" Channel:
- Benefit of adding a Low Frequency De-emphasis Filter to Correct the Step Response
  Best Case: No RJ, DJ, Noise, Crosstalk.

- **A Low Frequency filter is needed to help equalize long data patterns.**
  - **LF time constant: 0.1ns to 0.5ns for VSR**
  - **LF De-emphasis amount: 0 to 25% for VSR**

Highlights of oif2015.237 (Mazzini, Brooks, Reddy Kareti).

From 28.1GBaud waveforms acquisitions

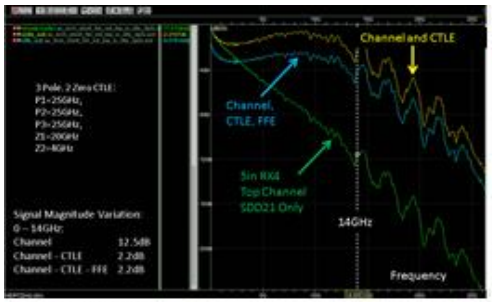
Stack 2'		BER 14 taps FIR	Errors	BER 6 taps FIR	Errors	CTLE2p1z + 6 TAPs FIR	CTLE	Errors	BER CTLE 2p1z	CTLE	Errors
RX2	bot	0.00E+00	0	0.00E+00	0	4.01E-05	5	6	2.97E-03	5	444
RX2	top	4.01E-05	6	1.07E-04	16	2.48E-04	5	37	4.92E-03	5	735
RX4	bot	6.02E-05	9	8.03E-05	12	1.00E-04	5	15	2.83E-01	5	42299
RX4	top	6.69E-06	1	2.01E-05	3	5.35E-05	5	8	3.75E-03	5	561
TX3	bot	6.69E-06	1	2.01E-05	3	6.69E-05	5	10	2.76E-03	5	413
TX3	top	0.00E+00	0	1.34E-05	2	1.34E-05	5	2	1.77E-03	5	264
TX1	bot	6.69E-06	1	3.34E-05	5	6.02E-05	5	9	1.92E-03	5	287
TX1	top	0.00E+00	0	0.00E+00	0	1.34E-05	5	2	2.98E-03	5	446

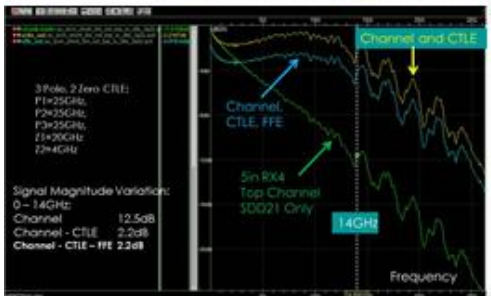
Stack 3'		BER 14 taps FIR	Errors	BER 6 taps FIR	Errors	CTLE2p1z + 6 TAPs FIR	CTLE	Errors	BER CTLE 2p1z	CTLE	Errors
RX2	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	9.77E-04	5	146
RX2	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	1.04E-03	5	156
RX4	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.92E-01	5	43616
RX4	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.93E-01	5	43859
TX1	bot	0.00E+00	0	2.01E-05	3	2.01E-05	5	3	3.77E-03	5	564
TX1	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	6.69E-05	5	10
TX3	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	1.67E-03	5	249
TX3	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	1.14E-03	5	171

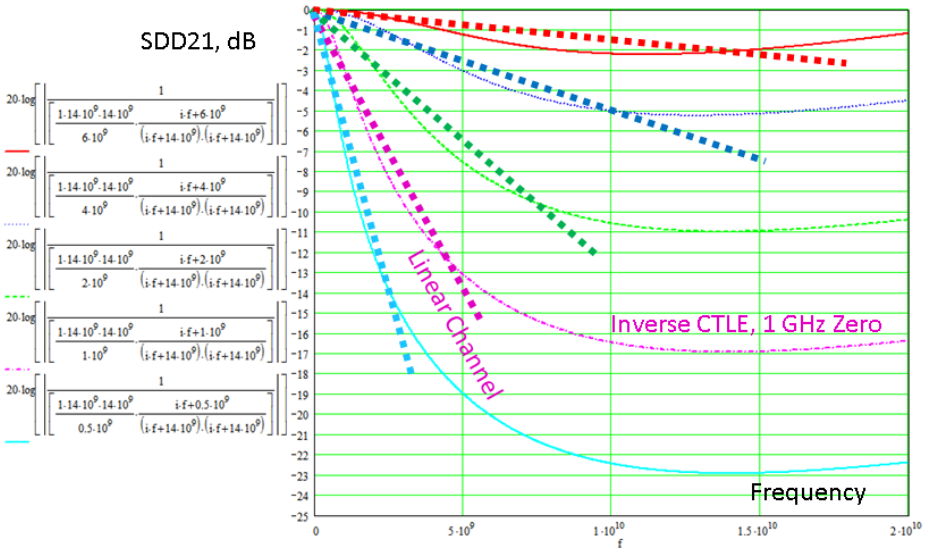
Stack 4'		BER 14 taps FIR	Errors	BER 6 taps FIR	Errors	CTLE2p1z + 6 TAPs FIR	CTLE gain	Errors	BER CTLE 2p1z	CTLE gain	Errors
RX2	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	7.83E-04	5	117
RX2	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	3.93E-03	5	587
RX4	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.88E-01	5	43007
RX4	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.85E-01	5	42677
TX1	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	8.70E-05	5	13
TX1	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	1.34E-02	5	2001
TX3	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	3.01E-04	5	45
TX3	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	1.26E-03	5	188

Stack 5'		BER 14 taps FIR	Errors	BER 6 taps FIR	Errors	CTLE2p1z + 6 TAPs FIR	CTLE gain	Errors	BER CTLE 2p1z	CTLE gain	Errors
RX2	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	3.91E-02	5	5842
RX2	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	3.12E-02	5	4657
RX4	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.86E-01	5	42680
RX4	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.88E-01	5	43103
TX1	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.01E-02	5	2999
TX1	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	1.32E-02	5	1969
TX3	bot	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	1.91E-02	5	2856
TX3	top	0.00E+00	0	0.00E+00	0	0.00E+00	5	0	2.41E-02	5	3596

- **2p1z CTLE not enough to ensure the correct target BER over any of the QSFP28 card tested cases.**
- **FFE or higher order CTLE seems needed.**



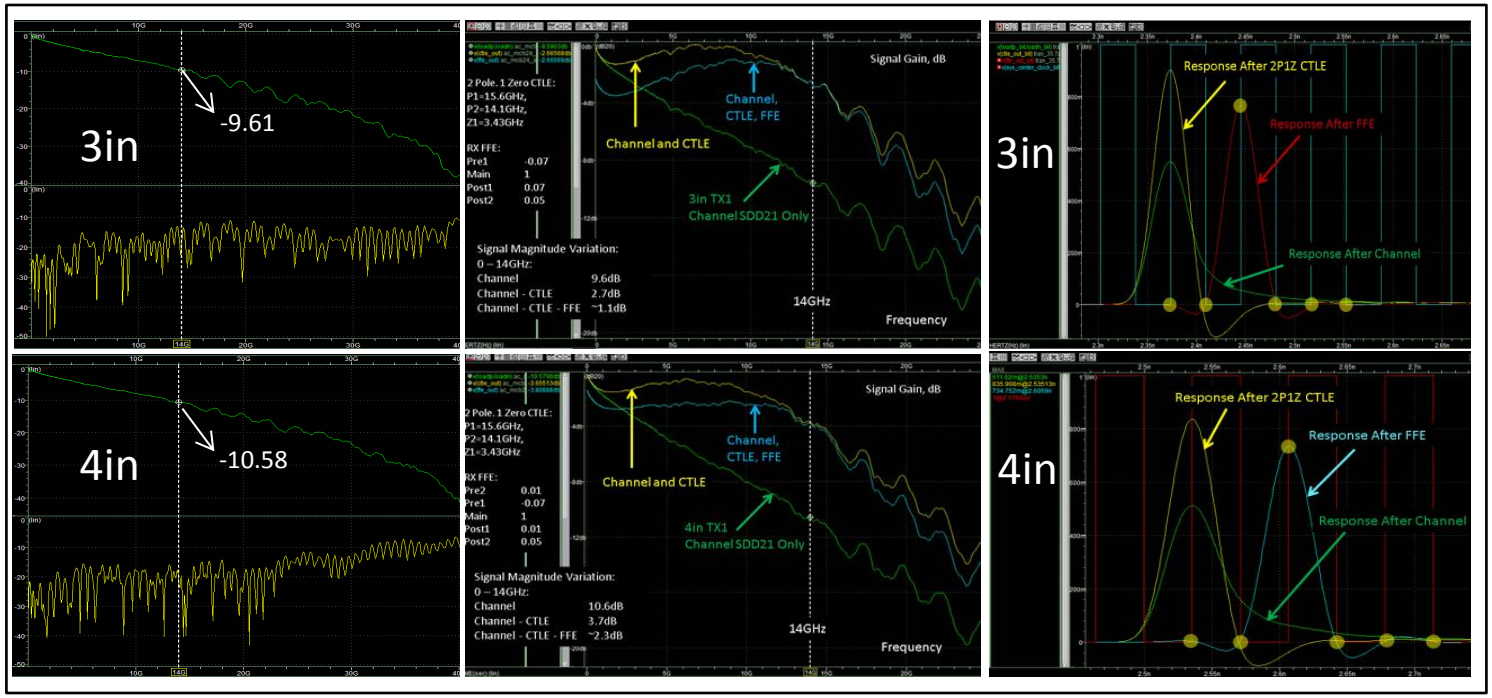




- **Channels are Roughly Linear on a dB vs Linear Frequency Plot.**
- **With CTLE Alone, Channels can be Equalized only up to a certain frequency.**

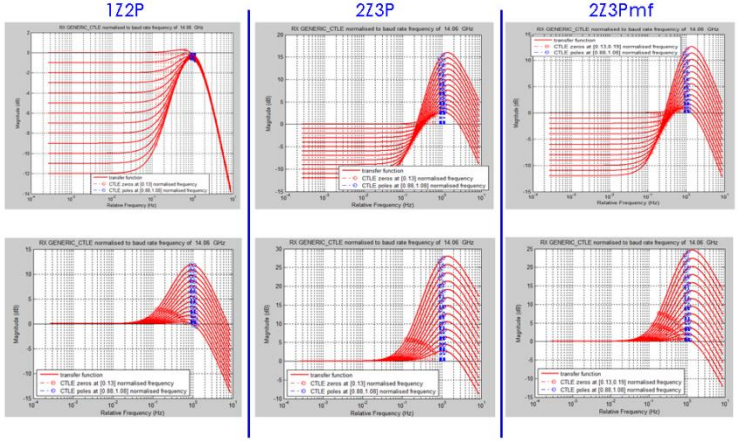
5in

Highlights of oif2015.237 (Mazzini, Brooks, Reddy Kareti).



Similar behavior is found over 3 and 4inches channels. CTLE,FFE allows better channel flatness and impulse response.

CTLE Types and Their Behavior : 1Z2P, 2Z3P and 2Z3Pmf.

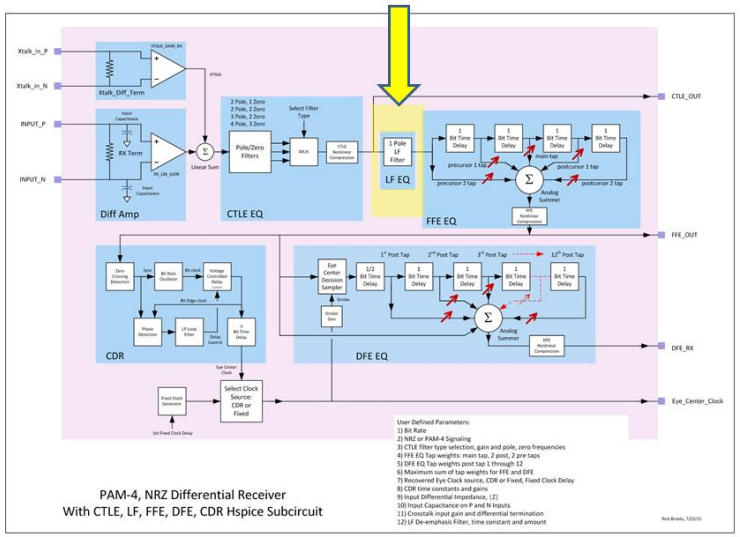


Case#	Transmitter BW Filter	Transmitter FIR	Receiver Gain Profile Setting	Receiver Gain Profile LF, dB	Receiver Gain Profile HF, dB	Receiver CTLE Type	Receiver FFE	BIT Error Rate 28G-VSR(NRZ)	BIT Error Rate 56G-VSR(PAM4)
1			11.5/11.5	0	11.5	1Z2P		1.00E-06	1.00E-03
2			12/12	0	12	1Z2P		1.00E-06	4.00E-03
3			7/7	0	17	2Z3P		3.00E-06	3.00E-03
4			8/8	0	20	2Z3P		1.00E-07	1.00E-05
5			9/9	0	18	2Z3Pmf		1.00E-07	7.00E-05
6			10/10	0	20	2Z3Pmf		1.00E-07	1.00E-05
7		5 tap	7/7	0	7	1Z2P		1.00E-05	8.00E-03
8		5 tap	8/8	0	8	1Z2P		3.00E-05	3.00E-03
9	Raised Cosine	5 tap	11/8	3	11	1Z2P		3.00E-05	3.00E-04
10	Raised Cosine		18/12	6	18	1Z2P		2.00E-04	8.00E-04
11	Raised Cosine		14/7	6	26	2Z3P		1.00E-05	1.00E-05
12		5 tap	8/4	4	10	2Z3P		1.00E-06	1.00E-04
13	Raised Cosine	5 tap	8/4	4	10	2Z3P		1.00E-05	1.00E-04
14			11 aFFE	11	11	VGA	9 tap	1.00E-05	5.00E-04
15			7/7	0	7	1Z2P	5tap	3.00E-05	3.00E-04

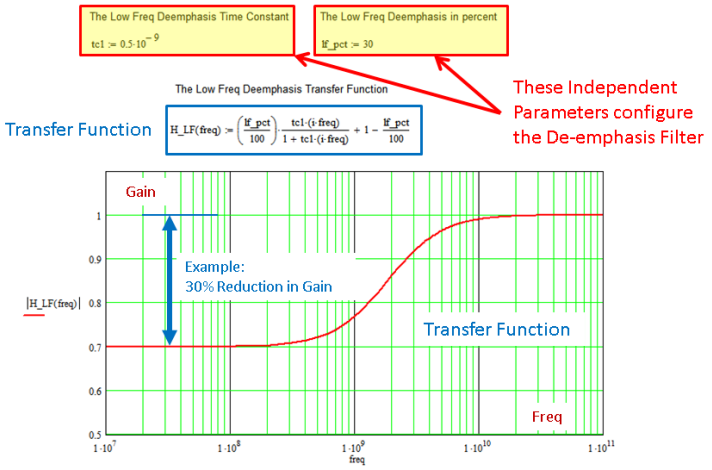
indicates possible solution(s) meeting objectives

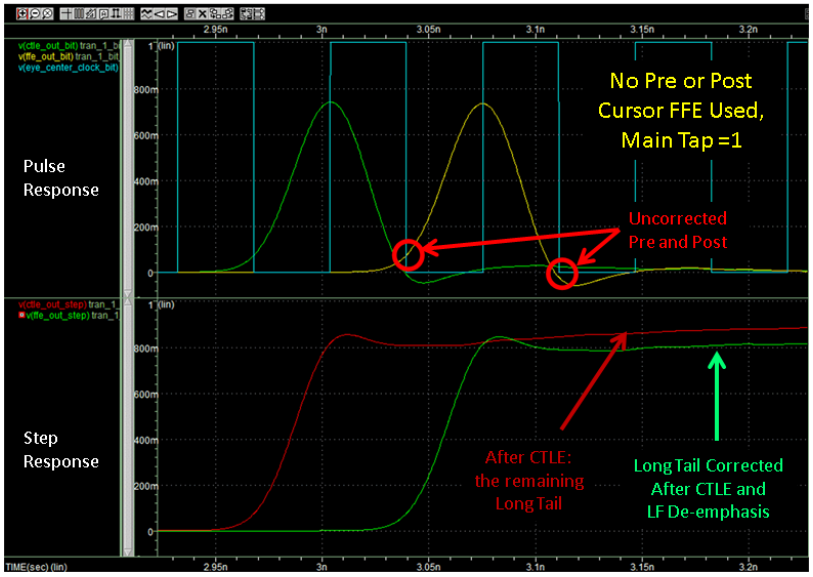
Further work: investigation on long data pattern over 5” Ch. (Brooks).

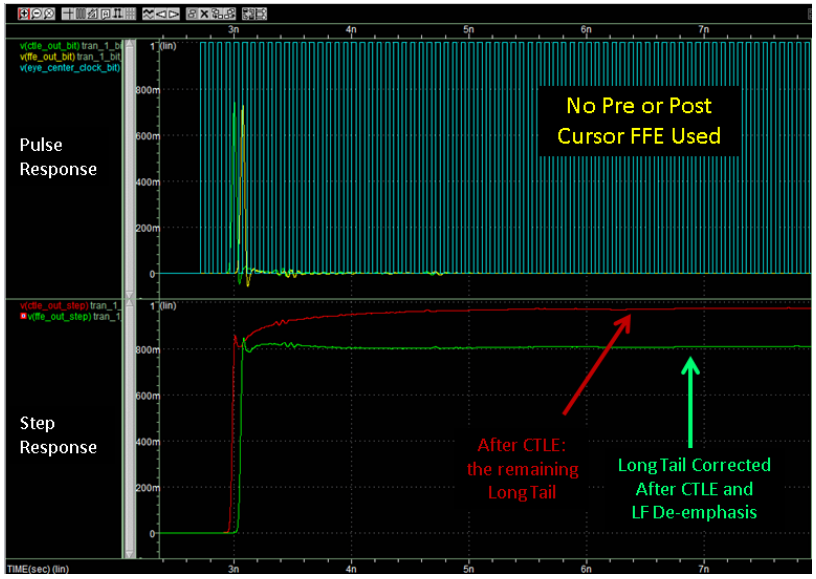
Adding Low Frequency De-emphasis Filter to Generic RX Model



Low Frequency Linear De-emphasis Filter Transfer Function

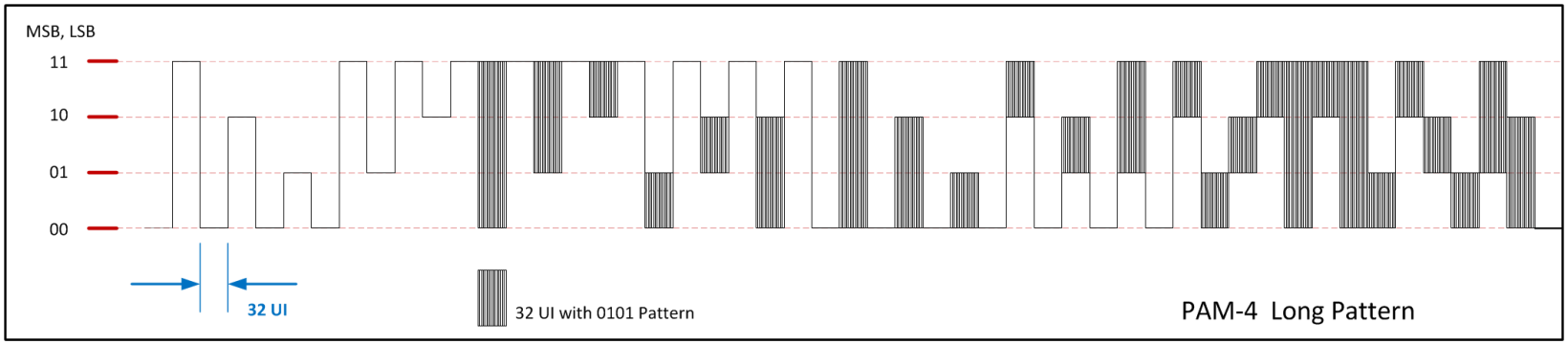




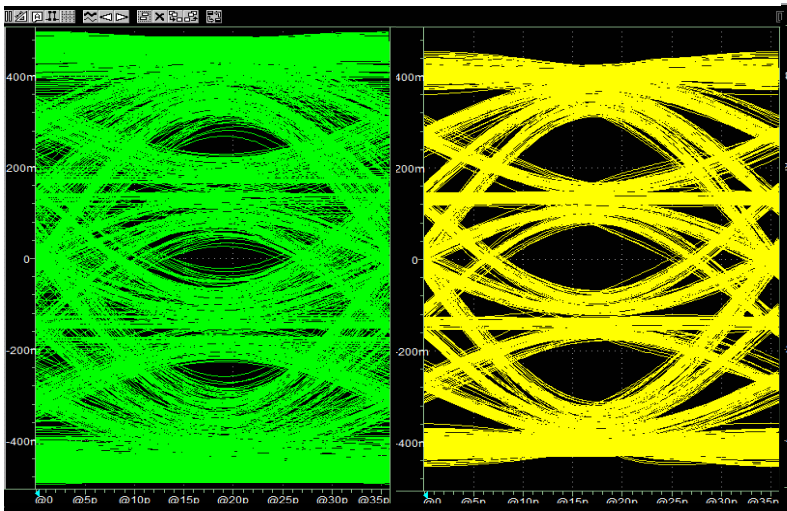


5” Channel Pulse Response – CTLE, Low Freq De-emphasis, No FFE

Further work: investigation on long data pattern over 5” Ch. (Brooks).

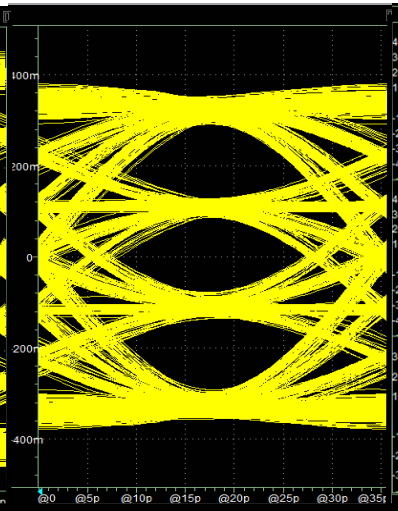


- In typical applications, Serdes run scrambled data patterns of 64B/66B encoded data.
- Long run lengths of zeros or ones are possible, surpassing 32 UI in length at times.
- The proposed data pattern uses 1600 UI total to allow simulation of possible wide. bandwidth signals with up to 32 UI duration of the same bit values (LSB and MSB).
- An alternate long pattern is to used 64UI lengths instead of 32UI lengths.

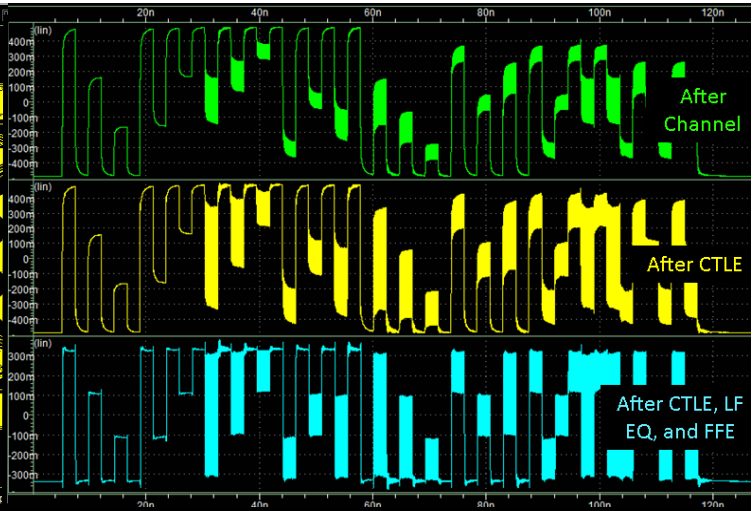


CLTE Only

CLTE and Low Freq De-emphasis
No Pre/Post taps



CLTE, LF De-emphasis, and FFE



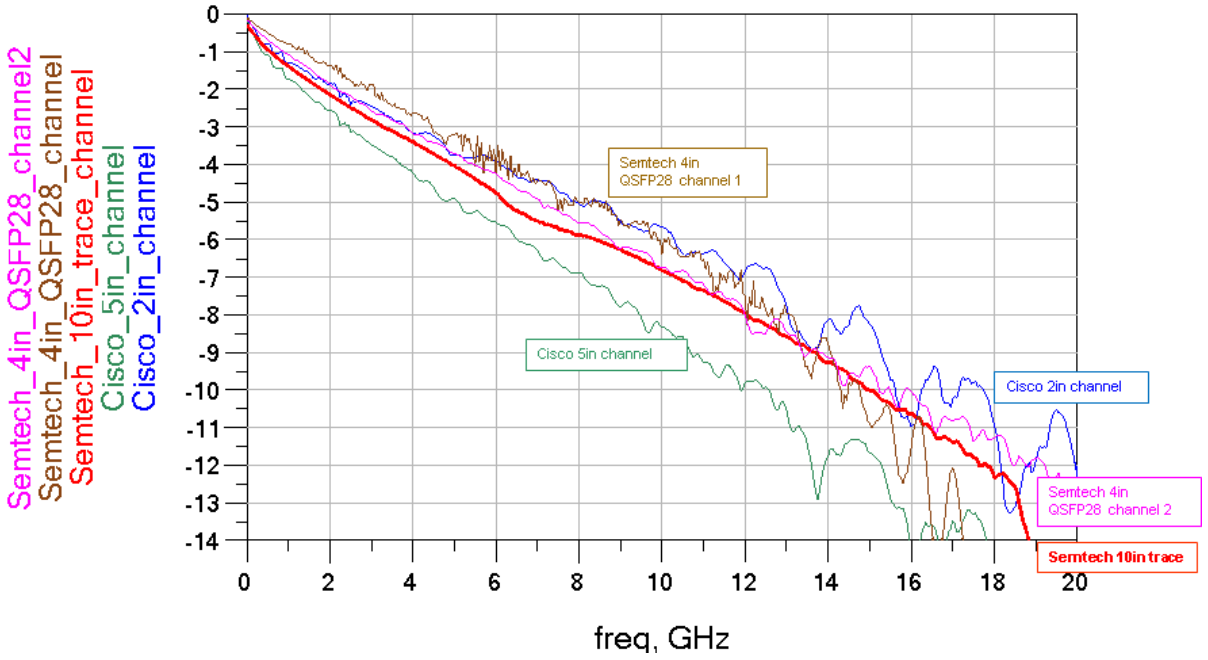
Channel 56Gbps PAM-4, Long Pattern Waveforms

Highlights of oif2015.350.01 (Tailor).

Five channels investigated

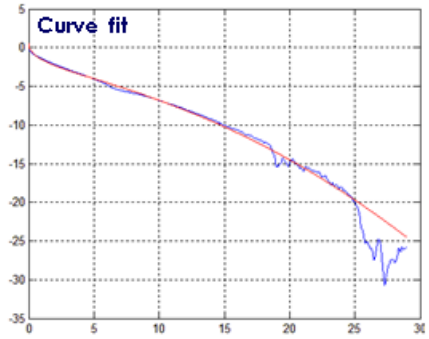
- 3 Semtech channels – a 10in stripline Meg6 trace and two 4in QSFP28 VSR channels
- 2 Cisco channels - one of Cisco 2in and 5in channels each

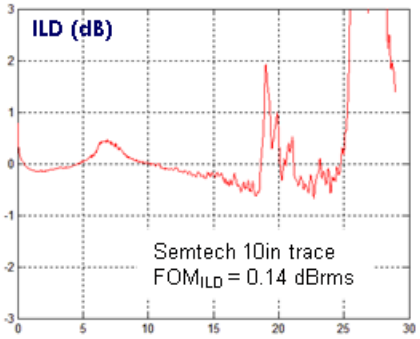
Various equalization approaches were studied including the standard 1z/2p CTLE as well as various 2z/3p CTLEs and a 3-tap FIR.



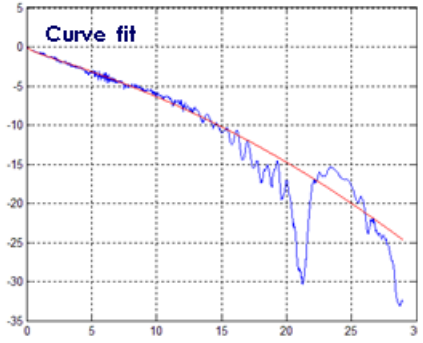
Simulation Parameter	Value
Tx Diff Volt	800 mVpp
PAM4 baud rate	29.0 GBd
Data pattern	PRBS15
EOJ	0.005 UIpp
Tx BUJ	0.05 UIpp
Random jitter	0.005 UIrms
Tx SNDR	29 dB

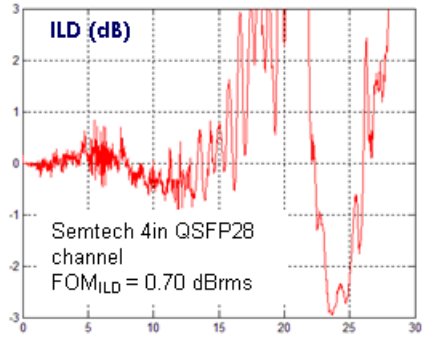
Highlights of oif2015.350.01 (Tailor).



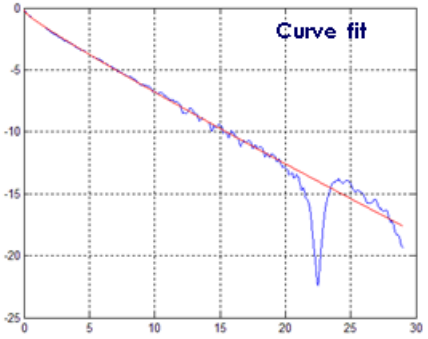


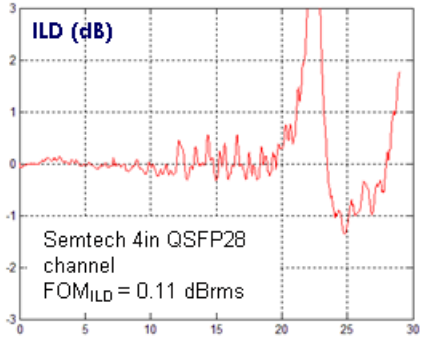
Semtech 10in strip line trace.



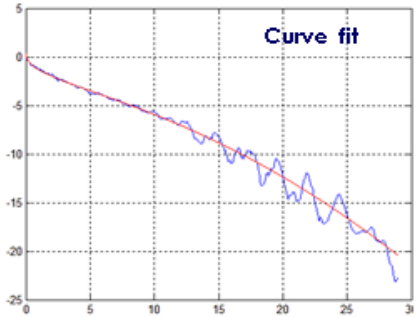


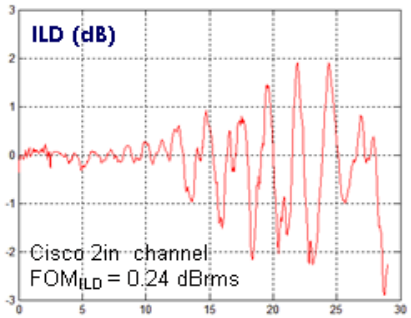
Semtech4in QSFP28 channel 1.



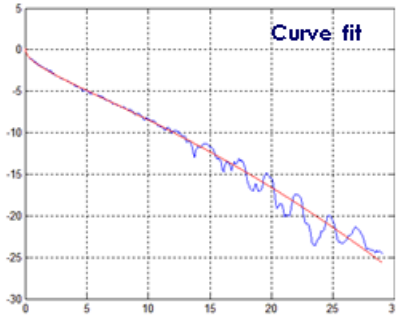


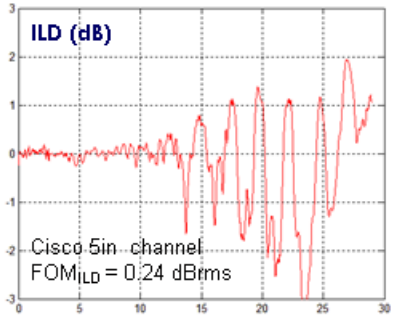
Semtech4in QSFP28 channel2.





Cisco 2in QSFP28 channel.





Cisco 5in QSFP28 channel.

Highlights of oif2015.350.01 (Tailor).

Case - channel	ILD rms	Tx FIR	Rx CTLE	Meet 2p1z freq of reference equalizer	Cross Talk	Veye (mVpp)	Heye (UIpp)
Semtech 10in trace	0.14 dBrms	None	1z (4.5GHz), 2p (15.0, 20. GHz)	No	No	56.8	0.316
		[-0.05 0.95]	1z (4.5GHz), 2p (15.0, 20. GHz)	No	No	70.1	0.336
		[-0.10 0.90]	1z (4.5GHz), 2p (15.0, 20. GHz)	No	No	69.4	0.307
		[-0.05 0.95]	2z (4.5 15.0 GHz) 3p (12.0 23.0 25.0 GHz)	No	No	64.8	0.36
Cisco 2in QSFP28 chan (stacked connector)	0.24 dBrms	None	1z (5.0GHz), 2p (15.0, 20. GHz)	No	No	56.3	0.27
		[-0.05 0.95]	2z (8.75 8.75GHz) 3p (15.0 20.0 20.0 GHz)	n.a.	No	45.2	0.293
Cisco 5in QSFP28 chan (stacked connector)	0.24 dBrms	[-0.10 0.90]	1z (4.0GHz), 2p (15.0, 20. GHz)	No	No	34.6	0.263
		[-0.08 0.68 -0.24]	None	n.a.	No	45.3	0.27
Semtech 4in QSFP28 chan 1	0.7 dBrms	[-0.07 0.93]	1z (4.5GHz), 2p (15.0, 20. GHz)	No	No	48.3	0.254
Semtech 4in QSFP28 chan 2	0.11 dBrms	[-0.07 0.93]	1z (4.5GHz), 2p (15.0, 20. GHz)	No	No	75.1	0.328

A standard 1z/2p CTLE should be adequate for most expected VSR channels in the host-to-module direction

- A 2-tap FIR in the host with some small pre-cursor de-emphasis can help to provide additional system margin.

A channel at maximum VSR loss with higher ILD may require one of:

- Multi-tap FIR

  This should not be mandatory for 56G-VSR-PAM4 as it is not the only option and forces too narrow a solution space.
- **Higher performance reference CTLE**

  This needs further study but is likely the preferable solution to minimize module power

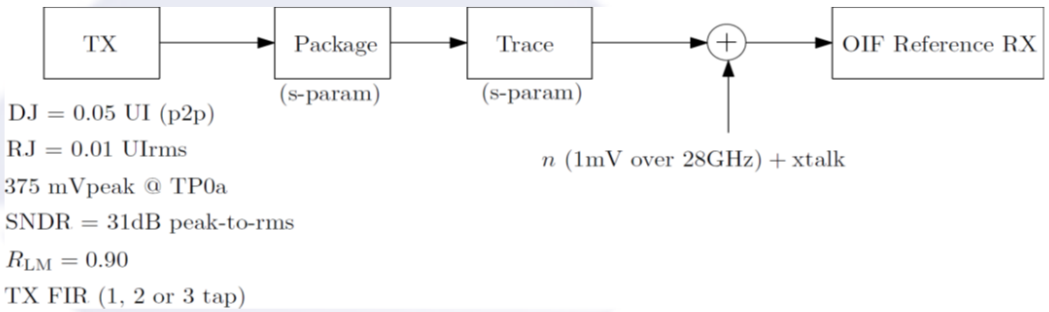
Highlights of oif2015.332.01 (Dallaire, Smith, Marlett).

- Investigated the dependence of link margin on the transmitter specifications.
  Link margin calculator based on the Channel Operating Margin (COM) used by IEEE 802.3bj/bs.
  Appropriately adapted, it is used to evaluate Eye Opening at TP1 for the reference receiver.
- For higher loss channels (~10dB), a TX FIR improves the vertical eye opening (VEO) at TP1 by ~ 2 dB.
  In the absence of a TX FIR, link margins on higher loss channels are insufficient
  Most of the gain of the TX FIR comes from the pre-cursor tap
  Recommend the adoption of a mandatory 2-tap (pre, cursor) TX FIR at minimum

	FEXT	NEXT	IL @ 14GHz (dB)
From IEEE 802.3bs shanbhag_3bs_14_0623:			
Nelco 4000-13SI Host PCB + next gen 28Gb/s high density SMT IO	5	0	9.33
EM-888 Host PCB + next gen 28Gb/s press-fit stacked IO	7	0	9.27
From IEEE 802.3bs shanbhag_3bs_01_1014:			
4in Megtron6 Host PCB + next gen 28Gb/s high density SMT IO	5	0	4.70
10in Megtron6 Host PCB + next gen 28Gb/s high density SMT IO	5	0	9.42
4in Megtron6 Host PCB + next gen 28Gb/s press-fit stacked IO	7	0	4.64
10in Megtron6 Host PCB + next gen 28Gb/s press-fit stacked IO	7	0	9.35

System Model

- 28.2 Gbaud PAM4
  - Reference RX zeros/poles scaled for 28.2GBaud



- A simulator based on the COM program is used to evaluate the link margin of the system
  - Target SER=1E-6

Highlights of oif2015.332.01 (Dallaire, Smith, Marlett).

Host Transmitter Specification @ TP0a

- For illustration, we calculate the link margins (VEO) at TP1 with perfect "linearity" (i.e., R_{LM}=1), SNDR=27 dB, RJ=5 mUIrms, and without a TX FIR

Channel Trace	VEO (dB)
TEC_10_2014_C2M_10in_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	0.18
TEC_10_2014_C2M_4in_Channel_Next_Gen_28Gbps_high_density_SMT_IO	2.03
TEC_10_2014_C2M_10in_Channel_Next_Gen_28Gbps_high_density_SMT_IO	0.14
TEC_10_2014_C2M_4in_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	1.83
TEC_23_06_2014_C2M_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	0.39
TEC_23_06_2014_C2M_Channel_Next_Gen_28Gbps_high_density_SMT_IO	0.26

- Meeting the TP0a informative spec is not nearly sufficient to close the link!

Sensitivity Analysis

- TX FIR: 1, 2, or 3 taps?
  - SNDR = 31 dB; RJ = 10 mUIrms; R_{LM} = 0.9

- TX FIR provides ~2dB margin improvement in higher loss channels!
- The majority of the improvement comes from adding a pre-cursor tap
  - It may be sufficient to require a 2-tap TX FFE with three settings (e.g., [0,1], [-0.05,0.95],[-0.1,0.9])

	VEO (dB)		
Channel Trace	1-Tap TX FIR	2-Tap TX FIR	3-Tap TX FIR
TEC_10_2014_C2M_10in_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	0.76	2.84	3.22
TEC_10_2014_C2M_4in_Channel_Next_Gen_28Gbps_high_density_SMT_IO	3.41	3.67	4.15
TEC_10_2014_C2M_10in_Channel_Next_Gen_28Gbps_high_density_SMT_IO	0.72	2.43	2.68
TEC_10_2014_C2M_4in_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	3.11	4.38	4.38
TEC_23_06_2014_C2M_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	1.10	2.78	3.20
TEC_23_06_2014_C2M_Channel_Next_Gen_28Gbps_high_density_SMT_IO	0.89	2.48	2.48

Highlights of oif2015.332.01 (Dallaire, Smith, Marlett) with added results over Cisco QSFP28 reference card.

- Proposed the following revisions to the TP0a specifications:
  - SNDR = 31 dB (minimum); (Currently 27 dB)
  - RJ <= 10 mUIrms; (Currently 5 mUIrms)
  - Level Linearity R_{LM} >= 0.9; (Currently Eye Linearity=1.5, which is equivalent to R_{LM} >= 0.855)
  - Mandatory 3-tap TXFFE.

Channel Trace	VEO (dB)	ILD (dBrms)	IL (@14G)
TEC_10_2014_C2M_10in_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	3.22	0.052	9.4
TEC_10_2014_C2M_4in_Channel_Next_Gen_28Gbps_high_density_SMT_IO	4.15	0.110	4.7
TEC_10_2014_C2M_10in_Channel_Next_Gen_28Gbps_high_density_SMT_IO	2.68	0.106	9.4
TEC_10_2014_C2M_4in_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	4.25	0.051	4.6
TEC_23_06_2014_C2M_Channel_Next_Gen_28Gbps_press_fit_stacked_IO	3.20	0.051	9.3
TEC_23_06_2014_C2M_Channel_Next_Gen_28Gbps_high_density_SMT_IO	2.29	0.110	9.3
Cisco_2_in_Stacked_rx2_top_short_bcm_hcb	**2.19**	**0.237**	**8.2**
Cisco_5_in_Stacked_rx2_top_short_bcm_hcb	**1.47**	**0.245**	**11.4**

For the above transmitter specs, results for the Cisco board are added to the existing results of oif2015.332.01

- Even with a TX FIR, the VEO for the Cisco board traces are insufficient
- The large ILD of the traces is especially problematic for PAM4, due to much greater sensitivity to residual ISI.
  - **For the four TEC channels with loss greater than 9 dB, and the 5" Cisco channel, the calculated VEOs are strongly correlated with ILD.**
  - **The greater ILD of the Cisco board is a significantly greater cause of margin degradation than the higher insertion losses.**

Summary of OIF contributions.

- Experiments and simulations were run by three different companies over the same reference channels, based on Cisco QSFP28 reference card.
  - This card is representative of a potential worst-case design for CDAUI-8 applications.
  - Return loss compliance to current OIF CEI-56G-VSR requirements, which most likely will be adopted as reference channel by CDAUI-8 too.
  - Insertion loss of 3,4 and 5 channels seems higher than current CDAUI-8 proposal (4 and 5 than current CEI-56G-VSR too).

- Current 2p1z CTLE reference receiver equalizer defined for TP1a compliance seems not fulfilling the EH,EW requirements.
  - oif2015.237 and further work - proposed combination of FFE (at TX) and CTLE.
  - Still saying 2p1z CTLE can work (with different poles and zeroes), oif2015.350.01 propose combination of higher order CTLE and/or TX fir for higher ILD channels.
  - oif2015.332.01 and further work - propose to improve TX characteristics, together with TX FIR pre-cursor for high loss traces – shown that high ILD of QSFP28 reference card is great cause of channel degradations.

- Another item to be discussed – Definition of continuos adaptation of module's CTLE RX.

- Currently OIF CEI-56G-VSR-PAM4 requires "Module receiver to be self-adaptive and autonomous".

- This keeps open the opportunity to develop "adaptive at start-up", but then "static" module's receivers, which we believe can have hard life to compensate CDAUI-8 channel variations.
  - Note that this item was already addressed during CAUI-4 definition with a couple of contributions from Cisco (see mazzini_01_042414_caui and alessandro_01_07032014_caui).

- **Since we do expect that channel variations should have worse impact than NRZ on PAM4, we believe there'll be the need of a slow (but continuous) adaptation of the CTLE receiver.**
  - For this CDAUI-8 should include a mention to «continuos» adaptation.
  - Our NEBS/DVT tests assume 2C/min temperature ramp variation, so we should cover these variations with the proposed adaptation method.
  - Our first estimation is +/- 1dB variation with respect to the previous CTLE gain setting with a minimum 1Hz frequency rate, but we're open to discussion.

- Another item to be discussed – Vertical eye closure (VEC) at TP1a.

Table 16-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Eye Width at 10^{-p} probability (EW6)[3]	0.25	-	UI	See Section 16.3.10
Eye Height at 10^{-6} probability (EH6)[3]	50	-	mV	See Section 16.3.10
Eye linearity[4]	-	1.5	-	

3. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) applicable to all three PAM4 eyes
4. Eye linearity = (max(AVupp, AVmid, AVlow) / min(AVupp, AVmid, AVlow))

Table 16-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP1a	900	-	mV	See Section 16.3.11

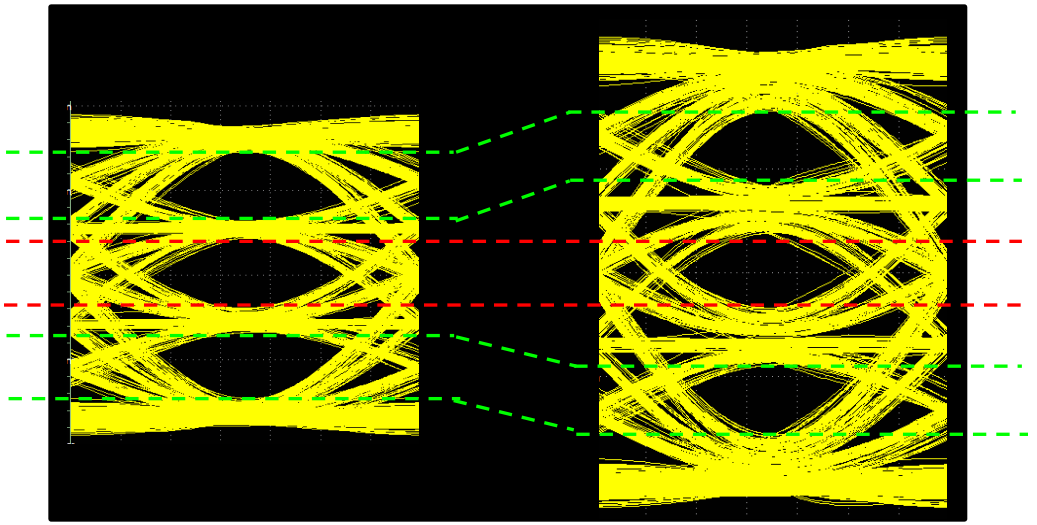
-For TP1a compliance test, at least one of the nine CTLE settings that meets both the EH6 and EW6 settings defined for TP1a in Table 16-1 indicates a pass. As for the TP4 compliance test, at least one of the two CTLE settings that meets both the EH6 and EW6 settings defined for TP4 in Table 16-4 indicates a pass.

At TP1a, passing is defined as a single equalizer setting that meets the EH6 and EW6 specifications defined in Table 16-1 for the lower, upper and middle eyes. At TP4, passing is defined as a single equalizer setting that meets the EH6, EW6 and VEC specifications given in Table 16-4.

$$\mathrm{VEC} = 20 \cdot \mathrm{LOG}\left(\mathrm{Min}\left(\left(\frac{\mathrm{AVupp}}{\mathrm{Vupp}}\right),\left(\frac{\mathrm{AVmid}}{\mathrm{Vmid}}\right),\left(\frac{\mathrm{AVlow}}{\mathrm{Vlow}}\right)\right)\right)$$

Same EW, EH can be achieved with different VEC at TP1a.

Define a maximum VEC at TP1a too would help to constrain host output and calibrate the TP1 input stressor to the CDAUI-8 module.



Options to be considered for CDAUI-8 C2M.

Six items (last one if strickly needed) that should be considered into C2M CDAUI-8, to allow TP1a EW/EH compliance and safe C2M link closure.

1. Define a more complex standard CTLE RX equalizer.
   - 3p2z or better.
   - Introduce a LF filter on the standard reference RX equalizer too?
2. Definition of continuos adaptation of module's CTLE RX.
   - Proposed +/- 1dB variation with respect to the previous CTLE gain setting with a minimum 1Hz frequency rate
3. Introduce a channel ILD deviation mask requirement.
   - Value to be agreed.
4. Improve TP0 TX SNDR requirement.
   - Value to be agreed (from 27 to 29dB ?).
5. Include TP1 VEC requirement.
   - Value to be agreed.
6. Allow "Coarse" host TX pre-cursor tap for long channels only (off for short ones) – this would be a fixed and "static" value.
   - Value and loss range to be eventually defined.
   - Symmetrically the same tap should be needed on module's transmitter too so should be writable by the host into the module.

Back-up slides

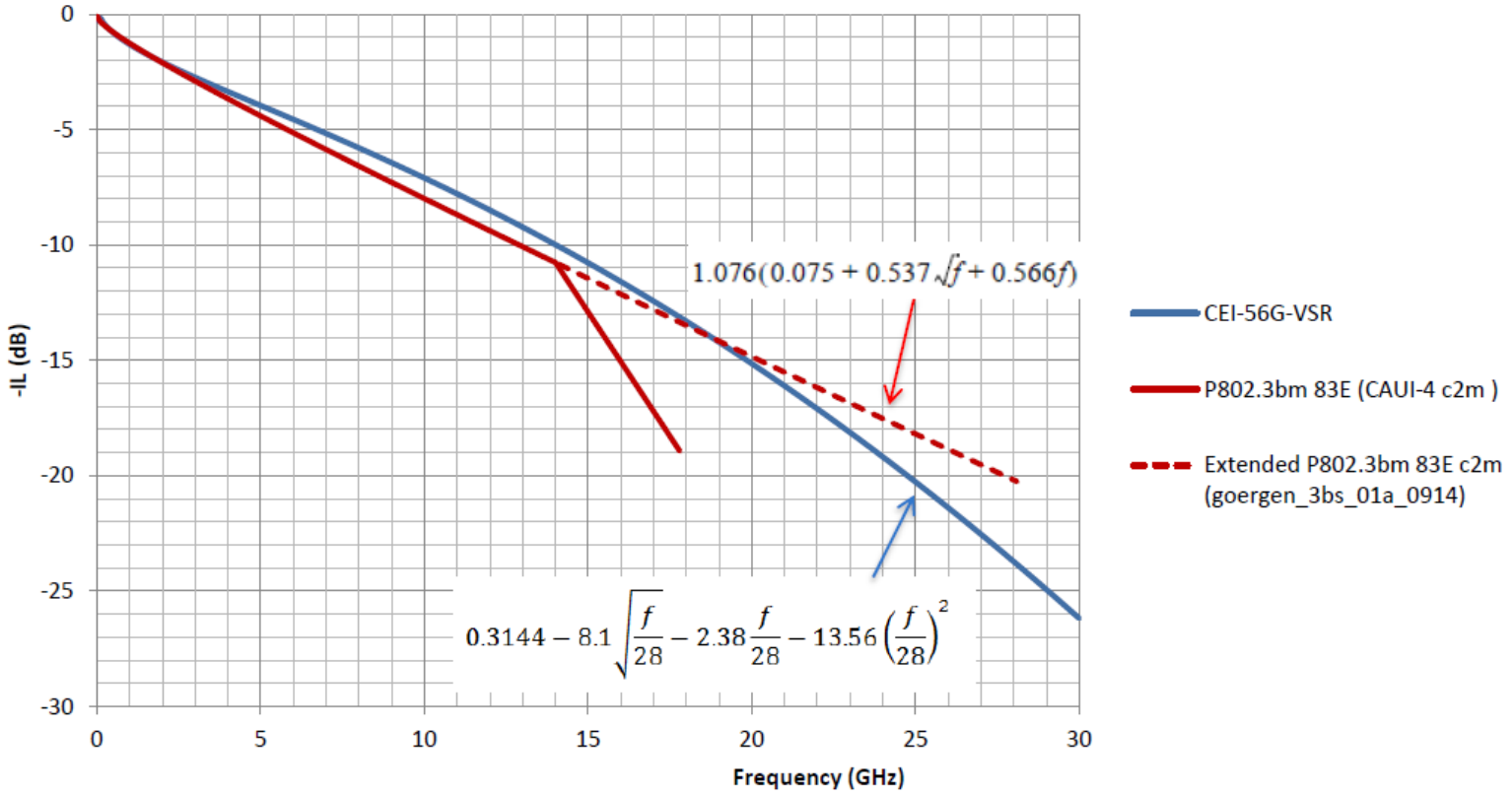
TP1a host output EW/EH P/F and reference equalizer coefficients.

Eye Width at 10^{-6} probability $(EW6)^3$	0.25	-	UI
Eye Height at 10^{-6} probability $(EH6)^3$	50	-	mV

Table 16-8. Reference equalizer coefficients for rate of 29 GBd.

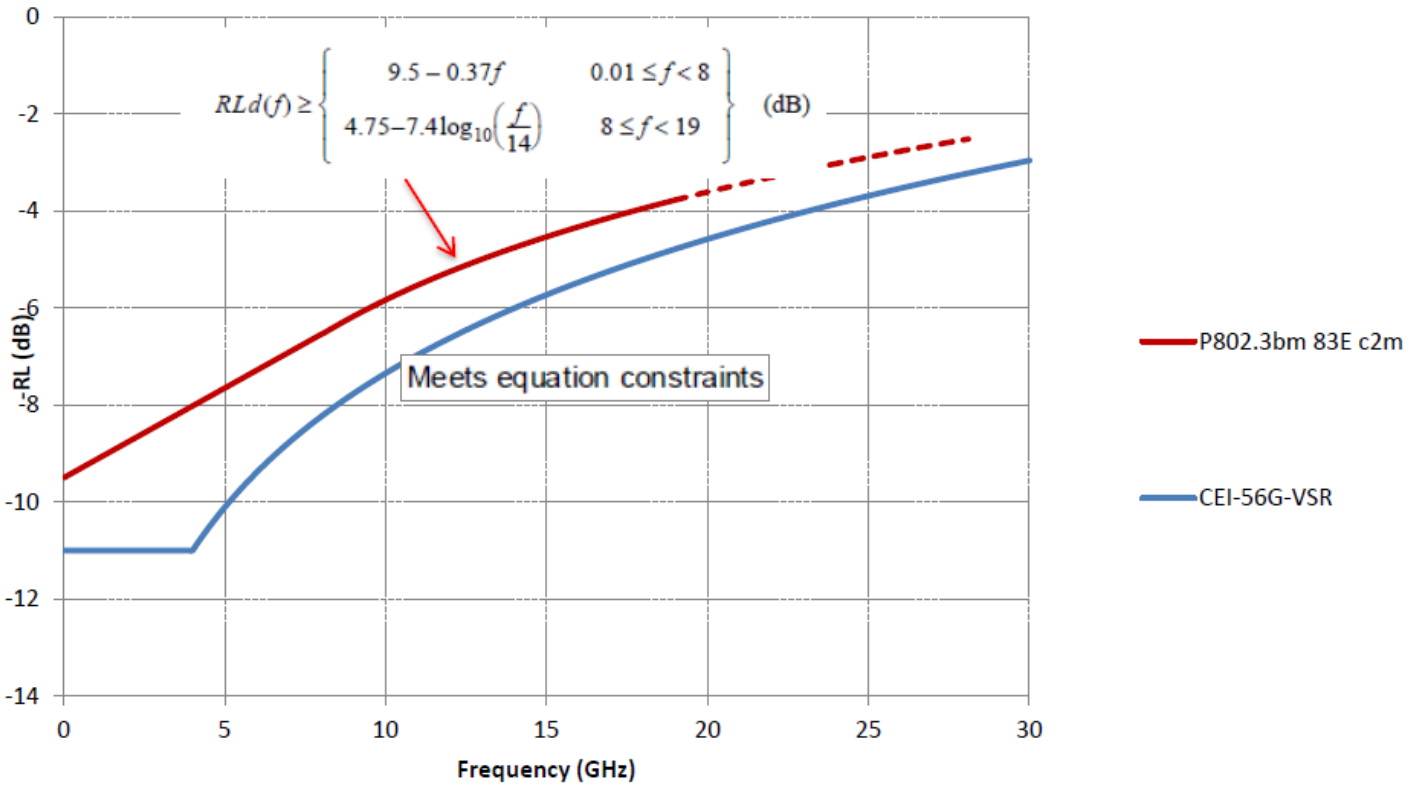
Peaking (dB)	G	P1/2π (GHz)	P2/2π (GHz)	Z1/2π (GHz)
1	0.891	18.6	14.1	8.31
2	0.794	18.6	14.1	7.10
3	0.708	15.6	14.1	5.68
4	0.631	15.6	14.1	4.98
5	0.562	15.6	14.1	4.35
6	0.501	15.6	14.1	3.82
7	0.447	15.6	14.1	3.43
8	0.398	15.6	14.1	3.00
9	0.355	15.6	14.1	2.67

CDAUI-8 c2m PAM4 Channel Insertion Loss



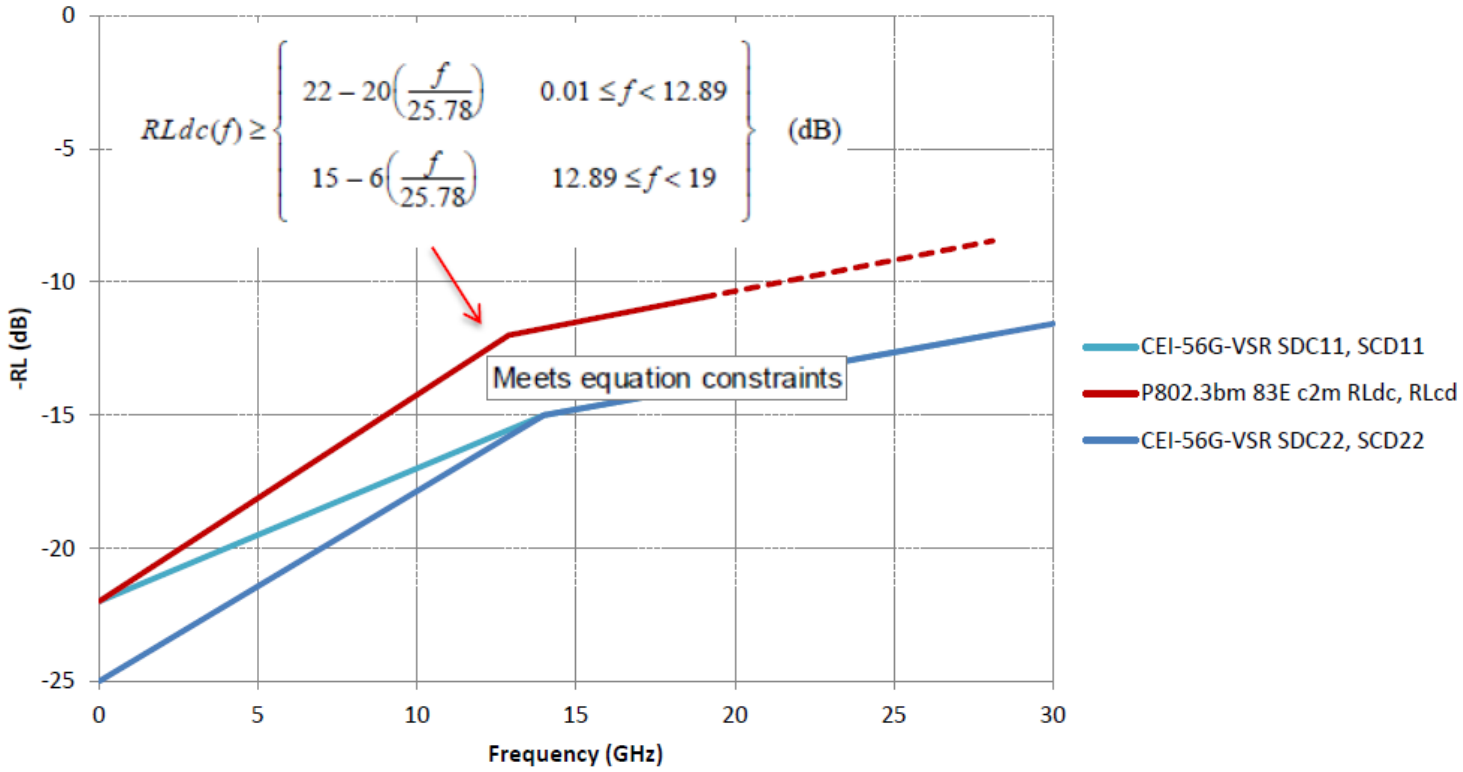
- Target IL curve is "extended CAUI-4 c2m" as adopted at Jan/2015 Interim
  - Loss at Nyquist (13.28GHz) = 10.27 dB
  - Working assumption: all IL curves shown are suitable for PAM4 signaling at 28GBd
  - Consider potential to operate over legacy CAUI-4 c2m channels

CDAUI-8 c2m Tx & Rx Differential Return Loss Spec



- Same as Annex 83E (CAUI-4 c2m)

CDAUI-8 c2m Tx Common-Mode to Differential & Rx Differential to Common-Mode Return Loss Specs



- Same as Annex 83E (CAUI-4 c2m)

Summary

- Baseline proposal using PAM4 signaling for a CDAUI-8 c2m electrical interface specification:
  - Supports CAUI-4 c2m channel
  - Reuses test infrastructures and setup in Annex 83E
  - Is consistent with CEI-56G-VSR draft baseline specification
    - Straightforward to extend/modify Annex 83E specification for PAM4 signaling

5” Channel TX, RX EQ Settings

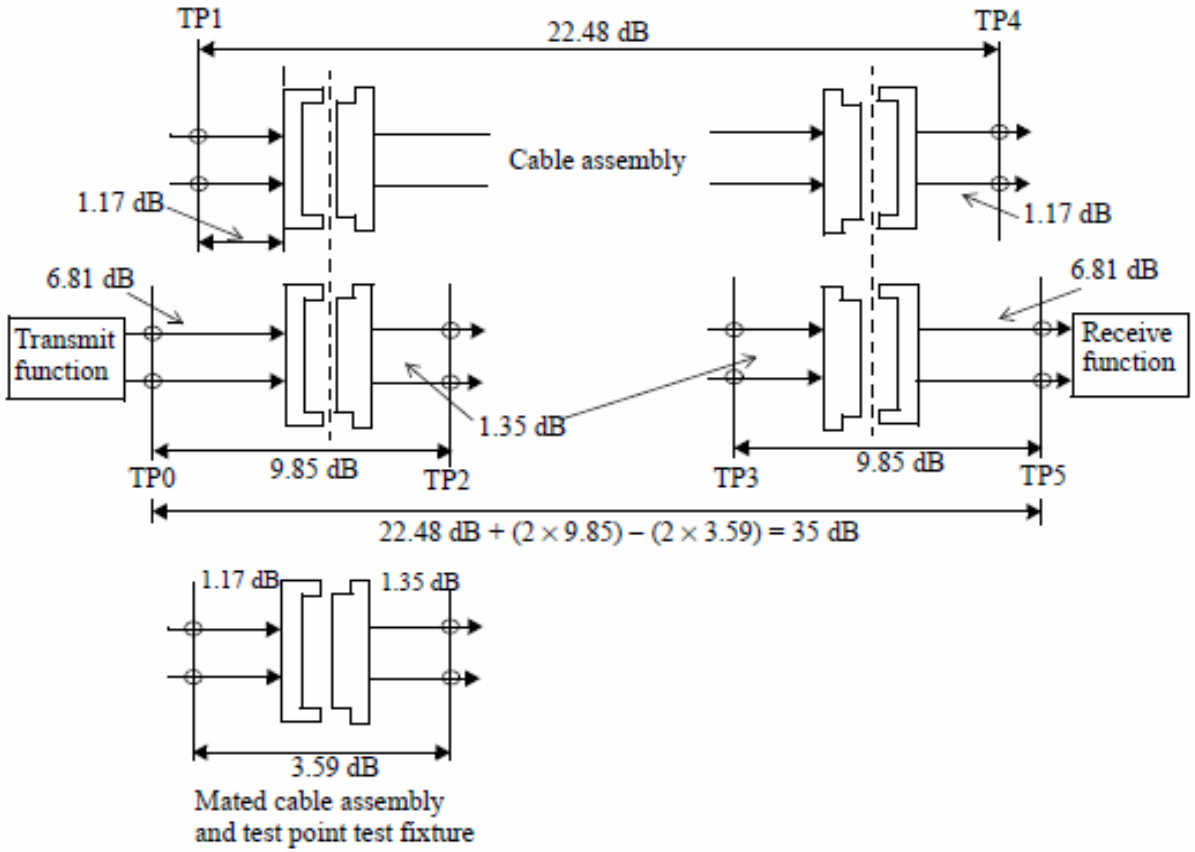
```
* TX FFE, Set to launch 1V pk-pk differential into ideal load
tap_pre2_tx             =0
tap_pre1_tx             =0
tap_main_tx             =1
tap_post1_tx            =0
tap_post2_tx            =0

* RX CTLE
freq_pole1_ctle         =25e9       $ sets the CTLE 1st pole frequency, in Hz
freq_pole2_ctle         =25e9       $ sets the CTLE 2nd pole frequency, in Hz
freq_zero1_ctle         =5e9        $ sets the CTLE 1st zero frequency, in Hz

* RX low frequency deemphasis
_lf_deemph_pct_                     =17         $ the amount of LF de-emphasis gain peaking in percent
_lf_deemph_time_const_              =0.4e-9     $ the time constant of LF de-emphasis

*RX FFE: the main FFE tap weights when FFE is used, otherwise: 0, 0, 1, 0, 0
FFE_pre_tap2_rx         =0.01       $ sets the RX FFE 2nd pre cursor tap value, in volts
FFE_pre_tap1_rx         =-0.1       $ sets the RX FFE 1st pre cursor tap value, in volts
FFE_main_tap_rx         =1          $ sets the RX FFE main tap value, in volts
FFE_post_tap1_rx        =0.04       $ sets the RX FFE 1st post cursor tap value, in volts
FFE_post_tap2_rx        =-0.0       $ sets the RX FFE 2nd post cursor tap value, in volts
```

Channel Compliance points



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 92A–2—35 dB channel insertion loss budget at 12.8906 GHz

Channel Compliance points

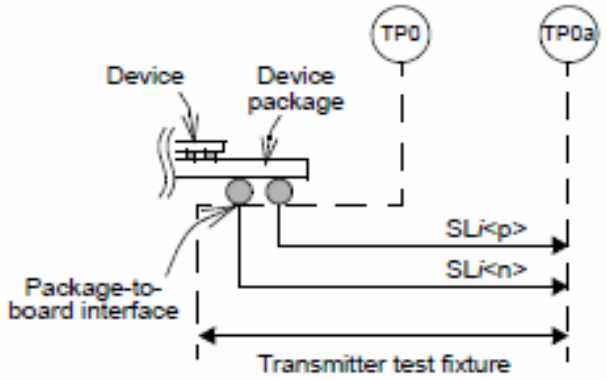


Figure 93–5—Transmitter test fixture and test points

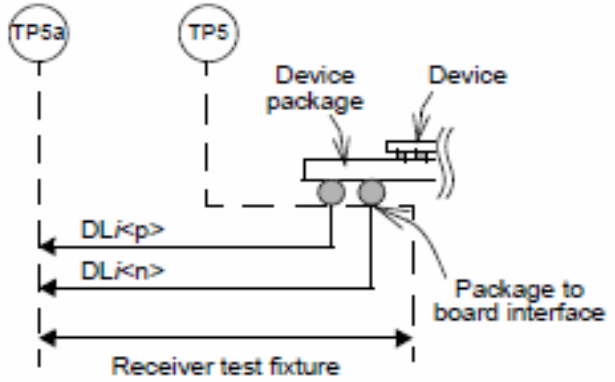


Figure 93–10—Receiver test fixture and test points

Host-to-Module Electrical Specifications at TP0a

Note: A 2 tap FIR filter may be advantageous in meeting the TP1a requirements.

Table 16-9. Host-to-Module Electrical Specifications at TP0a

Parameter	Symbol	Min.	Max.	Units	Conditions
Baud Rate		19.5	28.0	GBd	
Differential Voltage, pk-pk	T_Vdiff	800	-	mV	Note 1
DC Common Mode Voltage	T_Vcm	0	1900	mV	Note 2
Differential resistance	T_Rd	80	120	ohms	
Differential Termination Resistance Mismatch	T_Rdm	-	10	%	at 1 MHz
Differential Return Loss	T_SDD22	-		dB	
Transition Time: 20 to 80%	T_tr, T_tf	10	-	ps	
Common-mode return loss				dB	
Common Mode Noise, RMS	T_Ncm	-	12	mV	See 12.3
Output waveform					
Level separation mismatch ratio, R_{LM}		0.92		-	
Steady-state voltage, v_f		0.4	0.6	V	
Linear fit pulse peak		$0.85*v_f$		V	
Normalized coefficient step size		0.0083	0.05	-	
Pre-cursor full-scale range		1.54		-	
Post-cursor full-scale range		4		-	
Output Jitter and Linearity					
Clock random jitter			0.005	UI_{RMS}	

Table 16-9. Host-to-Module Electrical Specifications at TP0a

Parameter	Symbol	Min.	Max.	Units	Conditions
Clock deterministic jitter			0.05	UI	
Even-odd jitter			0.019	UI	
Signal-to-noise-and-distortion ratio			27	dB	

Notes 1:Max voltage is limited by specifications at TP1a. Minimum voltage can be lower for low loss channels.

Note 2: Load type 0 with min. T_Vdiff, AC-Coupling or floating load.

Module-to-Host Electrical Specifications

Table 16-4. Module-to-Host Electrical Specifications at TP4 (module output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage, pk-pk	-	900	mV	
Common Mode Voltage (Vcm)[1,2]	-350	2850	mV	
Common Mode Noise, RMS	-	17.5	mV	See Section 16.3.5
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz
Differential Return Loss (SDD22)[3]	-	See Equation 16-2	dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)[3]	-	See Equation 16-4	dB	
Common Mode Return Loss (SCC22)[3]	-	-2	dB	From 250 MHz to 29 GHz
Vertical Eye Closure (VEC)	-	5.8	dB	See Section 16.3.10.1.1
Eye Width at 10^{-6} probability (EW6) applicable to all three PAM4 eyes	0.40	-	UI	See Section 16.3.10
Eye Height at 10^{-6} probability (EH6) applicable to all three PAM4 eyes	120	-	mV	See Section 16.3.10
Eye linearity[4]	-	1.5	-	

Note 1: Vcm is defined in Table 1-2 General Definitions of Section 1.6
Note 2: Vcm is generated by the host. Specification includes effects of ground offset voltage.
Note 3: S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
Note 4: Eye linearity = (max(AVupp, AVmid, AVlow) / min(AVupp, AVmid, AVlow))

Table 16-5. Module-to-Host Electrical Specifications (host input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP4	900	-	mV	See Section 16.3.11
Differential Termination Resistance Mismatch	TP4a	-	10	%	
Differential Return Loss (SDD11)[1]	TP4a	-	See Equation 16-2	dB	
Common Mode to Differential conversion and Differential to Common Mode Loss (SDC11, SCD11)[1]	TP4a	-	See Equation 16-3	dB	

Table 16-5. Module-to-Host Electrical Specifications (host input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Stressed Input Test	TP4	See Section 16.3.10.3.1	-		See Section 16.3.10.3
Common Mode Voltage[2,3]	TP4a	-0.3	2.8	V	

Note 1: S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
Note 2: Vcm is defined in Table 1-2 General Definitions of Section 1.6
Note 3: Referred to host ground. Common mode voltage is generated by host

Host-to-Module Electrical Specifications

Table 16-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Voltage pk-pk	-	900	mV	
Common Mode Voltage (Vcm)[1]	-350	2850	mV	
Common Mode Noise RMS	-	17.5	mV	See Section 16.3.5
Differential Termination Resistance Mismatch	-	10.0	%	At 1 MHz See Section 16.3.6

Table 16-1. Host-to-Module Electrical Specifications at TP1a (host output)

Parameter	Min.	Max.	Units	Conditions
Differential Return Loss (SDD22)[2]	-	See Equation 16-2	dB	
Common Mode to Differential conversion and Differential to Common Mode Conversion (SDC22, SCD22)[2]	-	See Equation 16-4	dB	
Common Mode Return Loss (SCC22)[2]	-	-2	dB	From 250 MHz to 29 GHz
Common Mode Voltage	-0.3	2.8	V	Referred to host ground
Eye Width at 10^{-6} probability (EW6)[3]	0.25	-	UI	See Section 16.3.10
Eye Height at 10^{-6} probability (EH6)[3]	50	-	mV	See Section 16.3.10
Eye linearity[4]	-	1.5	-	

1. Vcm is defined in Table 1-2 General Definitions of Section 1.6
2. S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω
3. Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE) applicable to all three PAM4 eyes
4. Eye linearity = (max(AVupp, AVmid, AVlow) / min(AVupp, AVmid, AVlow))

Table 16-2. Host-to-Module Electrical Specifications (module input)

Parameter	Test Point	Min.	Max.	Units	Conditions
Overload Differential Voltage pk-pk	TP1a	900	-	mV	See Section 16.3.11
Common Mode Voltage (Vcm)[1,2]	TP1	-350	2850	mV	
Differential Termination Resistance Mismatch	TP1	-	10	%	At 1 MHz See Section 16.3.6
Differential Return Loss (SDD11)[3]	TP1	-	See Equation 16-2	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)[3]	TP1	-	See Equation 16-3	dB	
Stressed Input Test	TP1a	See Section 16.3.10.3.1	-		See Section 16.3.10.3

Note 1: Vcm is defined in Table 1-2 General Definitions of Section 1.6
Note 2: Vcm is generated by the host. Specification includes effects of ground offset voltage
Note 3: S-parameter specifications based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω