Annex 120D Receiver Jitter Tolerance Test Pattern

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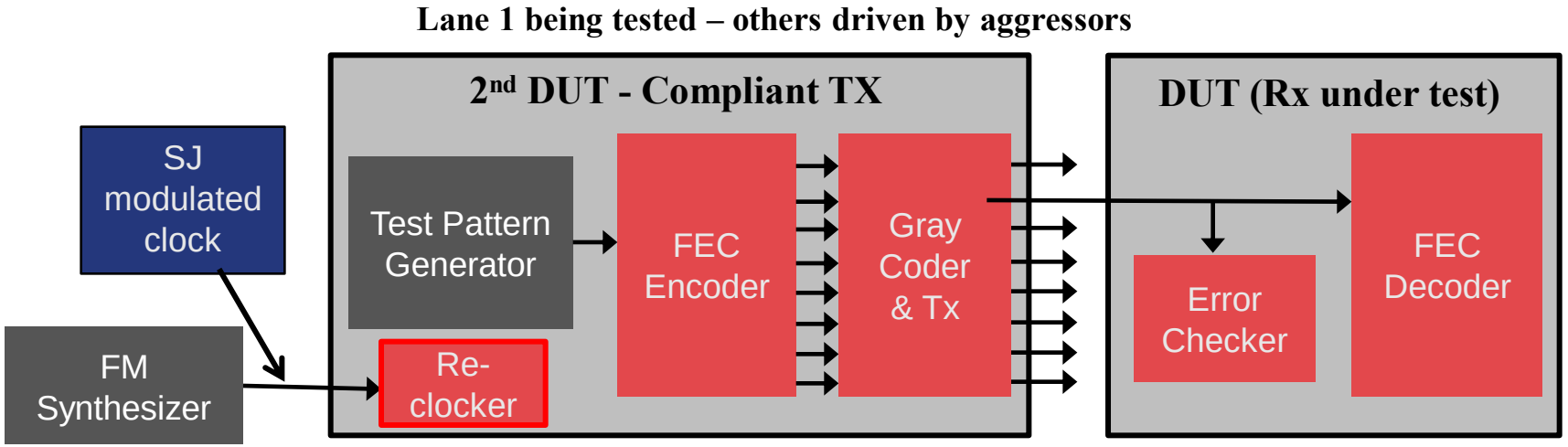
Situation

- The current test pattern called out for the chip to chip jitter tolerance test, 120D.3.2.2, referenced from 119.2.4.9. is:

  “an idle control block (block type=0x1E) with all idles as defined in Figure 82-5. The test pattern is sent continuously and is transcoded, scrambled, alignment markers are inserted and finally encapsulated by the FEC.”

- With the FEC encapsulation, scrambled idle is too long for BERT memory, and not practical to generate in hardware
- Can only be generated by use of compliant DUT Tx
- Compliant DUT Tx can marginally pass enough jitter through for pass/fail compliance test, and not enough for margin test
  - Common problem in 100G-KR4, which uses similar method

Problem with suggested test method



- **Prescribed test setup is marginal for pass/fail compliance test, but cannot test margin in most cases**
- **Reclocker in compliant Tx PLL often similar to CDR design in DUT Rx**
  - **Jitter transfer functions lie on top of each other – compliant Tx can not push enough stress to drive DUT Rx to fail**
- **Chip designers would like to use a BERT for margin testing**
  - **BUT the scrambled idle pattern is too long**
  - **Changing to a shorter test pattern that fits in memory or HW generated would allow use of BERT**

Recommendation

- Receiver Jitter tolerance test can use the same test method as the interference test, but substitute **PRBS31Q** with no FEC in place of scrambled idle for the test pattern
  - The QPRBS and PRBS patterns are generated in hardware in most BERTs
  - Allows compliant pass/fail and margin testing for characterization with simplified stress calibration
- Consider using same PRBS31Q for Interference Tolerance Test (120D.3.2.1) to use common on chip error checker hardware