Update of Bit multiplexing in 400GbE PMA

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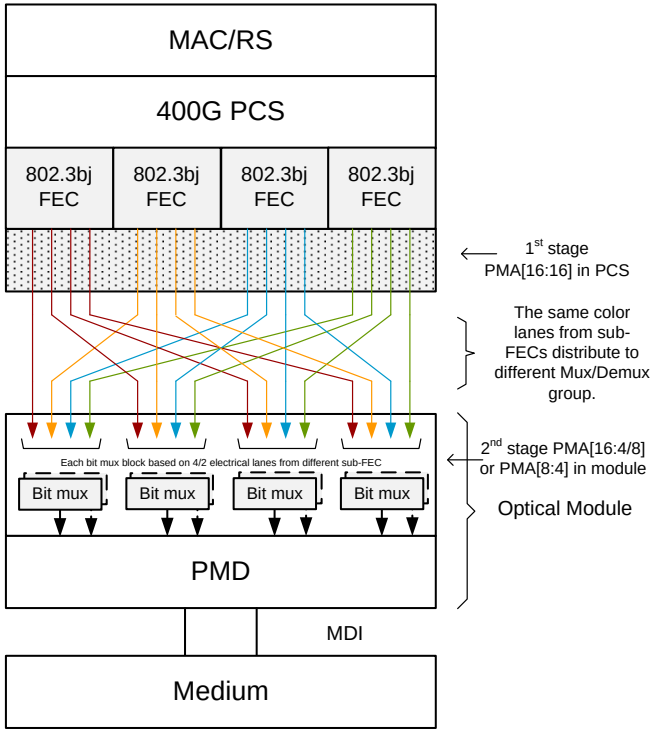
Contributors and Supporters

Motivation

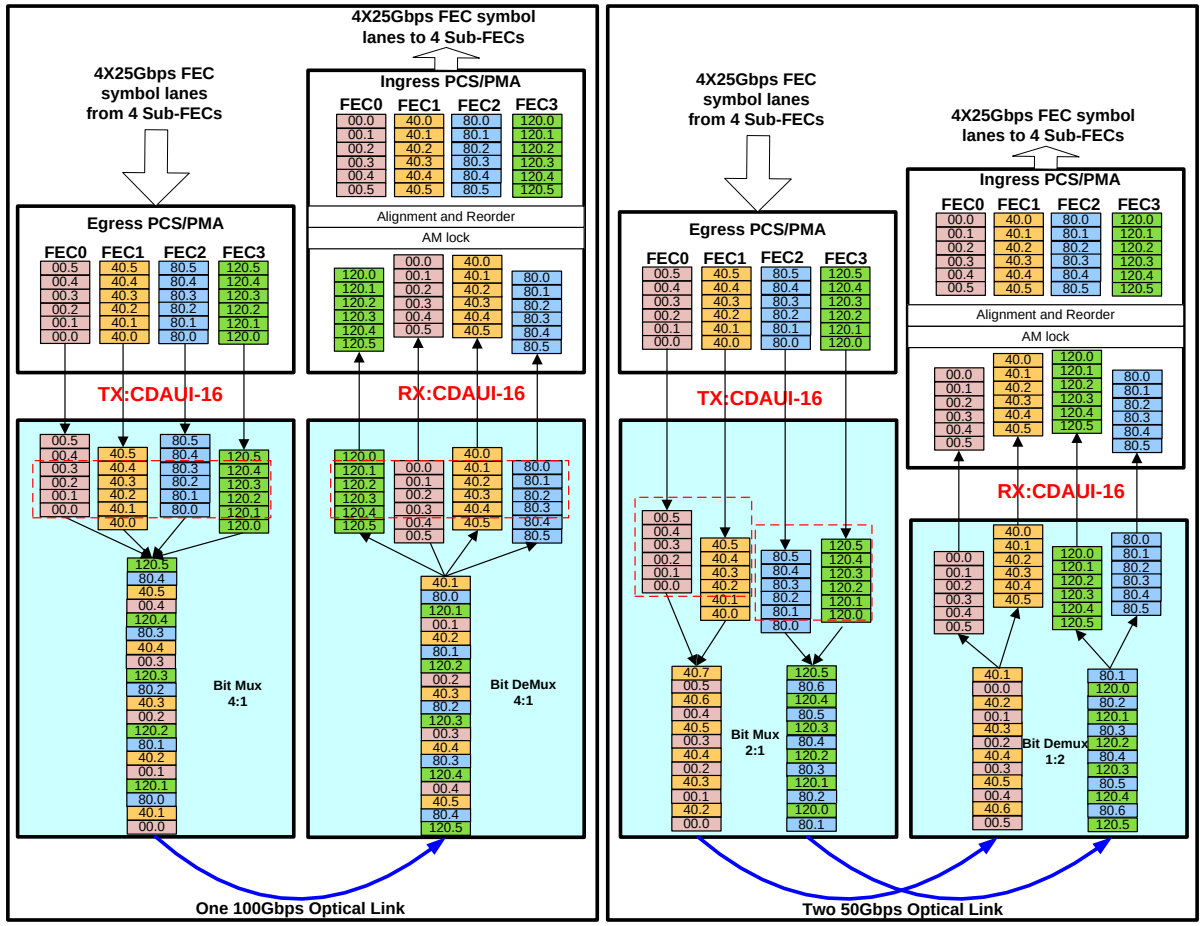
- A bit-multiplexing method based on FOM was presented in January meeting 2014 (*wang_400_01a_0114.pdf*), which enables protocol-agnostic optical modules and empower lower complexity/power/cost & broad market potential



- The following issues are raised during Jan meeting:
  - CDAUI-n interoperation
  - BER/MTTFPA analysis
  - Implementation cost in silicon
- More detailed work on PCS/FEC/PMA architecture with CDAUI-n interoperation is in this contribution.

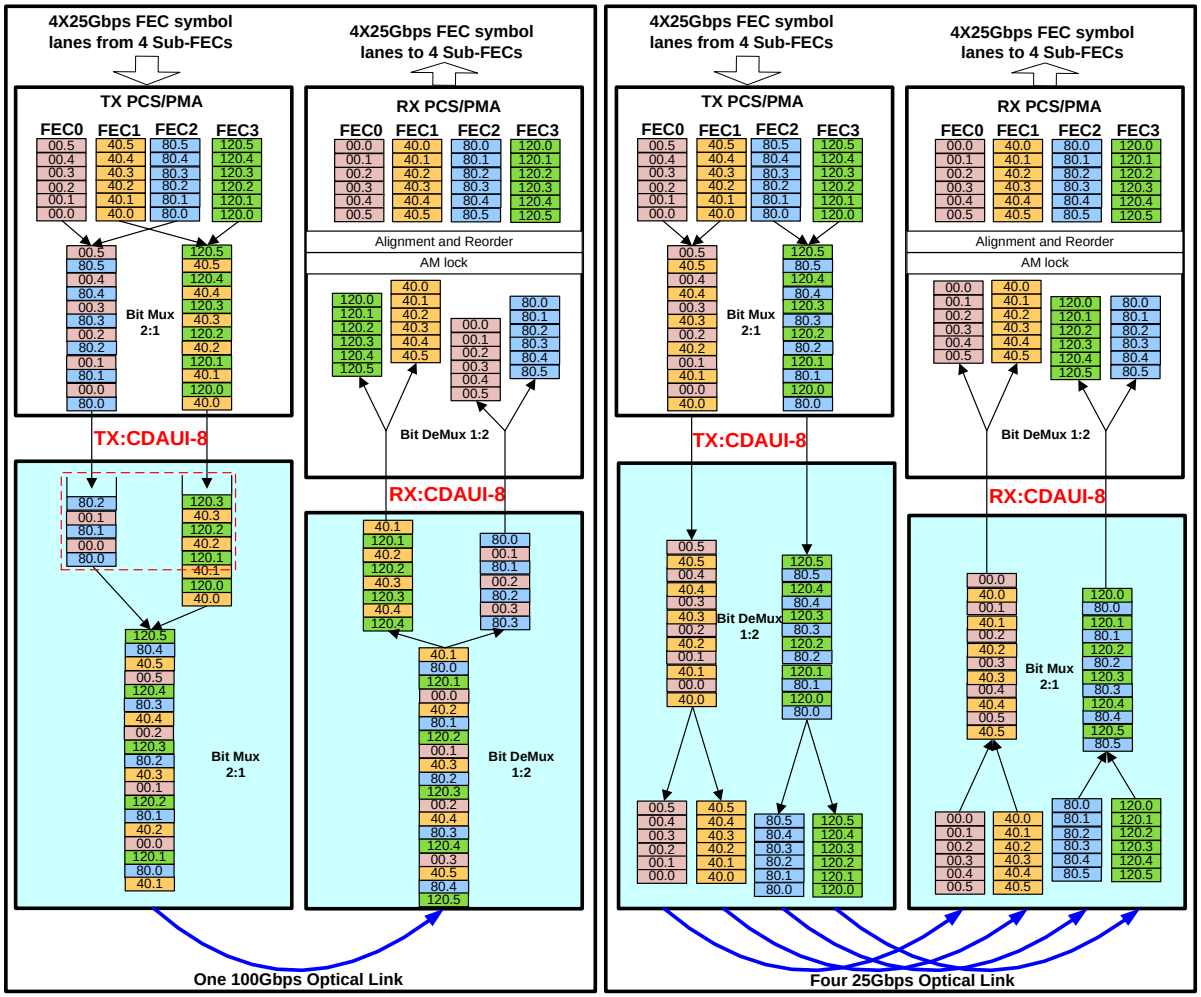
4:1/2:1 bit Mux with CDAUI-16 interface

- Use 16 FEC symbol lanes on CDAUI-16 and 100G/50G optical lane;
- Do 4:1/2:1 bit Mux/Demux from different sub-FECs to fit in 100/50Gbps optical lanes;
- Use AM Lock/Alignment and Reorder on RX side to restore all FEC symbol lanes;
- Have some constraint in SerDes layout design on TX side and no SerDes route order requirement on the RX side.



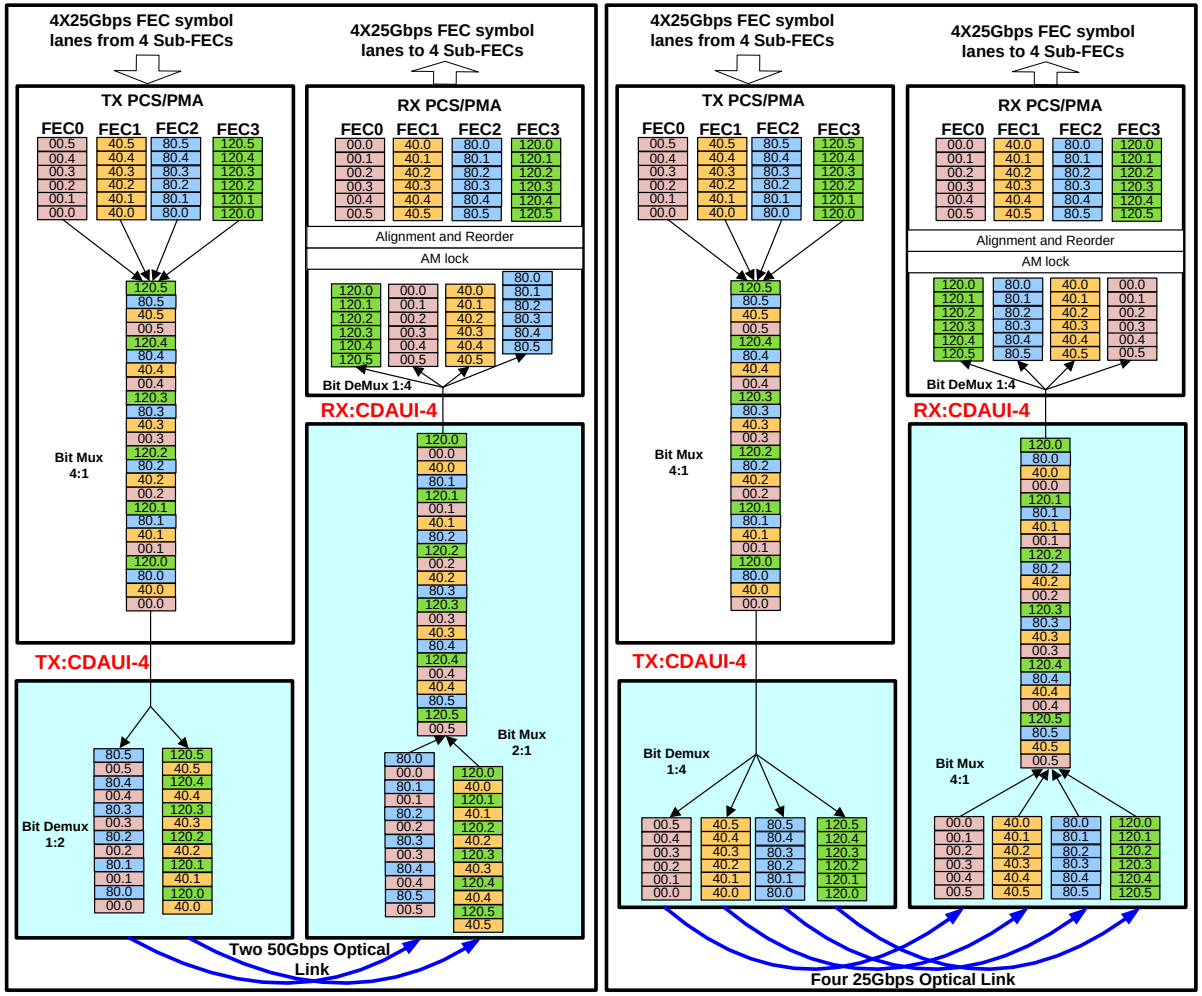
2:1/1:2 bit Mux/DeMux with CDAUI-8 interface

- Take 2:1 FOM Bit Mux/DeMux on each 50G SerDes of CDAUI-8;
- Use 2:1 bit Mux/DeMux based on 2x50G SerDes from different sub-FECs to fit in 100Gbps optical lanes;
- Use 1:2 bit DeMux/Mux for one 50G SerDes from different sub-FECs to fit in 25Gbps optical lanes;
- AM Lock/Alignment and Reorder in the RX side to restore all FEC symbol lanes;
- Have some constraint in SerDes layout design on TX side and no SerDes route order requirement on the RX side.

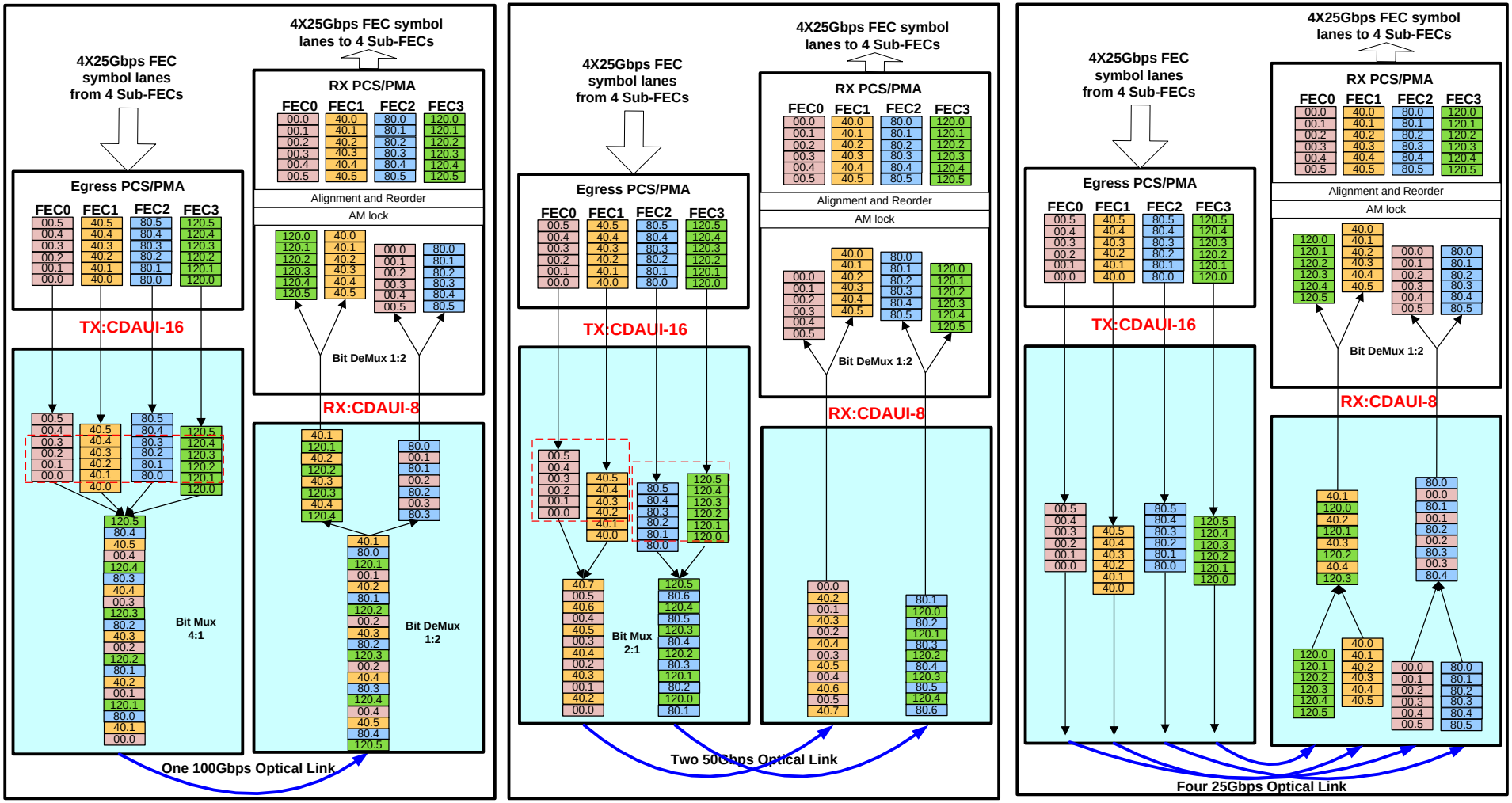


1:2/1:4 bit DeMux with CDAUI-4 interface

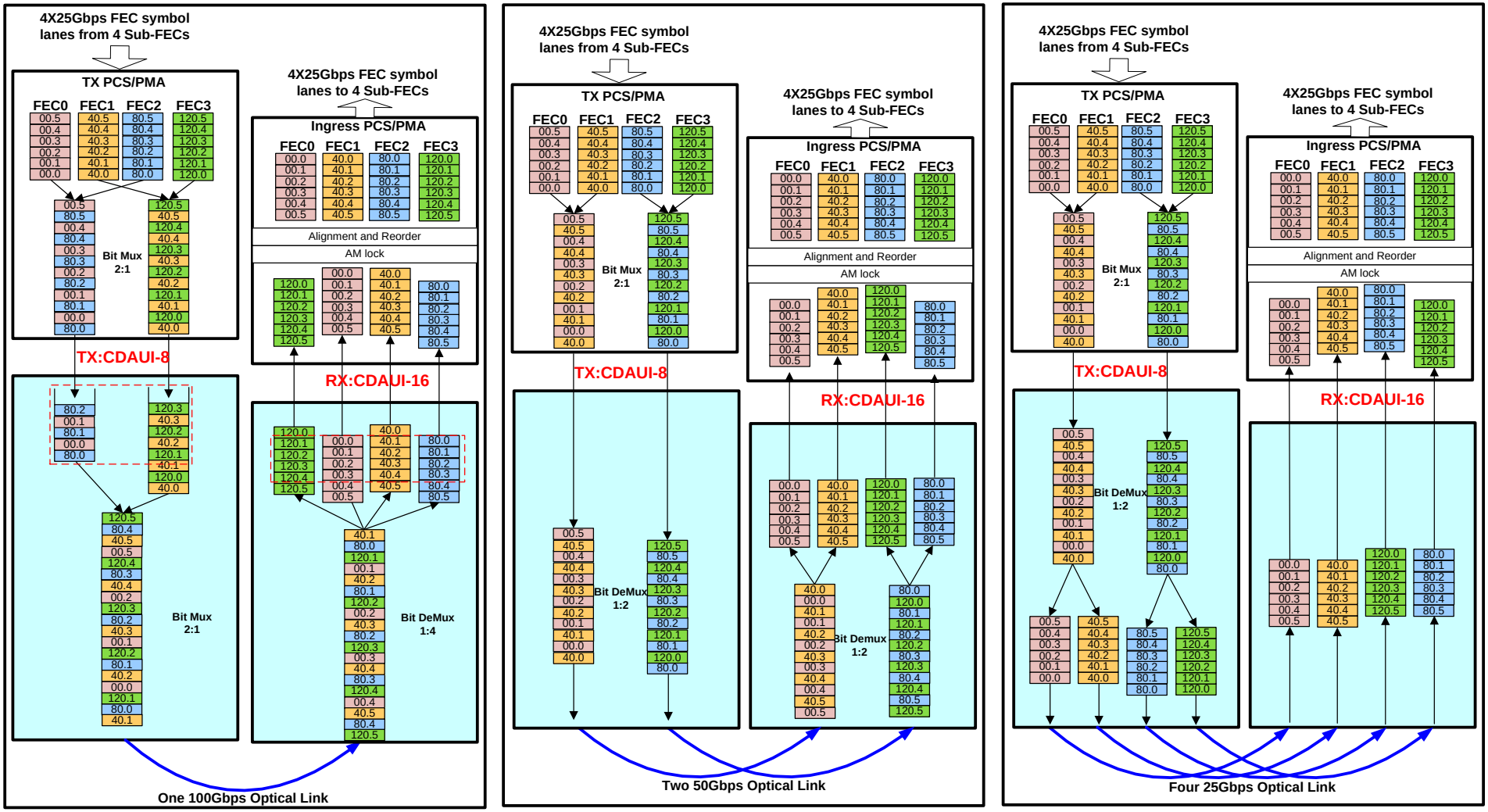
- Take 4:1 FOM Bit Mux/DeMux on each 100G SerDes of CDAUI-4;
- Use 1:2 bit DeMux/Mux for one 100G SerDes from different sub-FECs fitting in 50Gbps optical lanes;
- Use 1:4 bit DeMux/Mux for one 100G SerDes from different sub-FECs fitting in 25Gbps optical lanes;
- AM Lock/Alignment and Reorder in the RX side to recover all FEC symbol lanes;
- No SerDes route order requirement on the TX & RX side.



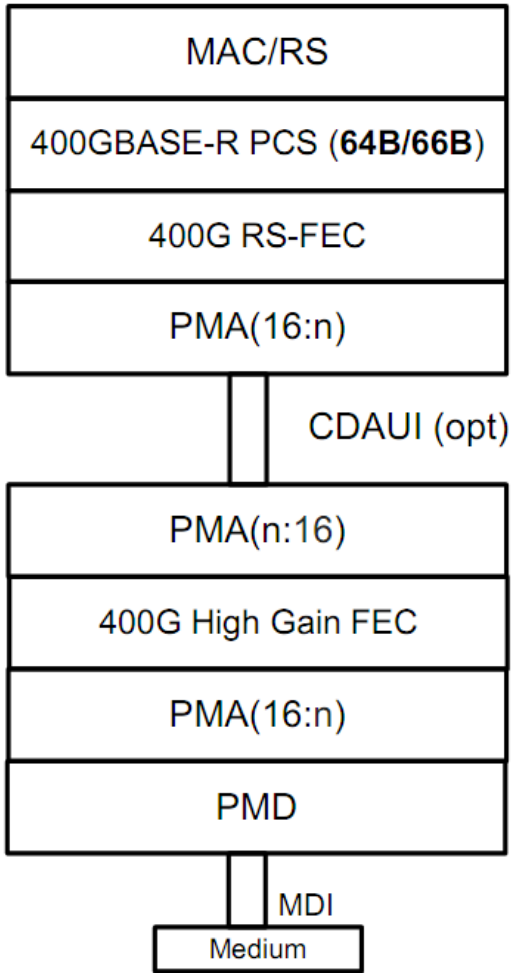
CDAUI-16 TX interoperate with CDAUI-8 RX



TX: CDAUI-8 interoperate with RX: CDAUI-16



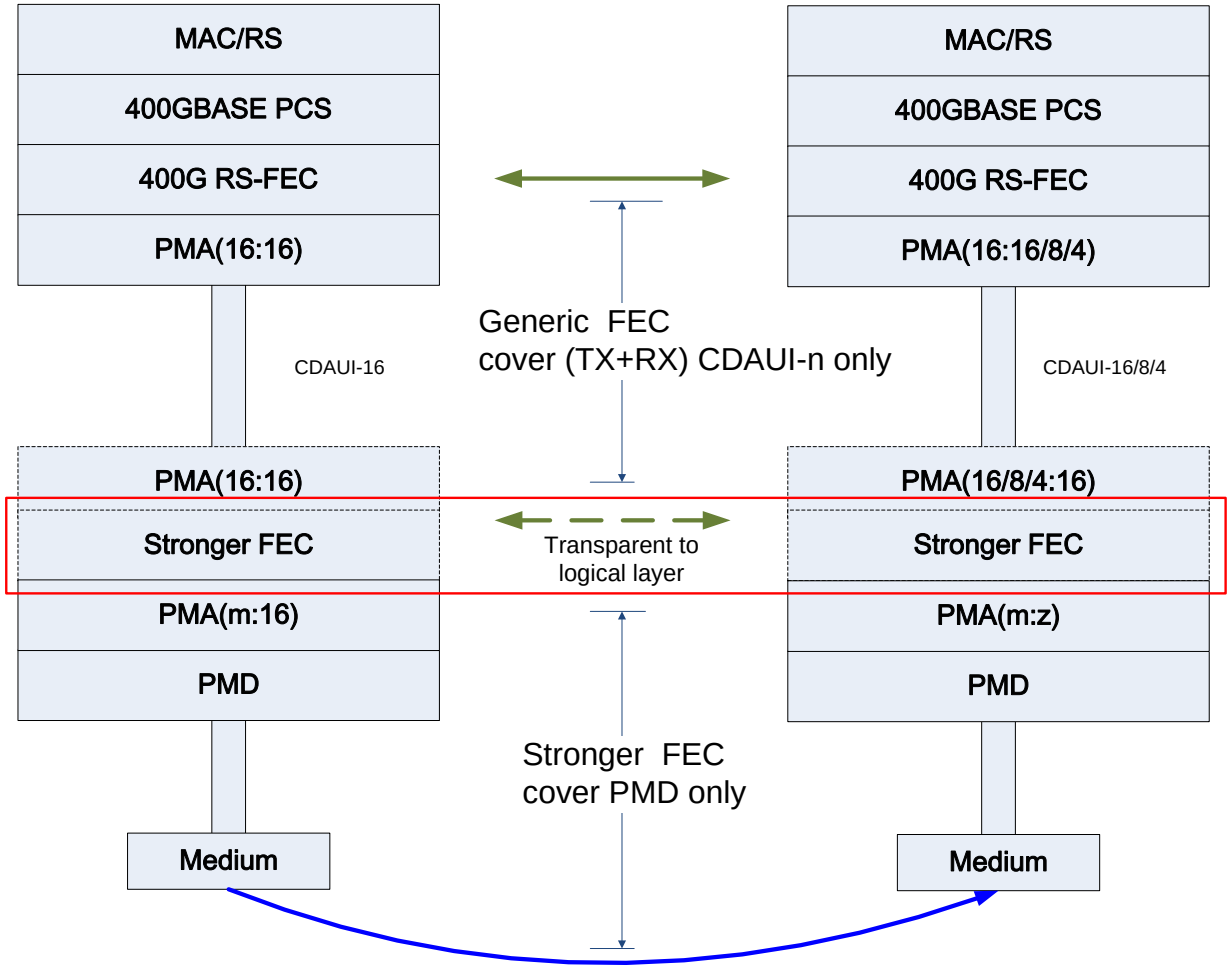
How to support High Gain FEC?



- As discussed In November 2013 Dallas meeting (gustlin_400_01_1113), High Gain FEC in the architecture can be integrated by:
  - Option 1: add the FEC on top of what is already there, no additional transcoding is needed
  - Option 2: strip off the current FEC and then add a stronger FEC to the PCS encoded data.
- With the FOM Bit-Mux proposal and Option1, it is easy to add high gain FEC on top of the FEC encoded data and implement protocol agnostic optical module.
  - If the mandatory generic RS-FEC is RS(528, 514) with transcoding, 0% overclocking in CDAUI interface, there is no need to bypass this generic FEC if High Gain FEC is deployed.
- FOM Bit-Mux proposal also support option 2, where it just can not realize protocol agnostic optical modules anymore. Further iteration FEC for additional gain can be enabled after generic FEC decoding.

CDAUI-n interoperation with High Gain FEC

- One PCS/FEC architecture with FOM bit mux to support CDAUI-16/8/4 interoperation.
- The generic RS FEC should be identical with or without stronger FEC.
- Additional stronger FEC on both sides does not affect the interoperation.
- FOM based bit-mux can support CDAUI-n interoperation with high gain FEC deployed in optical module



Refer to: wang_400_01_1113.pdf

Summary

- Detailed analysis of PMA architecture based on FOM(FEC Orthogonal Multiplexing) bit mux is presented in this contribution
  - The issue of how to do CDAUI-16/8/4 interoperation with FOM and mandatory generic FEC is cleared. This will lead to bit mux protocol agnostic module and lower complexity /power/cost
  - It is also possible to implement protocol agnostic optical module by adding High Gain FEC on top of the architecture
  - Stripping generic FEC and adding High Gain FEC in gearbox will make optical module protocol aware
  - Design of gearbox in module will be simplified by bit mux solution.
  - Bit mux based on FOM can adapt to 16/8/4 physical lanes and is PMD independent, e.g. PAMn/DMT
  - 400GE FOM Bit Mux may have some limitation in certain applications,, for example 4X100GE common design in host side and some 100GE serial PMDs solution

Further Work

- Analyze the cost comparison of complexity/power/area for bit/symbol mux scheme;
- Continue analysis for one dual-mode 1X400GE/4X100GE PMA in host side ASIC;
- Investigate Burst Error model of various PMDs in 400GE;
- MTTFPA analysis;

Thank you

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