

Wander in 400GbE Transcoding Link

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Introduction and Background

- This contribution analyses baseline and clock wander of 64/66B-256/257B transcoding before or after the scrambler

PCS Big Ticket Items

- Slide 11 per gustlin_3bs_02 are work items
 - What FEC will be used, or even possibly multiple FECs
 - 4x100G vs. 1x400G FEC
 - What do AMs look like
 - Details of the scrambling process, exactly what is scrambled and how
 - What muxing is used for each PMA instance
 - Details around EEE operation
 - Adopted EEE baseline in January
- PMD selection influence PCS and FEC
- Need burst error nature to select PCS and FEC
- Error model by PMD type?
 - See slide 5
- Status
 - Many of these issues are being looked at, work in progress

[gustlin_01_0215_logic](#)

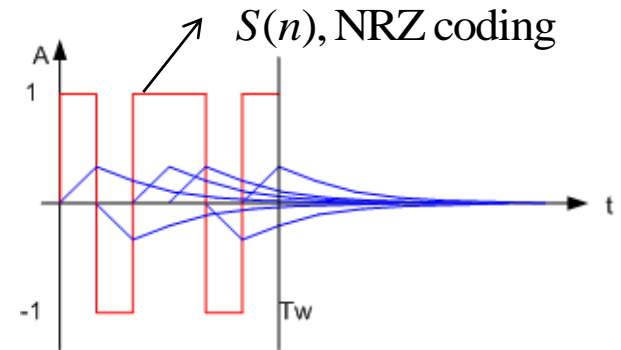
Baseline Wander and Clock Wander

- Baseline wander is the instant offset in the signal on AC **coupled** link. By iteration method, it can be accumulated from last moment, as the wave shows.

$$V_{BLW}(1) = -(1 - e^{-\frac{UI}{T}}) \times S(0),$$

$$V_{BLW}(n+1) = V_{BLW}(n) \times e^{-\frac{UI}{T}} - (1 - e^{-\frac{UI}{T}}) \times S(n),$$

$$UI = \frac{1}{bit_rate}, T = \frac{1}{W_{cutoff}} = \frac{10000}{bit_rate}, e^{-\frac{UI}{T}} \approx 1 - \frac{UI}{T}.$$



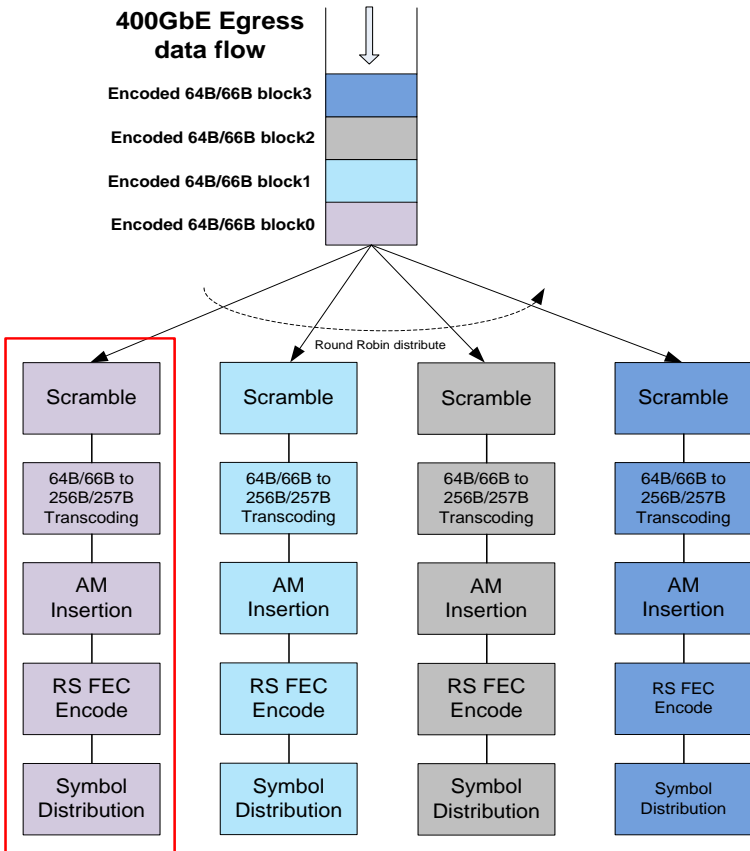
- Clock wander is the low frequency part of the bit transition stream $X(i)$, in which 1 stands for transition and 0 for no transition. For NRZ coding, $1 \rightarrow -1$ and $-1 \rightarrow 1$ mean transition; $1 \rightarrow 1$ and $-1 \rightarrow -1$ indicate no transition. So clock wander can be extracted by RC LPF circuit. Here $Y(i)$ is the clock wander:

$$Y(i) = \alpha \times X(i) + (1 - \alpha) \times Y(i - 1),$$

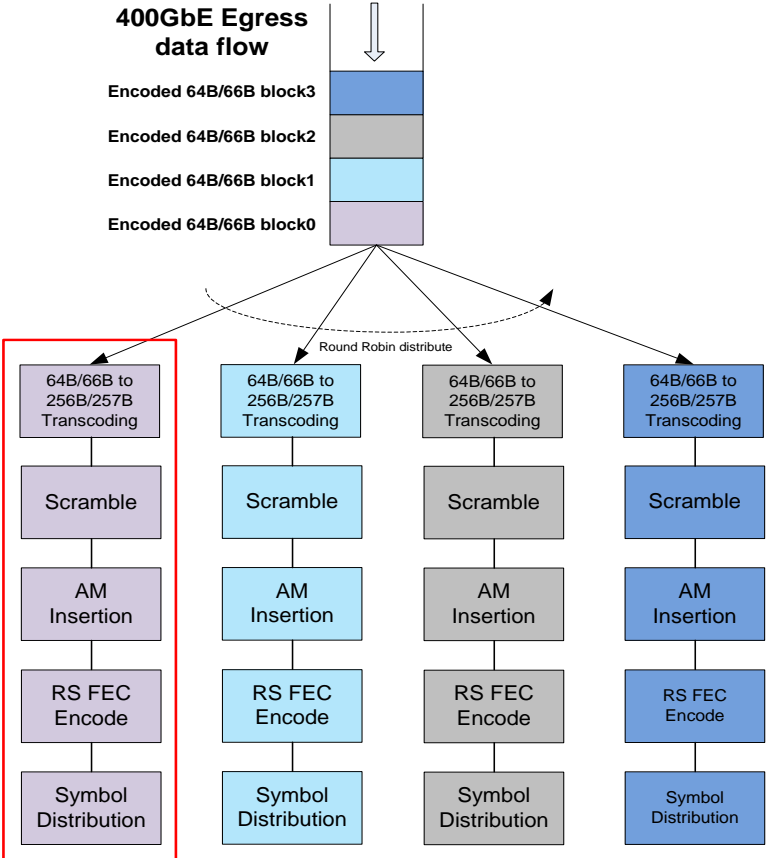
$$UI = \frac{1}{bit_rate}, T = \frac{1}{2\pi \times F_{cutoff}} = \frac{1667}{2\pi \times bit_rate}, \alpha = \frac{UI}{T + UI} \approx \frac{UI}{T}.$$

*Refer to anslow_01_0108.pdf

Scrambling and Transcoding scenarios



Scramble at each 100Gbps chunk and "Scrambling+Transcoding" scheme

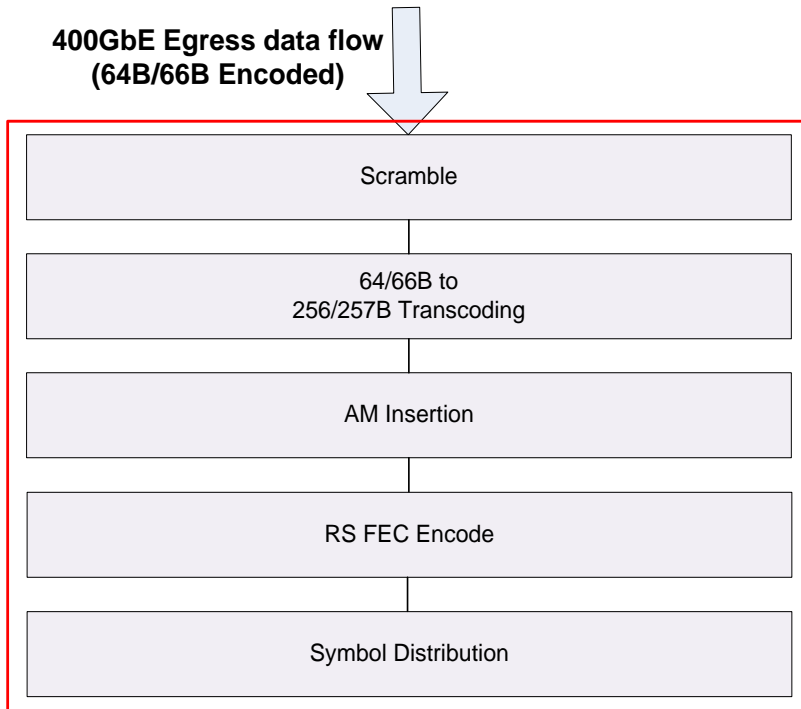


Scramble at each 100Gbps chunk and "Transcoding+Scrambling" scheme

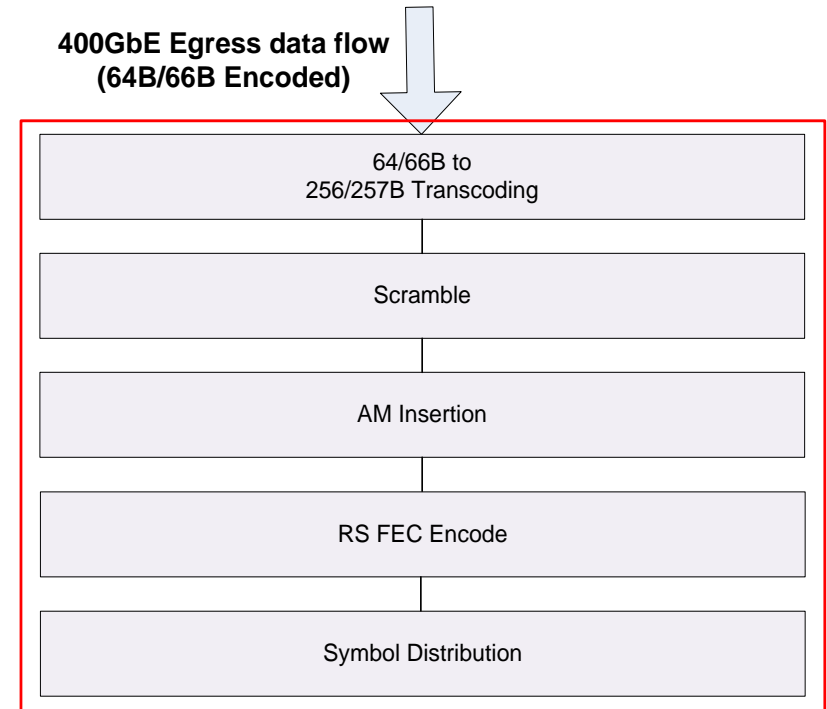
Option 1: 100Gbps "Scrambling+Transcoding"

Option 2: 100Gbps "Transcoding+Scrambling"

Scrambling and Transcoding Scenarios (Cont'd)



Scramble at 400Gbps chunk and
"Scrambling+Transcoding" scheme



Scramble at 400Gbps chunk and
"Transcoding+Scrambling" scheme

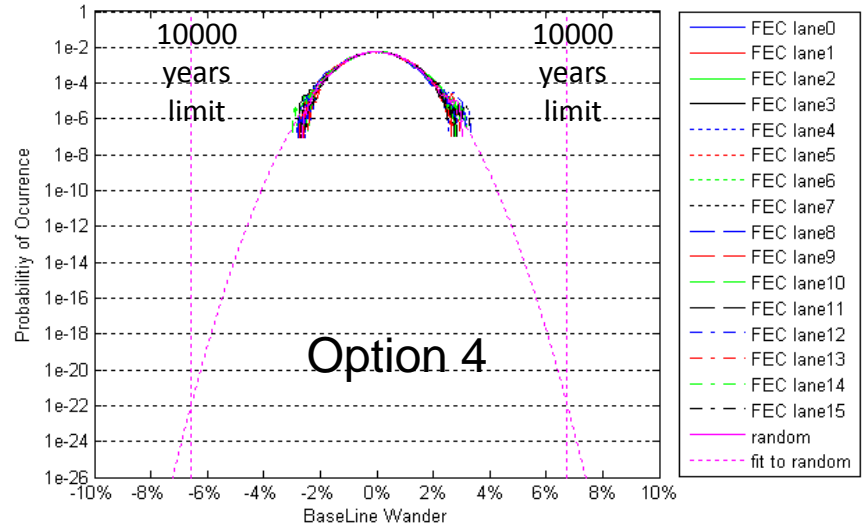
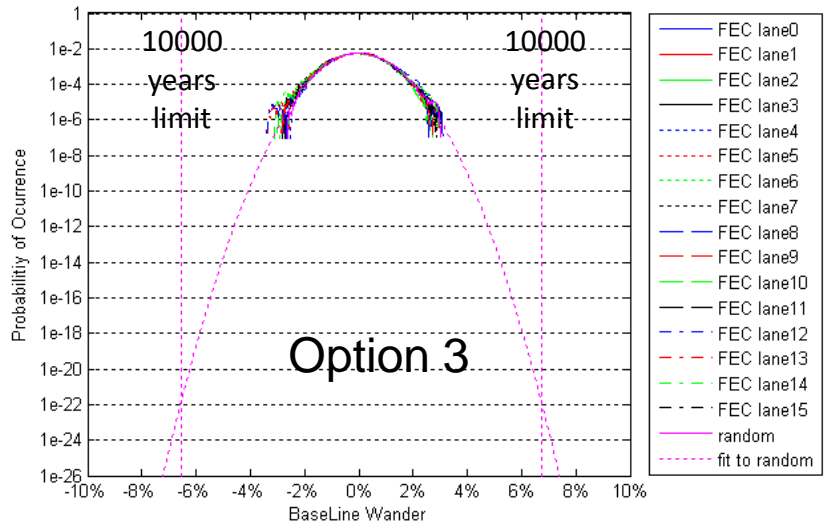
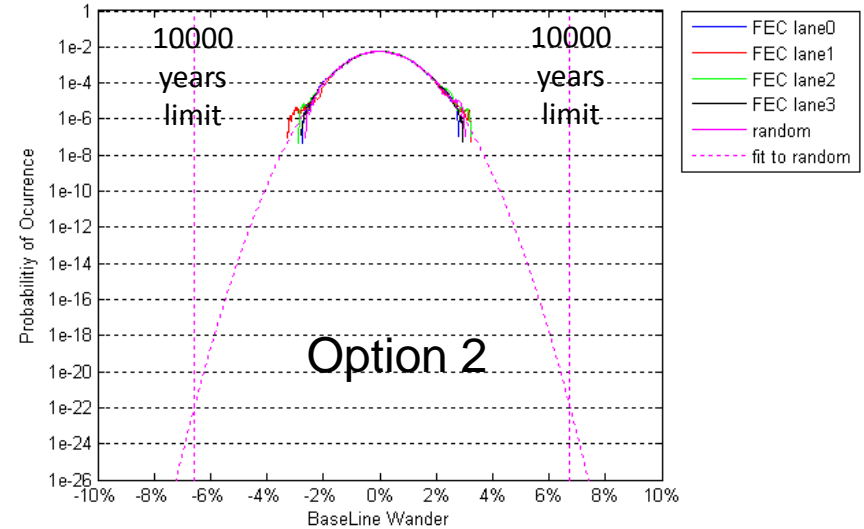
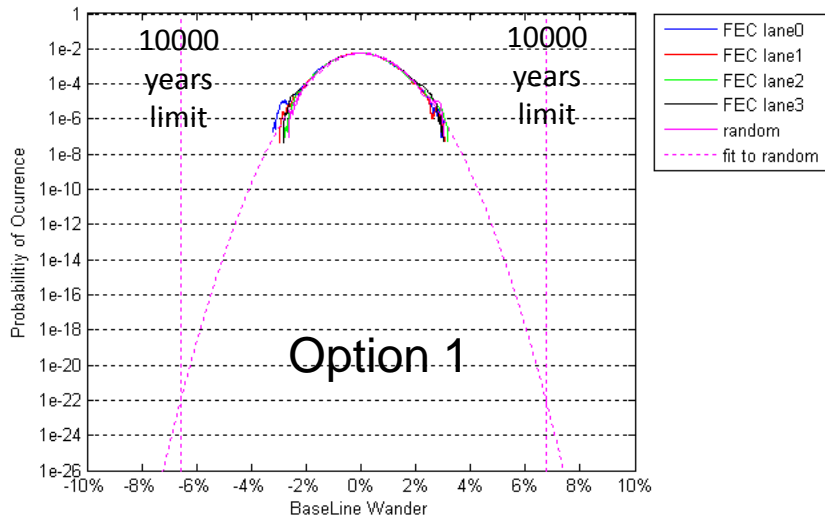
Option 3: 400Gbps "Scrambling+Transcoding"

Option 4: 400Gbps "Transcoding+Scrambling"

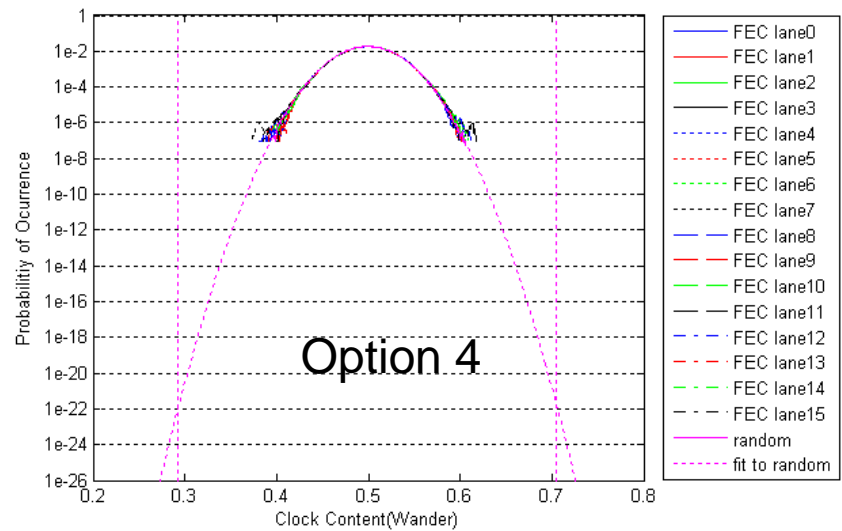
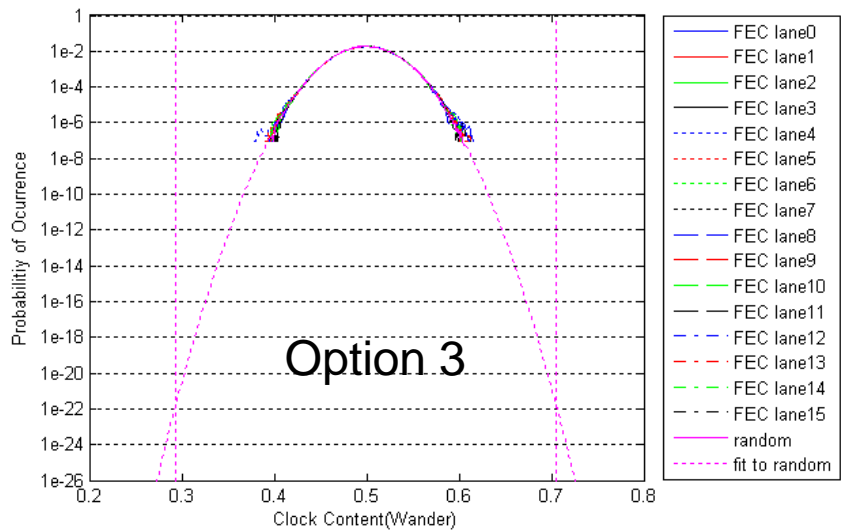
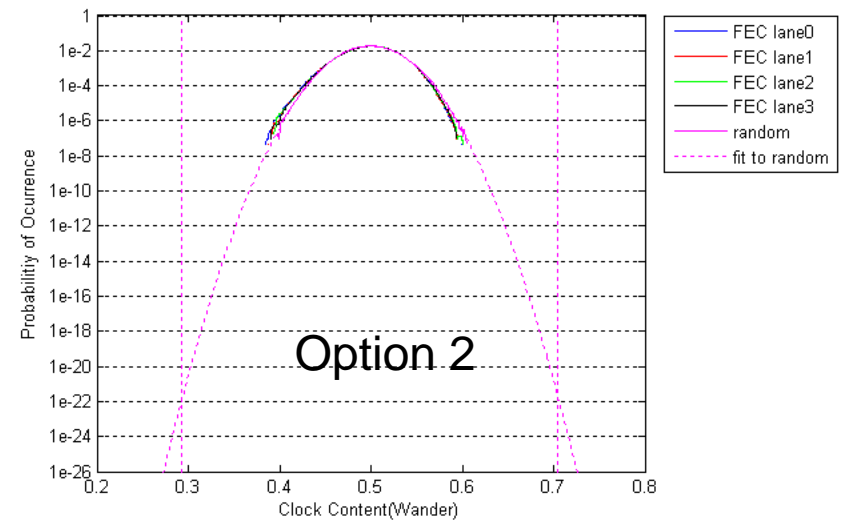
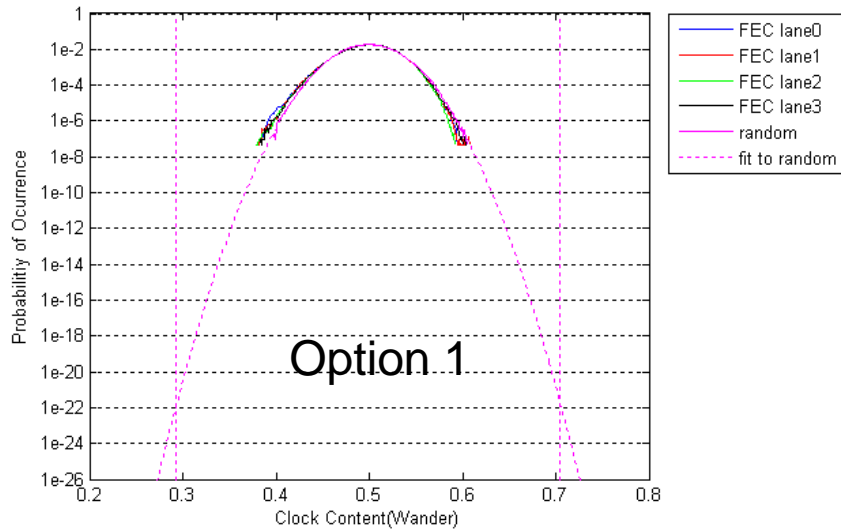
Wander Simulation Assumption:

- Transcoding : 64B/66B to 256B/257B
- Scrambler: $G(x) = 1 + x^{39} + x^{58}$
- Seed [57:0] of Scrambler: 0x00000007FFFFFFF
- Using Probability Density Functions (PDFs)/Probability of occurrence to show the probability at any instant that the baseline wander or clock wander exceeds a given value
- Simulation input signal length:
 - 16384*66*20*4 bits for option 1&2
 - 16384*66*80*2 bits for option 3&4
- Tested data pattern:
 - ① Random
 - ② Idle : {0x1e00000000000000, 0x1e00000000000000,}
 - ③ Square wave : {0xff00ff00ff00ff00.....}
 - ④ All ones: {0xffffffffffff.....}
 - ⑤ All zeros: {0x0000000000000000.....}
- Sync_header of 64B/66B block for all data patterns(except for Idle) has 3 cases:
 - ① 2'b10 for Control character only; ② 2'b01 for data character only; ③ mix of 2'b10, 2'b01 for control and data characters
- 10000 years probability limits based on random data pattern are plotted in all following figures by vertical dotted lines

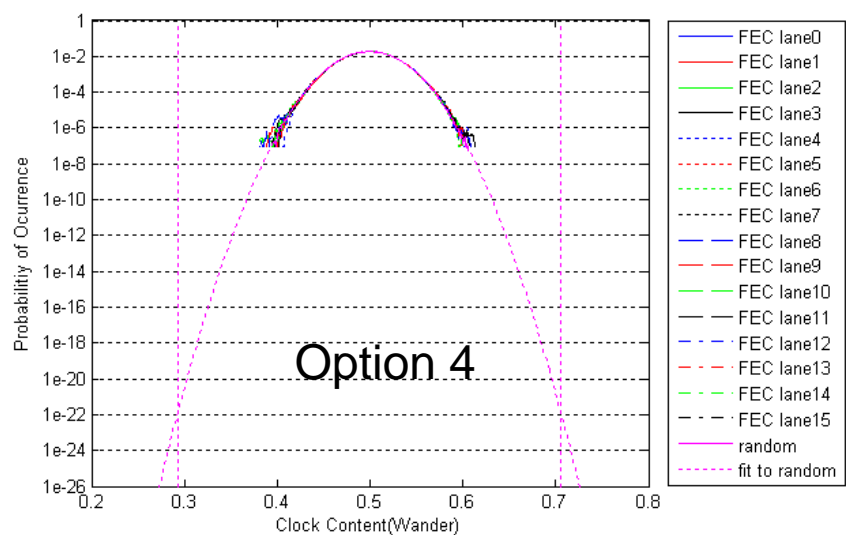
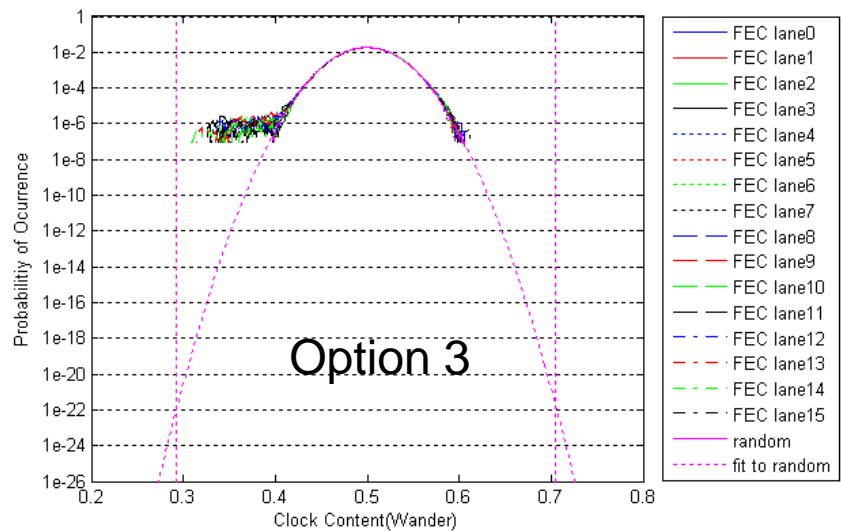
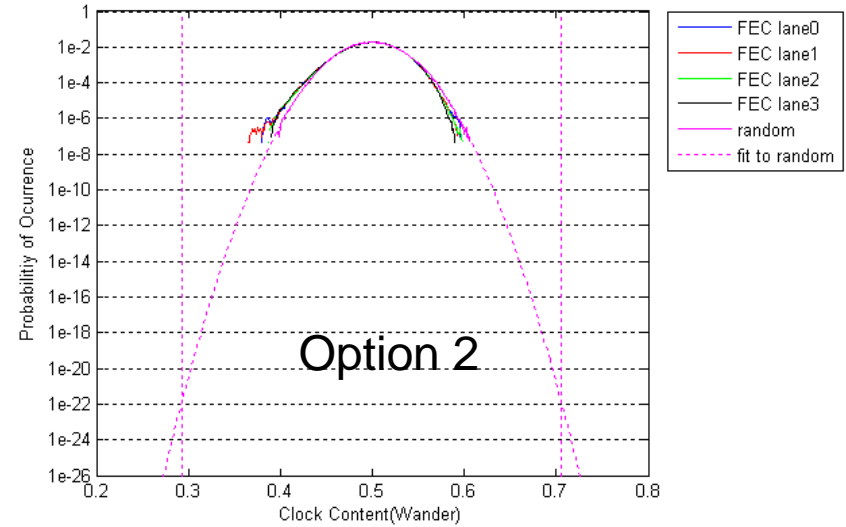
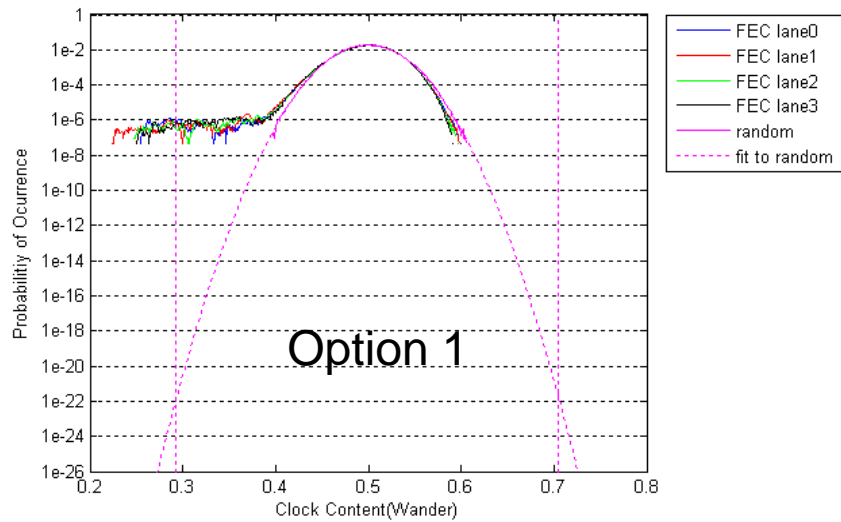
Baseline Wander PDFs for All Data Pattern



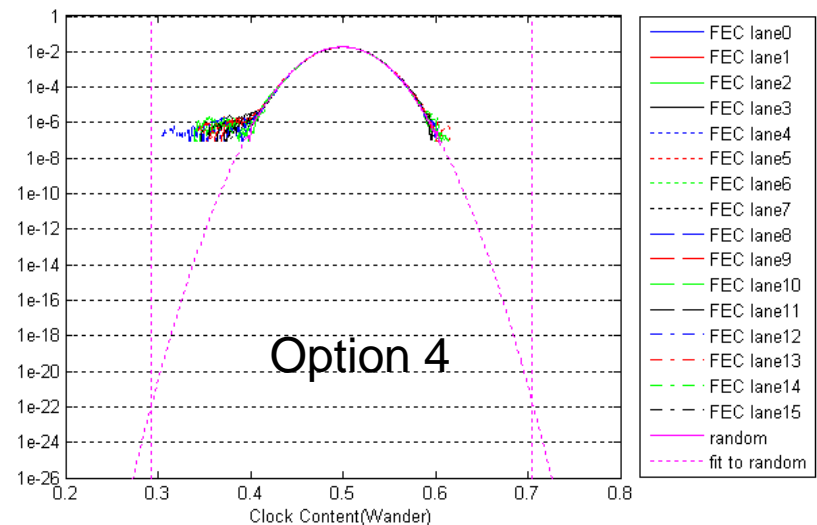
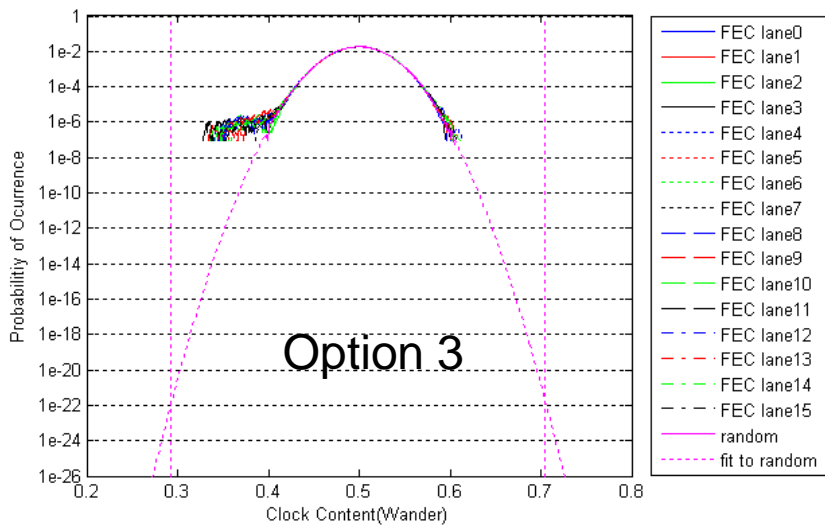
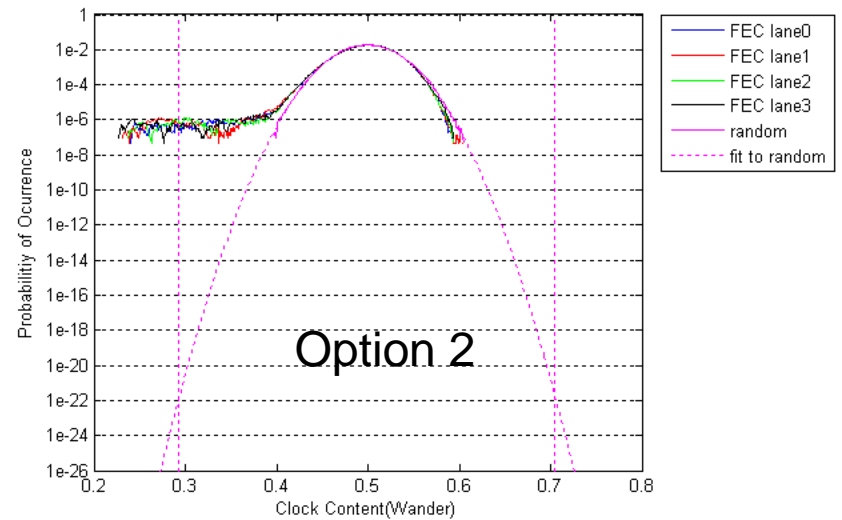
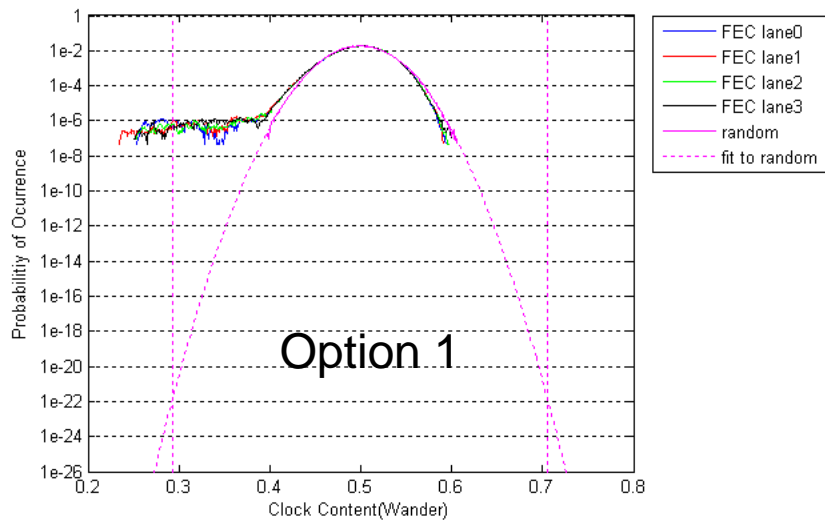
Clock Wander PDFs for Data Pattern 1/2/3



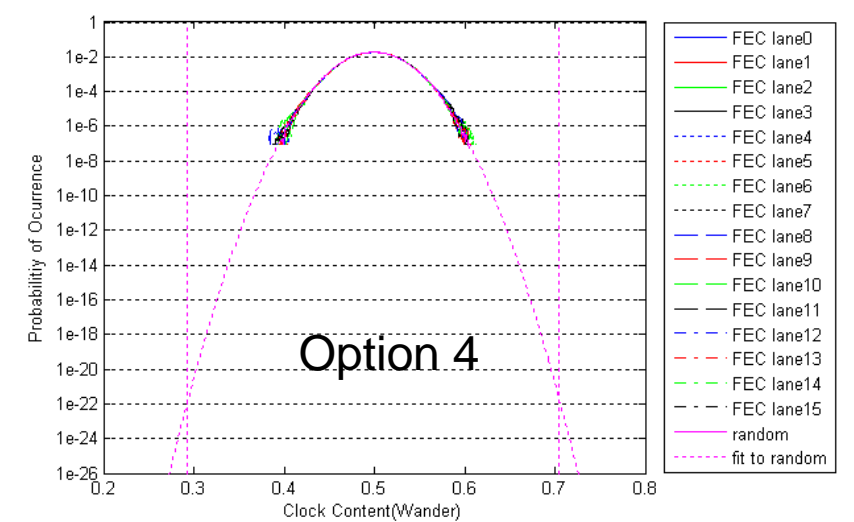
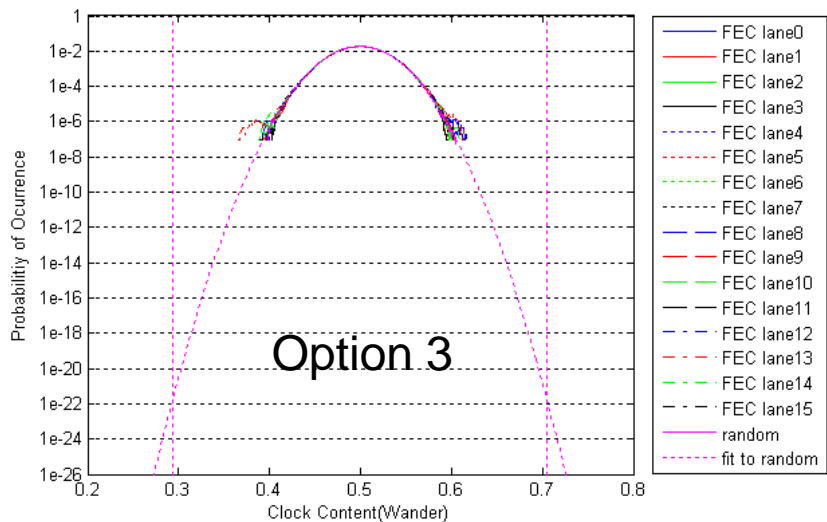
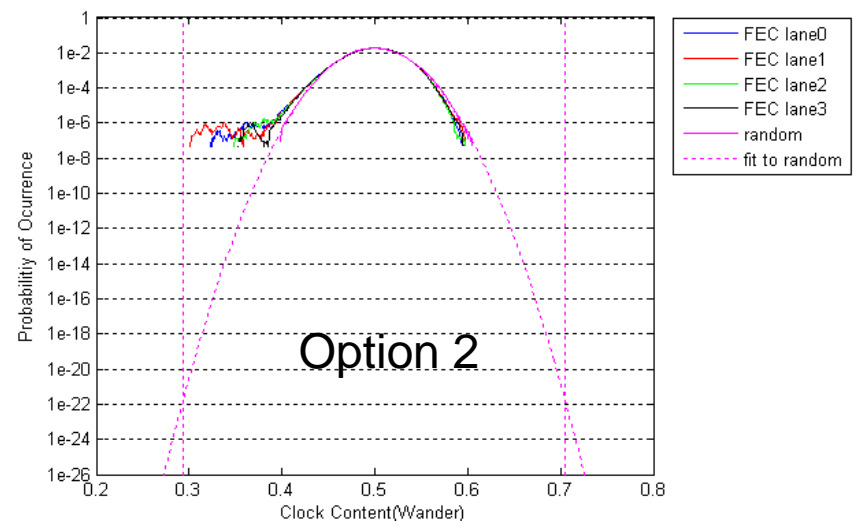
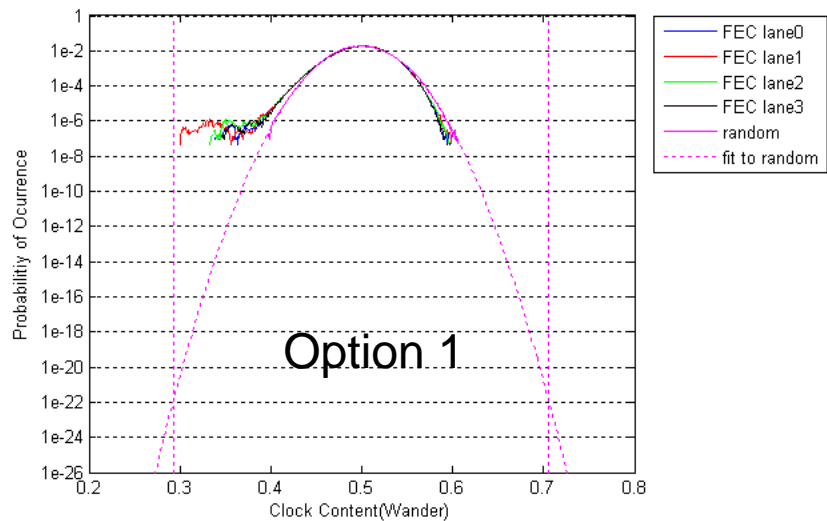
Clock Wander PDFs for Data Pattern 4 and Sync Header Case 1/3



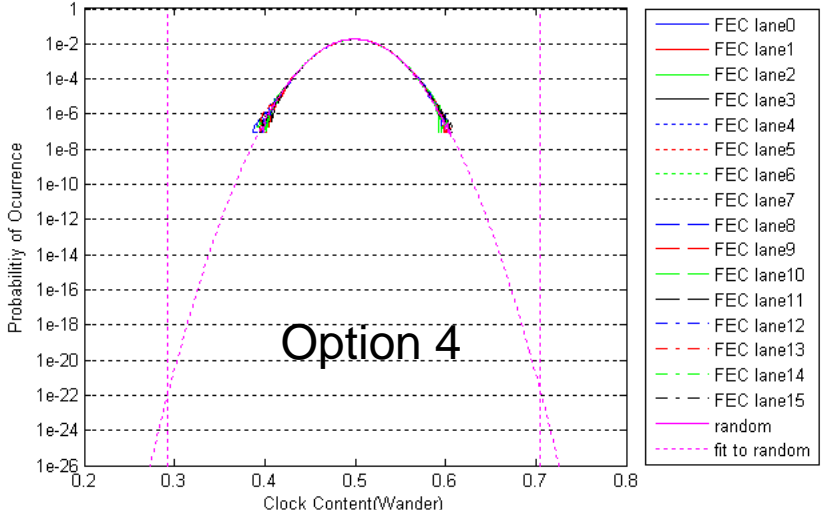
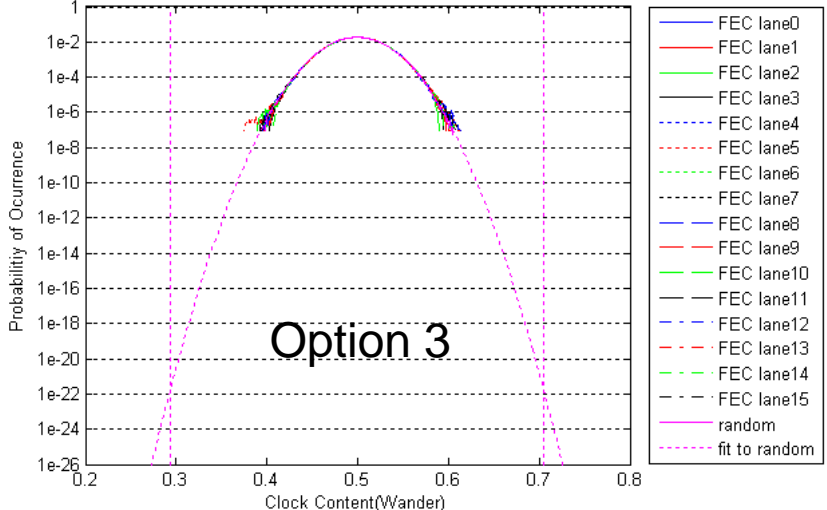
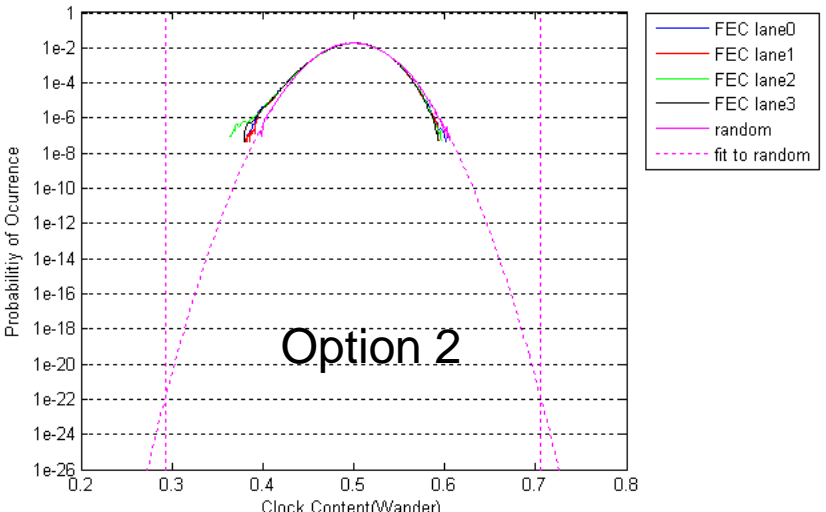
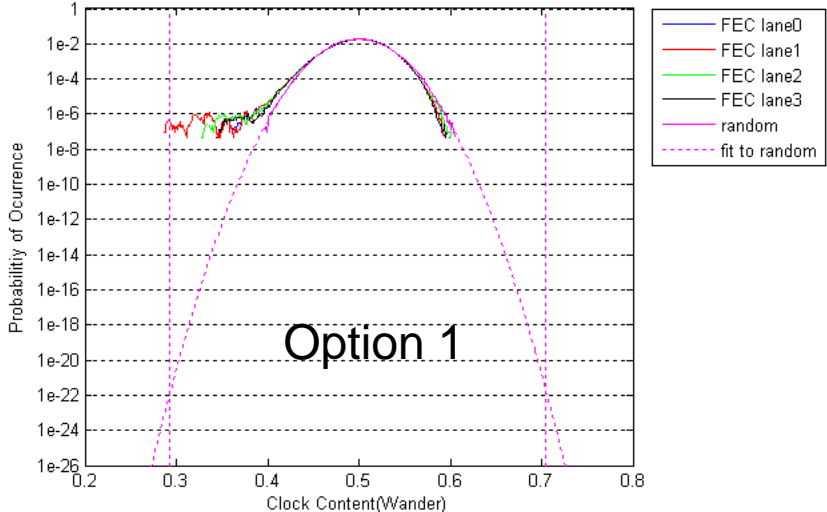
Clock Wander PDFs for Data Pattern 4 and Sync Header Case 2



Clock Wander PDFs for Data Pattern 5 and Sync Header Case 1

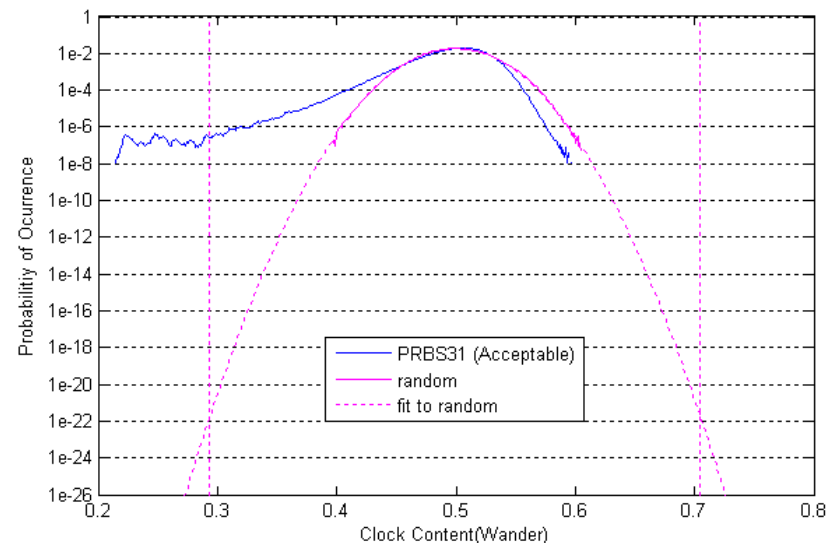
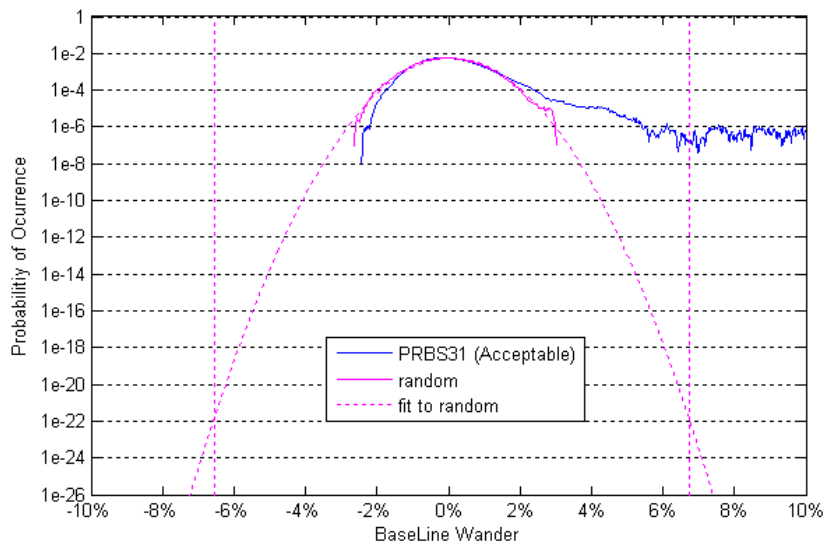
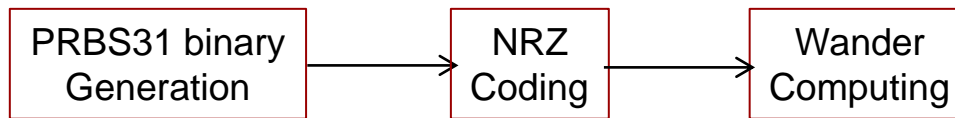


Clock Wander PDFs for Data Pattern 5 and Sync Header Case 2/3



Reference to Baseline & Clock Wander of PRBS31

- Simulation of baseline & clock wander of PRBS31 PDFs:
 - PRBS31 data pattern mapping in NRZ coding, then simulate on wander
 - Random data pattern for reference



- All of baseline/clock wander results in this slide for any option and test data pattern is much better or similar to result of PRBS31.

Summary

- Baseline wander PDFs for following scrambling and transcoding schemes have similar results, with different test data patterns
 - *Option 1: 100Gbps “Scrambling+Transcoding”*
 - *Option 2: 100Gbps “Transcoding+Scrambling”*
 - *Option 3: 400Gbps “Scrambling+Transcoding”*
 - *Option 4: 400Gbps “Transcoding+Scrambling”*
- Clock wander PDFs for all 4 options have different results, but they are all acceptable (compare to PRBS31 data pattern scenario)
- “Transcoding+Scrambling” scheme is feasible in 400GbE system for simple logic layer architecture
- Future work:
 - *Wander simulation with future defined AM pattern and PMA Multiplexing*
 - *PAM4 signaling influence on Wander*

Thank you