IEEE P802.3bs 400 Gb/s Ethernet Task Force Logic Ad Hoc

April 28, 2016

Mark Gustlin - Xilinx

Meeting Notes

- ➤ The stated charter is: The charter of the Logic Ad hoc will be to address all issues in relation to the overall architecture of IEEE P802.3bs to ensure progress towards a technically complete draft
- ➤ Any changes to the meeting minutes from the 2/23/16 call?
- > Reminder of the patent policy: http://www.ieee802.org/3/patent.html
 - Is anyone unfamiliar with it?
- ➤ Attendees names and affiliations will be taken from the Webex participants list. If you attend via phone only, or if your employer and affiliation are different, please send me an e-mail.
- ➤ Logic ad hoc location:

http://www.ieee802.org/3/bs/public/adhoc/logic/index.shtml

Agenda

- > PreFEC BER Signaling Features David Ofelt, Juniper
- **➤** SSPRQ test pattern Pete Anslow, Ciena
- **▶** 400GbE AMs revisited Pete Anslow, Ciena
- ➤ Next Logic ad hoc call:
 - TBD, after the May meeting