

PreFEC BER Signaling Features

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Supporters

Mark Gustlin - Xilinx

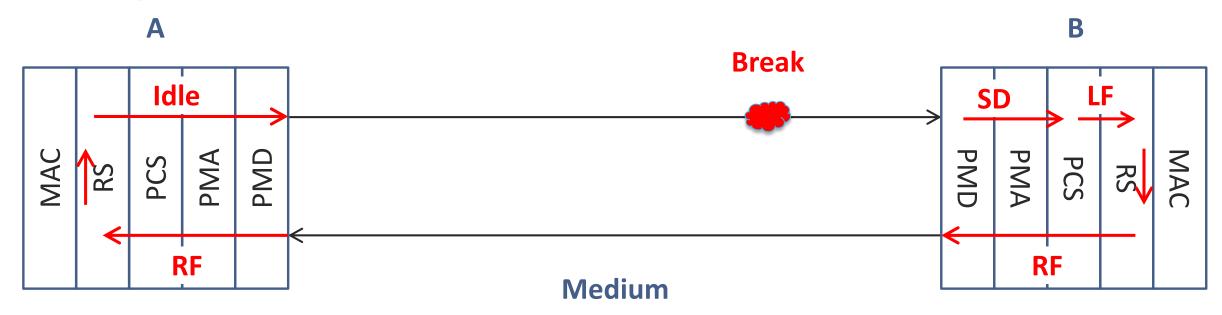
Background

- Working to add PreFEC BER monitoring features to 802.3bs
 - maki_3bs_01a_1115.pdf Background and Justification
 - ofelt_3bs_01a_0116.pdf Initial proposal
 - ofelt_3bs_01_0316.pdf

Status:

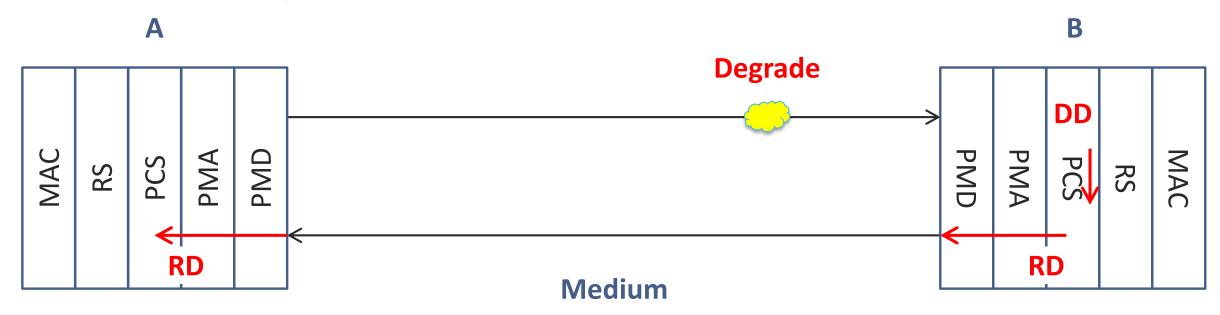
- Detailed PreFEC SER signaling proposal made at March meeting
- Consensus is positive for the features, but not the current details
- Punted it to the May meeting so we can work out the issues

Existing local fault / remote fault



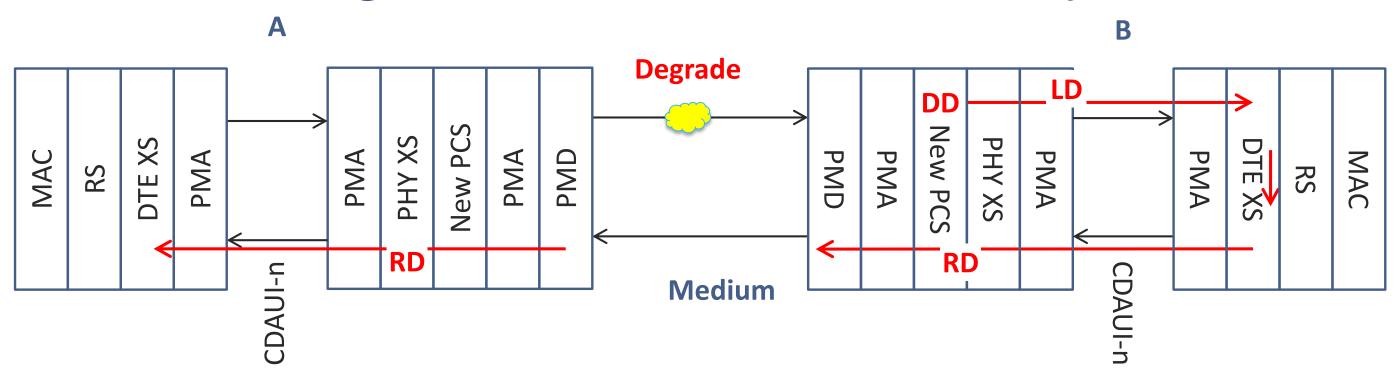
- PMD Rx at B sets SIGNAL_DETECT (SD) to FAIL
- PCS at B sends local fault (LF) to RS at B
- RS at B sends remote fault (RF) to A
- RS at A receives RF and sends all idle characters

Pre-FEC degrade no extender sublayer



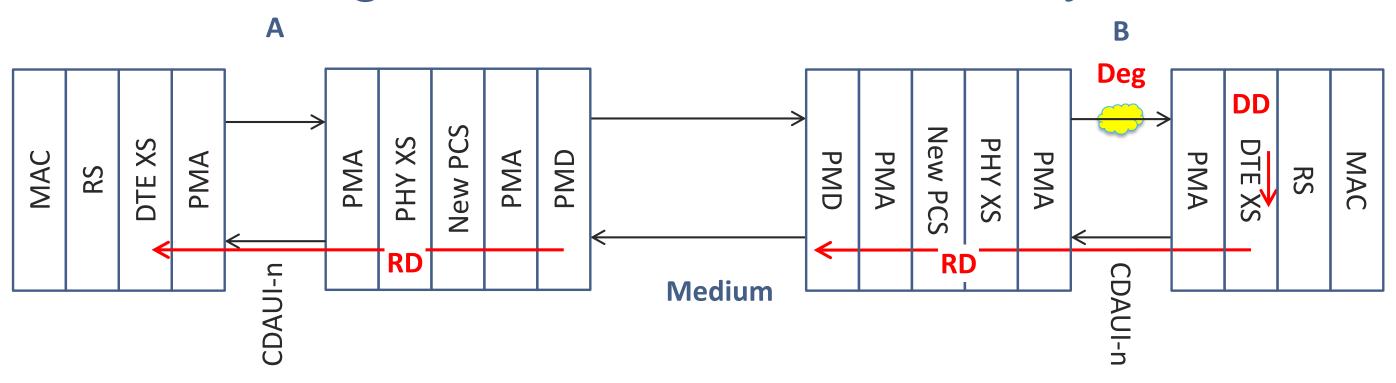
- PCS at B exceeds pre-FEC symbol error ratio (SER) threshold and detects degrade (DD)
- PCS at B sends remote degrade (RD) to PCS at A
- Traffic unaffected

Pre-FEC degrade with extender sublayer 1



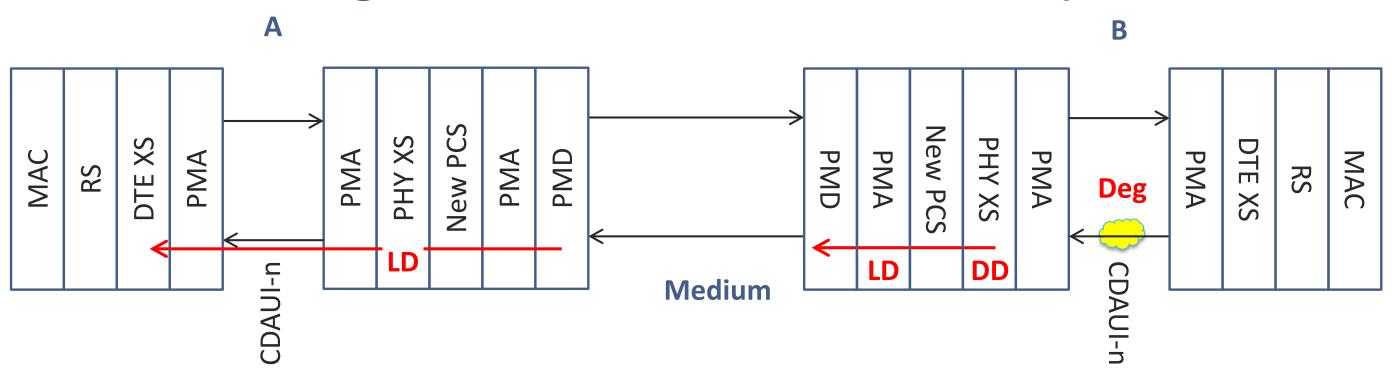
- New PCS at B exceeds pre-FEC symbol error ratio (SER) threshold and sends local degrade (LD) to DTE XS at B
- DTE XS at B sends remote degrade (RD) to DTE XS at A
- Traffic unaffected

Pre-FEC degrade with extender sublayer 2



- DTE XS at B exceeds pre-FEC symbol error ratio (SER) threshold and sends remote degrade (RD) to DTE XS at A
- Traffic unaffected

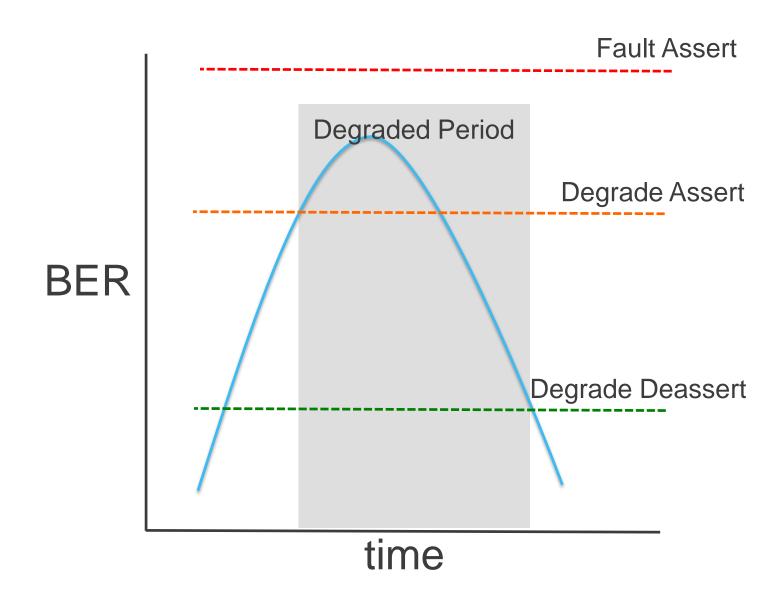
Pre-FEC degrade with extender sublayer 3



- PHY XS at B exceeds pre-FEC symbol error ratio (SER) threshold and sends local degrade (LD) to DTE XS at A
- Traffic unaffected

PreFEC Fault and Degrade

- Fault
 - Single threshold & interval
- Degrade
 - Separate activate and de-activate threshold and intervals



Issues From March

- PreFEC Fault
 - Why piggyback on FEC Bypass Indication?
 - Is PreFEC Fault needed?
- Why have separate intervals for both Degrade assert & deassert?
- How exactly does LD/RD work with an external FEC (XS)?
- Is using bits in the alignment markers the best way to carry LD/RD?

PreFEC Fault

- The proposal built the PreFEC Fault feature by teasing apart the FEC Bypass Indication (FBI) feature into a FBI piece and a HighBER piece.
- There was push back for two reasons:
 - Trying to reuse parts of the FBI feature didn't really simplify the specification nor was it a significantly cheaper approach than just having two separate features.
 - There was a desire to write the standard such that if the FBI feature was on, then there was no option on how you set the threshold and interval, since there is a safety/correctness issue if you don't set them correctly.
 - Basically- "you shall set the threshold and interval to 5560 and 8192 respectively"
- Proposal:
 - Add PreFEC Fault as an orthogonal feature to FBI (if we add it)

PreFEC Fault (2)

- In the discussions around PreFEC signaling the PreFEC Fault feature has not garnered much support.
- PCS has mechanisms for shutting down interface when too many uncorrectable FEC frames.
- A PreFEC Fault setting will be between this and the Degrade setting
 - Not clear if having this intermediate fault setting is useful
 - General feeling is that the Degrade detect is good enough
- Proposal:
 - Skip the PreFEC Fault feature unless someone makes a good case.

Degrade Assert & Deassert intervals

- The proposal specified separate interval and threshold values for both the PreFEC degrade assert and deassert settings
- At least one person felt that there should be just a single interval but two thresholds.
 - Some concern that the deassert SER needs to be significantly lower than the assert SER and having a separate interval would make easier to set appropriate values.

Proposal:

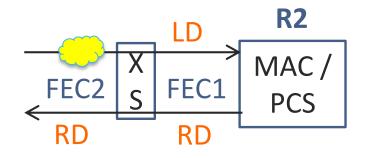
- Use a single interval and separate thresholds in the standard.
- Implementations are free to have separate intervals

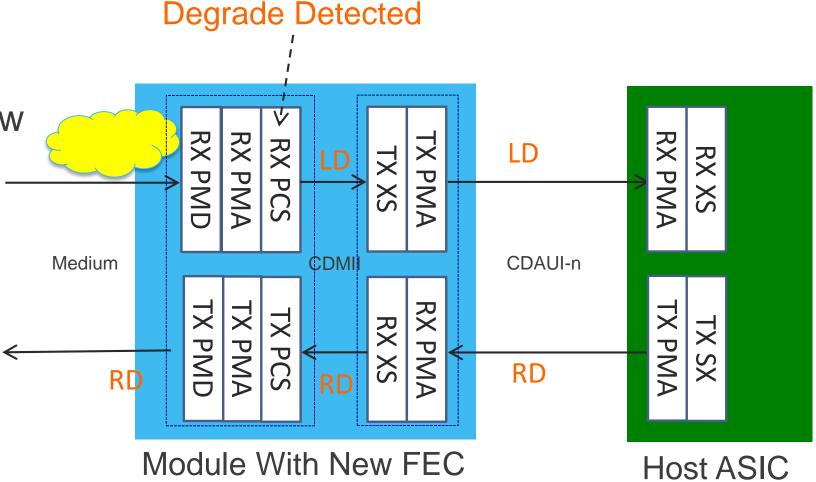
How does LD/RD work with an external FEC (XS)?

- The original proposal did not properly document the way PreFEC Degrade needs to work when using an external FEC in an extender sublayer.
- Extender Sublayer has two sets of transmit and receive blocks and information is not passed between them in the way described in the proposed text.

Pre-FEC Degrade External FEC

- Module with new FEC
- Degrade detected in module
 - Need to inform host
- New FEC is future work
 - But need to build host ASIC now
- LD/RD needs to pass over
 - CDMII
 - CDAUI





How does LD/RD work with an external FEC (XS)?

- Proposal:
 - In the 400GbE PCS Clause (119):
 - Document how LD/RD is carried in the data stream (see next issue)
 - Document how LD/RD is handled and generated
 - In the 400GbE extender sublayer clause (118):
 - Include picture showing layer diagram
 - Include text indicating how the LD and RD information moves between blocks
 - Could add formal CDMII signaling, but it doesn't seem necessary

Is using bits in the alignment markers the best way to carry LD/RD?

- Current proposal uses reserved alignment marker bits for the in-band PreFEC local & remote degrade signaling.
- Someone asked why we are putting things in the alignment markers.
 - If this feature is useful, then it is likely useful across multiple rates, PCS variations, etc, so it would be better to make it first-class and use an ordered set or similar approach.

Proposal:

- Stick with the AM approach. Significantly more to specify if we use ordered sets and increases the scope of the feature.
- It does mean that I'll be supporting a CWM in 50GbE ☺

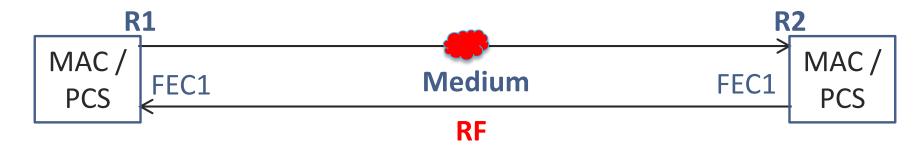
Summary & Next Steps

- Reviewed four issues with the previous PreFEC signaling proposal
 - PreFEC Fault implementation and justification
 - Degrade assert & deassert intervals
 - LD/RD handling in the extender sublayer
 - LD/RD transport mechanism
- Next steps:
 - If there is consensus, then I will provide detailed edits to D1.3 in the May meeting



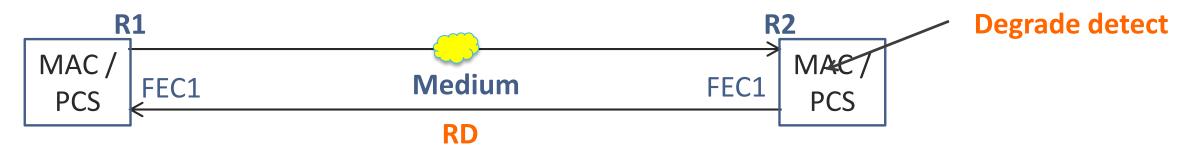
Thanks

Pre-FEC Fault Example



- Receive MAC in R2 detects pre-FEC count above the fault threshold
- RF sent to transmit MAC in R1
- Interface brought down

Pre-FEC Degrade Example



- Receive MAC in R2 detects pre-FEC count above the degrade threshold
- Remote Degrade (RD) signal sent to the transmit MAC in R1
- Traffic not affected

Pre-FEC Degrade Example with XS



- Receive XS at R2 detects pre-FEC error above degrade threshold
- Receive XS at R2 signals Receive MAC using LD (Local Degrade)
- MAC in R2 signals a RD (remote degrade) to the MAC in R1. The RD signal is regenerated by both the XS in R2 and in R1.
- Packet traffic not affected