# Simplified Transcoding Scheme for 400GbE

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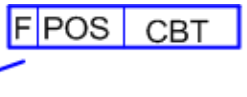
# Motivation

- Bj FEC (either KR4 FEC or KP4 FEC) has been well discussed for possible adoption by IEEE P802.3bs standard.
- The 256b/257b transcoding (TC) scheme is closely tied with bj FEC.
- It is reported that the hardware of transcoding and reverse transcoding circuitry in 100G-GE systems is not insignificant. Thus seeking a simple simplification to transcoding scheme may be worthwhile.
- One example of 256b/257b transcoding:

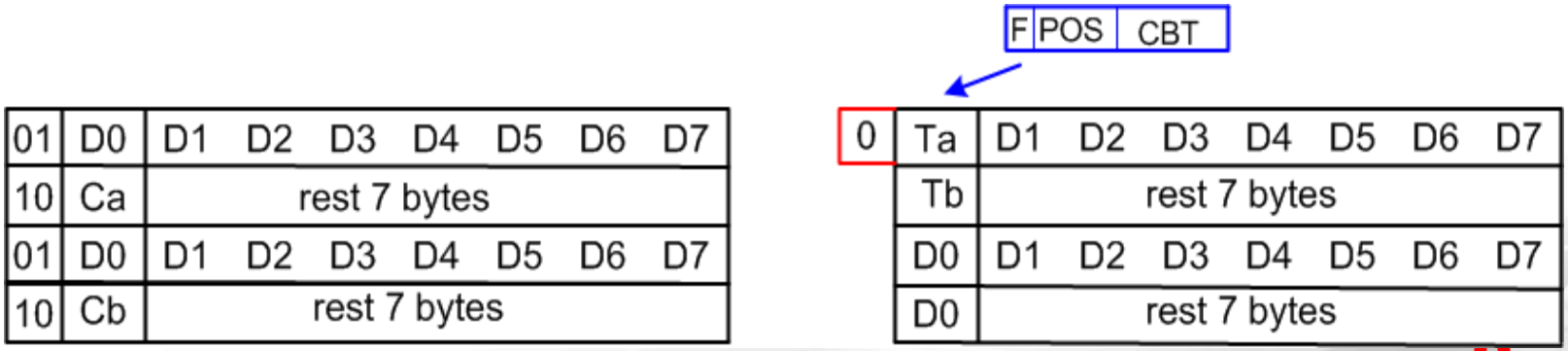
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 01 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| 10 | Ca | rest 7 bytes | | | | | | |
| 01 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| 10 | Cb | rest 7 bytes | | | | | | |



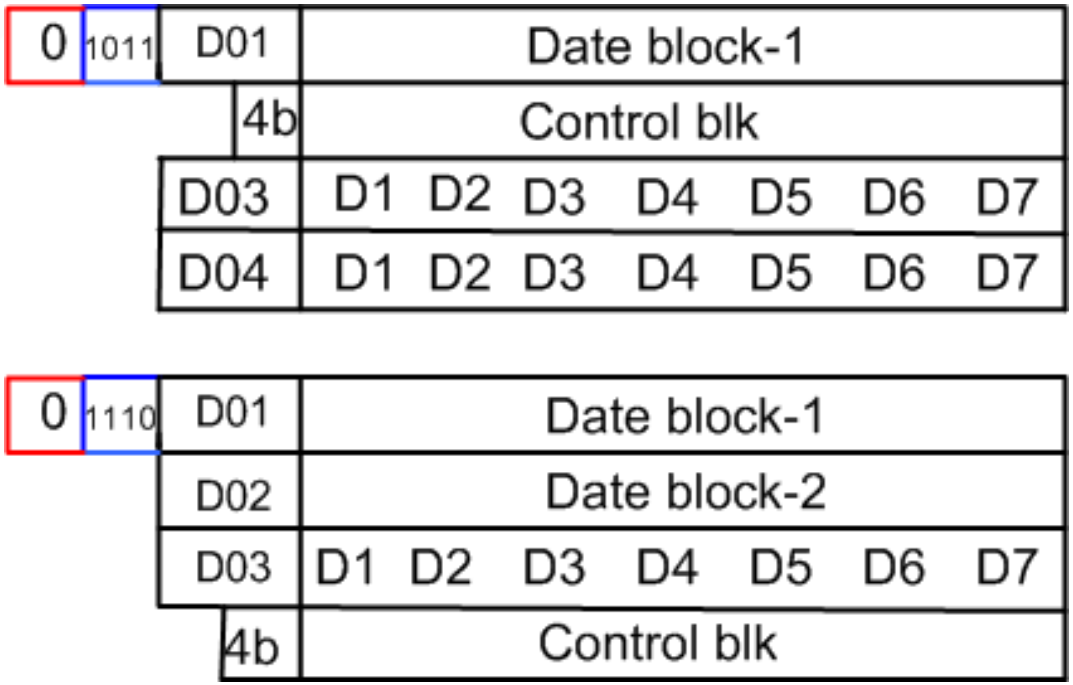

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | Ta | rest 7 bytes | | | | | | |
| | Tb | rest 7 bytes | | | | | | |
| | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |

# Reduced Complexity Solution

- To reduce implementation complexity, we can ONLY swap (if needed) first bytes for each row. An example is shown in the following figure. This idea can be applied to other transcoding schemes such as 512B/514B TC and 1024B/1027B TC as well.
- In case of multiple ctrl block, positions index in POS field are in order.
- With new scheme, the muxing logic is only associated with first 8 bits instead of 64 bits in conventional design.



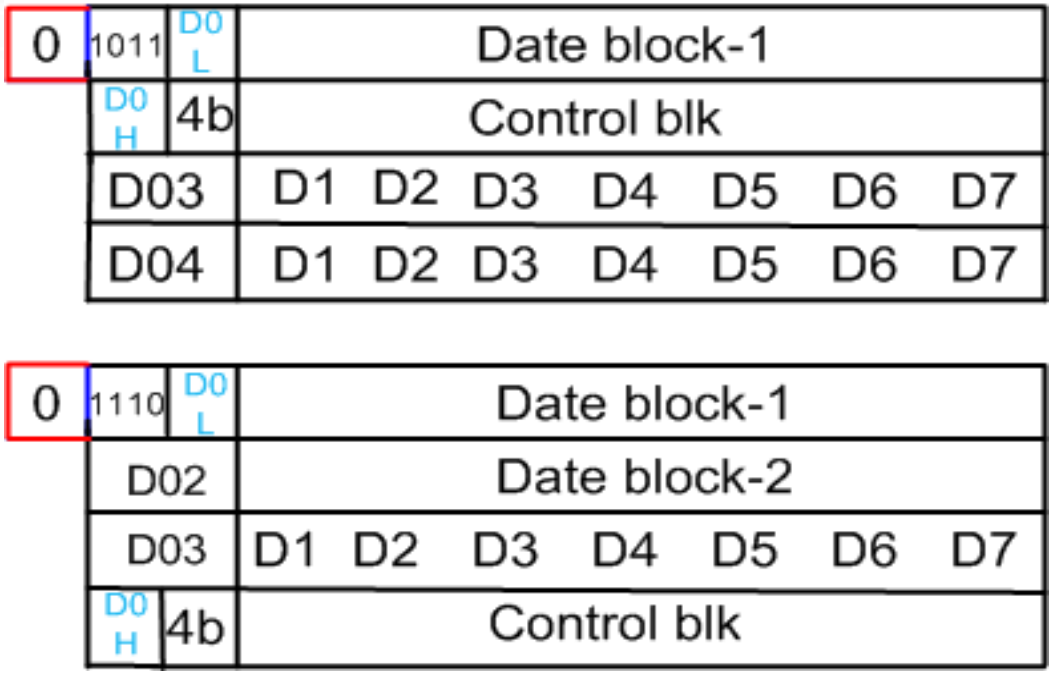
# Revisit 802.3bj TC Scheme




- **The above figure shows an example illustrating the transcoding scheme [1].**
- **With this solution of shifting around bits, we need muxing logic for most of the bits within 256b block.**

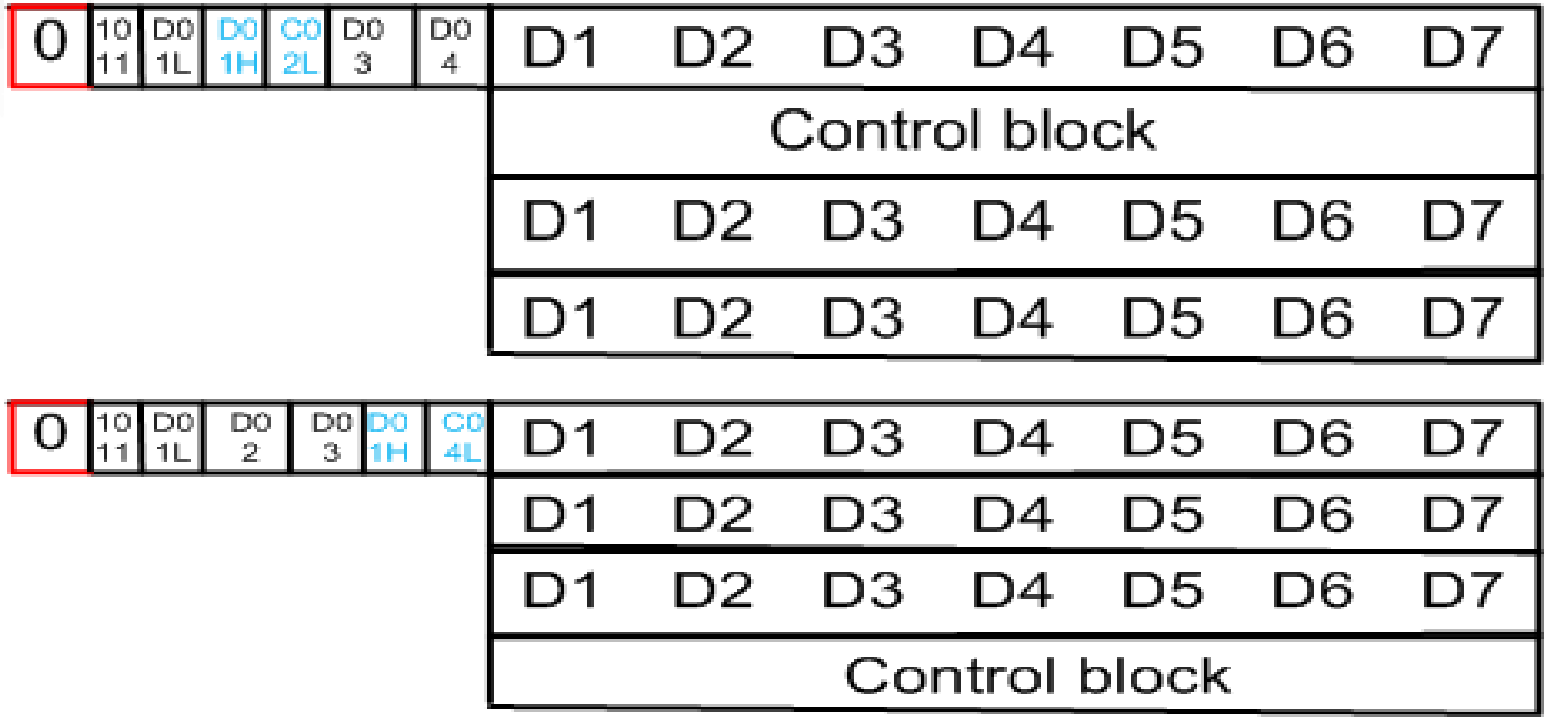
[1] http://ieee802.org/3/100GNGOPTX/public/mar12/interim/cideciyan_01_0312_NG100GOPTX.pdf

# A Simplified Solution




- If all 4 sub-blocks are data block, there's no need to switch any data.
- If there's at least one 66-b control block, we obtain the 4-bit index as before. But we only replace 4 msb's of the 1st ctrl block with 4 msb's of the 1st data block (D0H). The complexity of muxing logic will be much reduced.

# Alternate Solutions




- Lump first bytes of all 4 sub-blocks together and put them at the beginning.
- The above schemes can maximally maintain the low-latency property in trans-decoding of original TC scheme adopted by IEEE P802.3bj.

# Summary

- Simplified transcoding schemes are presented to simplify the hardware implementation. The complexity of muxing logic for data portions can be reduced by many times.

- If transcoding is performed over 200Gbps or 400Gbps data stream, we most likely need process 256bits or more per clock cycle. In these cases, the low-latency feature of original TC scheme is not useful.

- If TC is done over 100Gbps data stream, we could potentially save 1.2ns in trans-decoding if we can operate the circuit near 800Mhz.

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