IEEE P802.3bs 400 Gb/s Ethernet Task Force
Logic Ad Hoc

December 11, 2015

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Meeting Notes

- The stated charter is: **The charter of the Logic Ad hoc will be to address all issues in relation to the overall architecture of IEEE P802.3bs to ensure progress towards a technically complete draft**

- **Any changes to the meeting minutes from the 10/22/15 call?**

- **Reminder of the patent policy: http://www.ieee802.org/3/patent.html**
  - Is anyone unfamiliar with it?

- Attendees names and affiliations will be taken from the Webex participants list. If you attend via phone only, or if your employer and affiliation are different, please send me an e-mail.

- **Logic ad hoc location:**

  http://www.ieee802.org/3/bs/public/adhoc/logic/index.shtml

Agenda

- **Alignment Marker Lock/Unlock Schemes for 400GE – Zhongfeng Wang**
- **FEC Modes – Phil Sun**
- **400GbE AMs and PAM4 test pattern characteristics – Pete Anslow**
- Next Logic ad hoc call:
  - Friday 1/8/2016, 8am PST