400GbE AMs and PAM4 test pattern characteristics

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IEEE P802.3bs Task Force, Logic Ad Hoc, 11 December 2015

Introduction

A PRBS13Q short test pattern was added to P802.3bs D1.1 and there has been a proposal to use PRBS31Q as a long test pattern. This contribution analyses the performance of these test patterns.

The alignment markers for 400GbE are TBD. This contribution also proposes some marker values and analyses the performance of them.

Baseline wander

Previous NRZ contributions have used a “baseline wander” parameter

This was defined as:

Baseline wander is the instantaneous offset (in %) in the signal generated by AC coupling at the Baud rate / 10,000.

This analysis re-uses this definition unmodified, but it should be noted that for PAM4, the eye height is 1/3 that of NRZ so the effects of a given amount of baseline wander will be greater.

For NRZ contributions see:

P802.3ba anslow_01_0108
P802.3ba anslow_06_1108
P802.3bj anslow_01a_0112

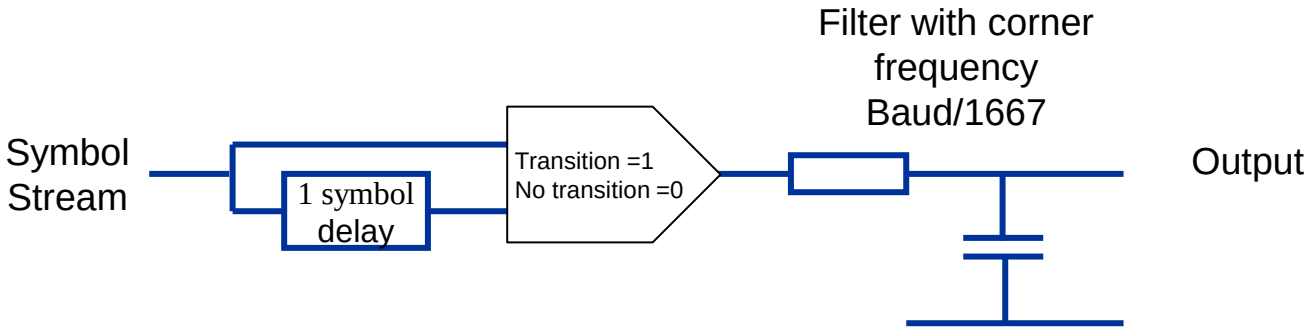
Clock content

Previous NRZ contributions have also used a “clock content” parameter defined as:

Create a function which is a 1 for a transition and a 0 for no transition and then filter the resulting sequence with a corner frequency of Baud/1667.

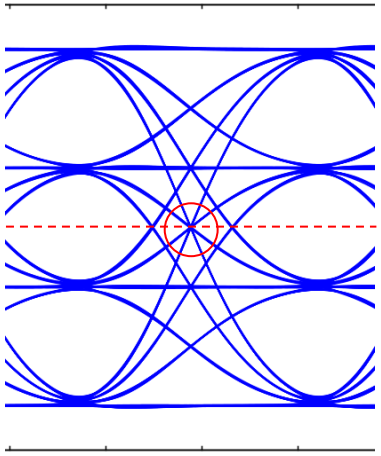
This analysis re-uses this definition unmodified but defines a transition as one of three possibilities (as per healey_3bs_01_1115):

- Symmetrical transitions through the signal average
- Transitions through the signal average
- All transitions

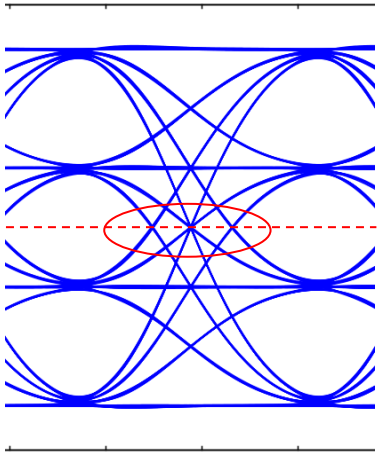


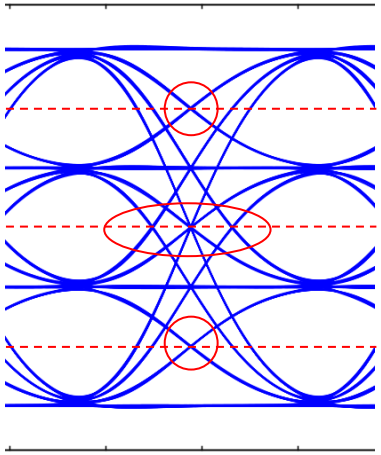
Clock content illustration

Symmetrical transitions through the signal average



Transitions through the signal average





All transitions

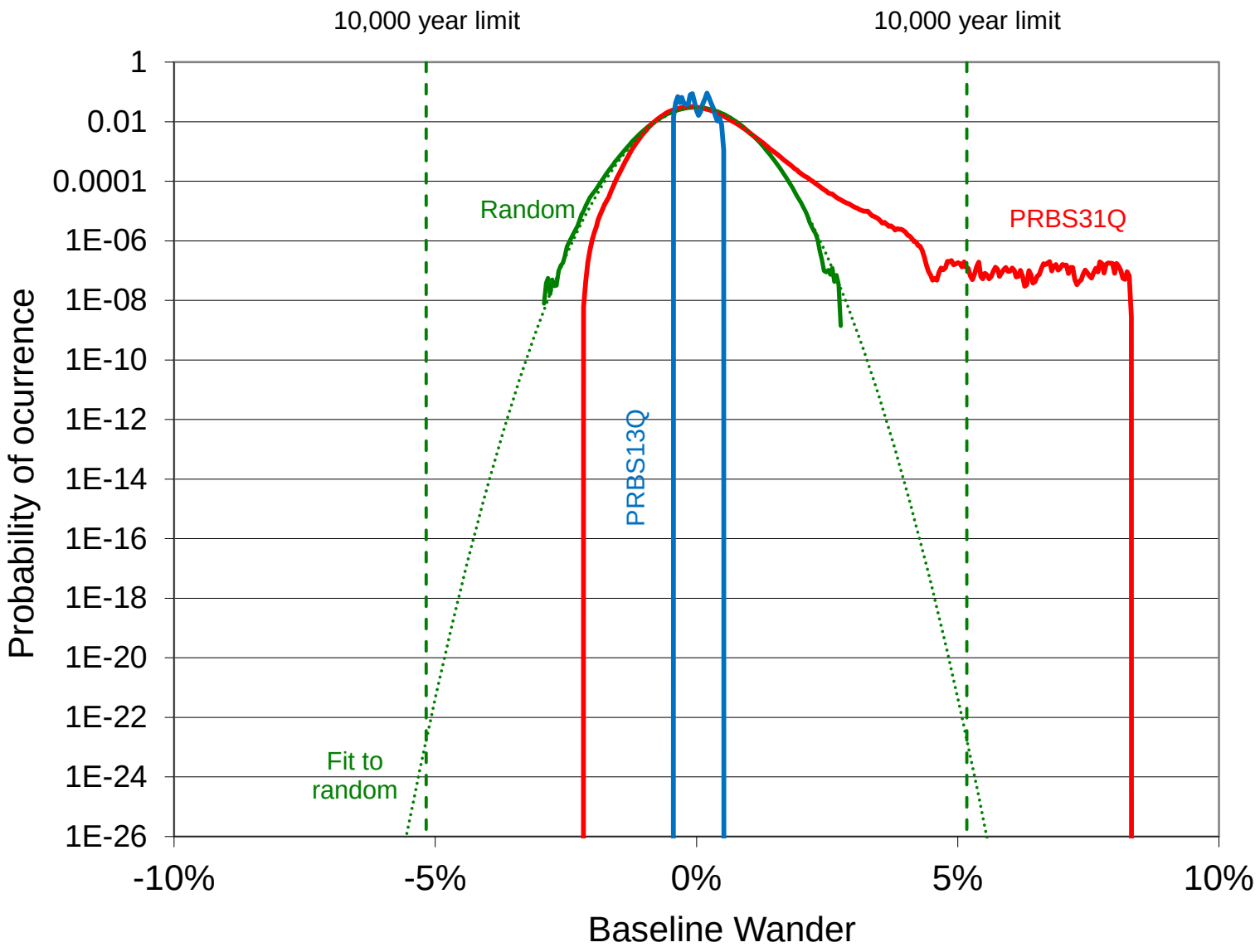
PRBS13Q and PRBS31Q

The following slides contain the baseline wander and three clock content probability density plots for:

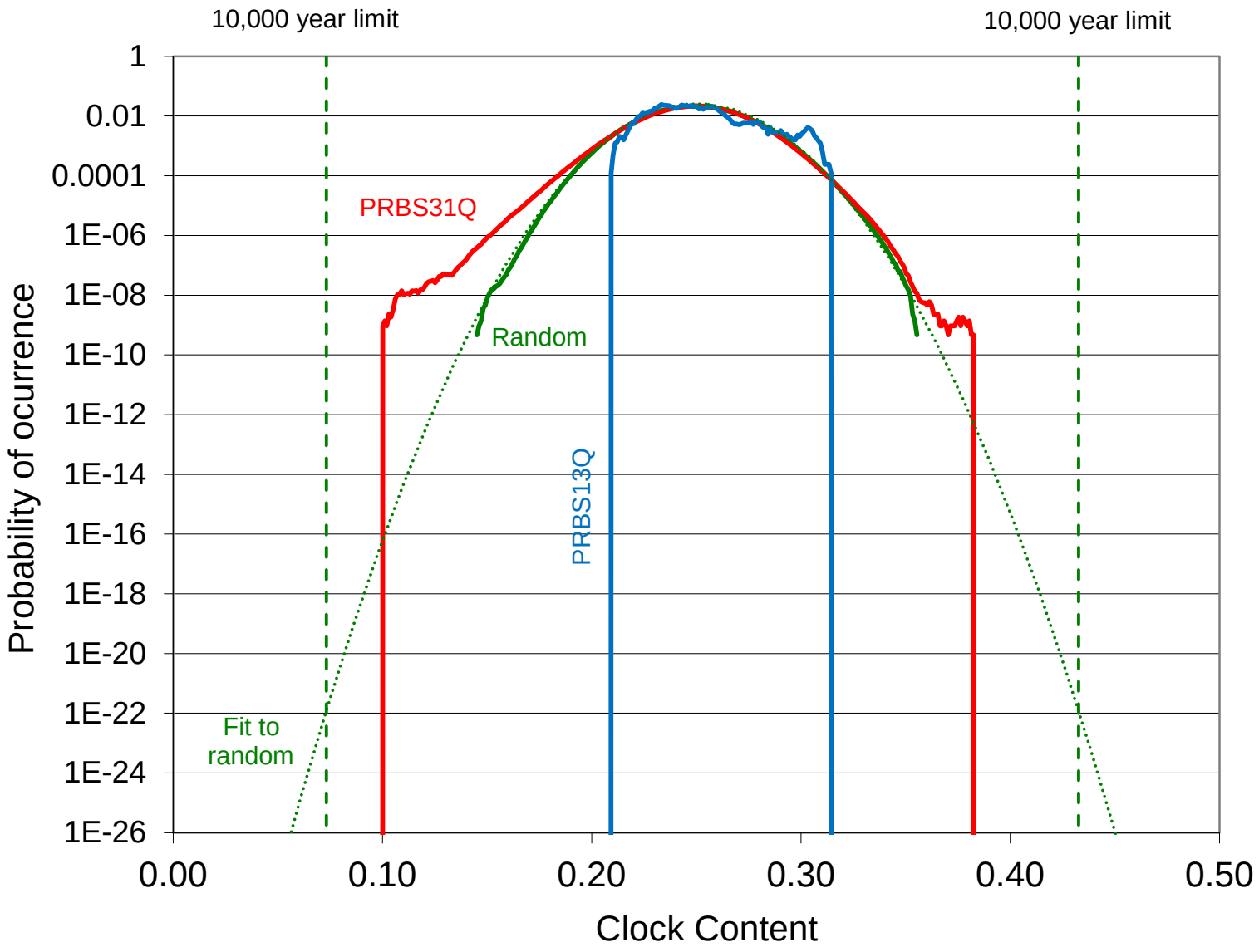
- Random data (solid green)
- Fit to random data (dotted green)
- PRBS13Q (blue)
- PRBS31Q (red)

Where the PRBS31Q pattern was formed as per PRBS13Q but with a PRBS31 NRZ starting pattern in place of the PRBS13 pattern.

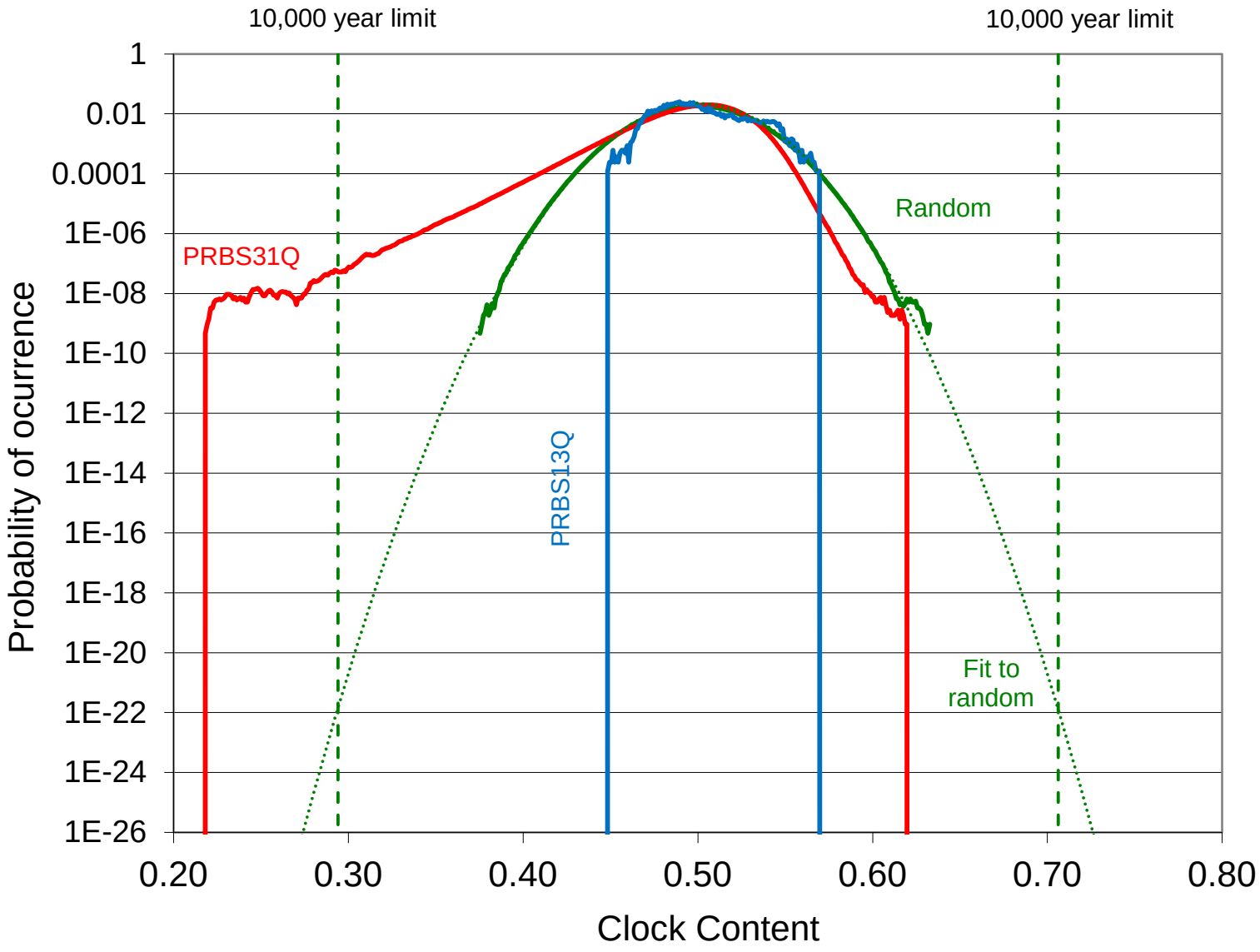
Baseline wander



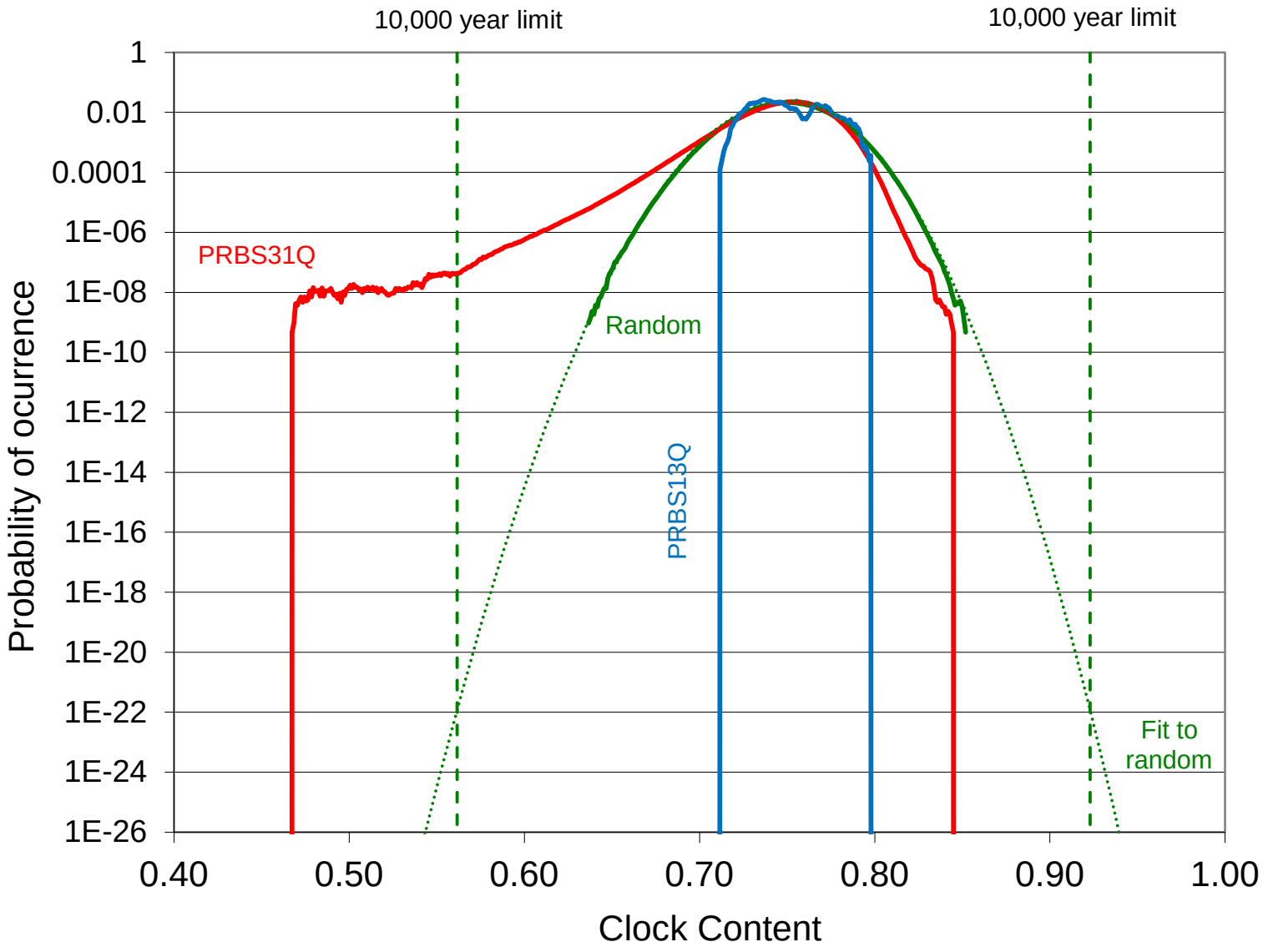
Clock, symmetric transitions through ave.



Clock, transitions through ave.



Clock, all transitions



Alignment markers

In D1.1, Table 119-1 defines 120-bit alignment markers with a 64-bit common part of “0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B” followed by a 56-bit unique part.

The alignment markers for 40 and 100 GbE were defined in anslow_06_1108 and anslow_01_0108, respectively. The codes used were generated using a section of the $1 + x^{39} + x^{58}$ scrambler output with all zeros input.

This contribution proposes a set of 56-bit unique part alignment markers for 400 GbE based on a section of the $1 + x^{39} + x^{58}$ scrambler output with all zeros input. The markers were chosen so that each byte of the unique part (M_8, M_9, etc.) is unique for each marker including the 20 x 100 GbE, 4 x 40 GbE, and markers used by OIF for MLG.

Bytes 12, 13, and 14 of the marker were formed from the inverse of bytes 8, 9, and 10 to minimise the baseline wander caused by the markers.

The proposed markers are shown on the next page.

Alignment marker proposal

Table 119–1—400GBASE-R Alignment marker encodings

PCS lane number	Encoding[a] {M_0, M_1, M_2, M_3, M_4, M_5, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}}
0	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x9E, 0xEB, 0x27, 0xB4, 0x61, 0x14, 0xD8
1	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x50, 0x74, 0x88, 0x5A, 0xAF, 0x8B, 0x77
2	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0xB4, 0xB7, 0xEA, 0xB4, 0x4B, 0x48, 0x15
3	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0xE4, 0xFB, 0xF1, 0xB4, 0x1B, 0x04, 0x0E
4	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0xDC, 0x58, 0xEE, 0x78, 0x23, 0xA7, 0x11
5	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0xBD, 0xA9, 0xBF, 0xA5, 0x42, 0x56, 0x40
6	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x97, 0x67, 0x77, 0x78, 0x68, 0x98, 0x88
7	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x24, 0x35, 0xA5, 0x87, 0xDB, 0xCA, 0x5A
8	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x57, 0x64, 0x51, 0xB4, 0xA8, 0x9B, 0xAE
9	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x28, 0xF9, 0x3E, 0xB4, 0xD7, 0x06, 0xC1
10	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0xCB, 0xD1, 0xAD, 0x2D, 0x34, 0x2E, 0x52
11	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x5E, 0x1E, 0x38, 0x4B, 0xA1, 0xE1, 0xC7
12	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x19, 0x98, 0xF9, 0x96, 0xE6, 0x67, 0x06
13	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x84, 0xEC, 0x20, 0x4B, 0x7B, 0x13, 0xDF
14	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x13, 0xA4, 0xED, 0xC3, 0xEC, 0x5B, 0x12
15	0xC1, 0x68, 0x21, 0xF4, 0x3E, 0x97, 0xDE, 0x0B, 0x3F, 0x8A, 0xBE, 0x5A, 0xC0, 0x75, 0x41

[a]Each octet is transmitted LSB to MSB.

Simulations

Using these new alignment codes, all possible combinations of PCS lanes for 2:1 bit interleaving for 50 Gb/s lanes and 4:1 bit interleaving for 100 Gb/s lanes were then analysed to find the worst cases for Baseline Wander (BW) and Clock Content (CC) after Gray coding to PAM4 symbols. These searches included lane delays of -40 to +40 bits for each PCS lane for the 2:1 case and -20 to +20 for the 4:1 case.

The worst case PCS lane combinations and delays were then used to generate the worst case PDFs for 400 GbE scrambled idle 50 Gb/s lanes and 100 Gb/s lanes.

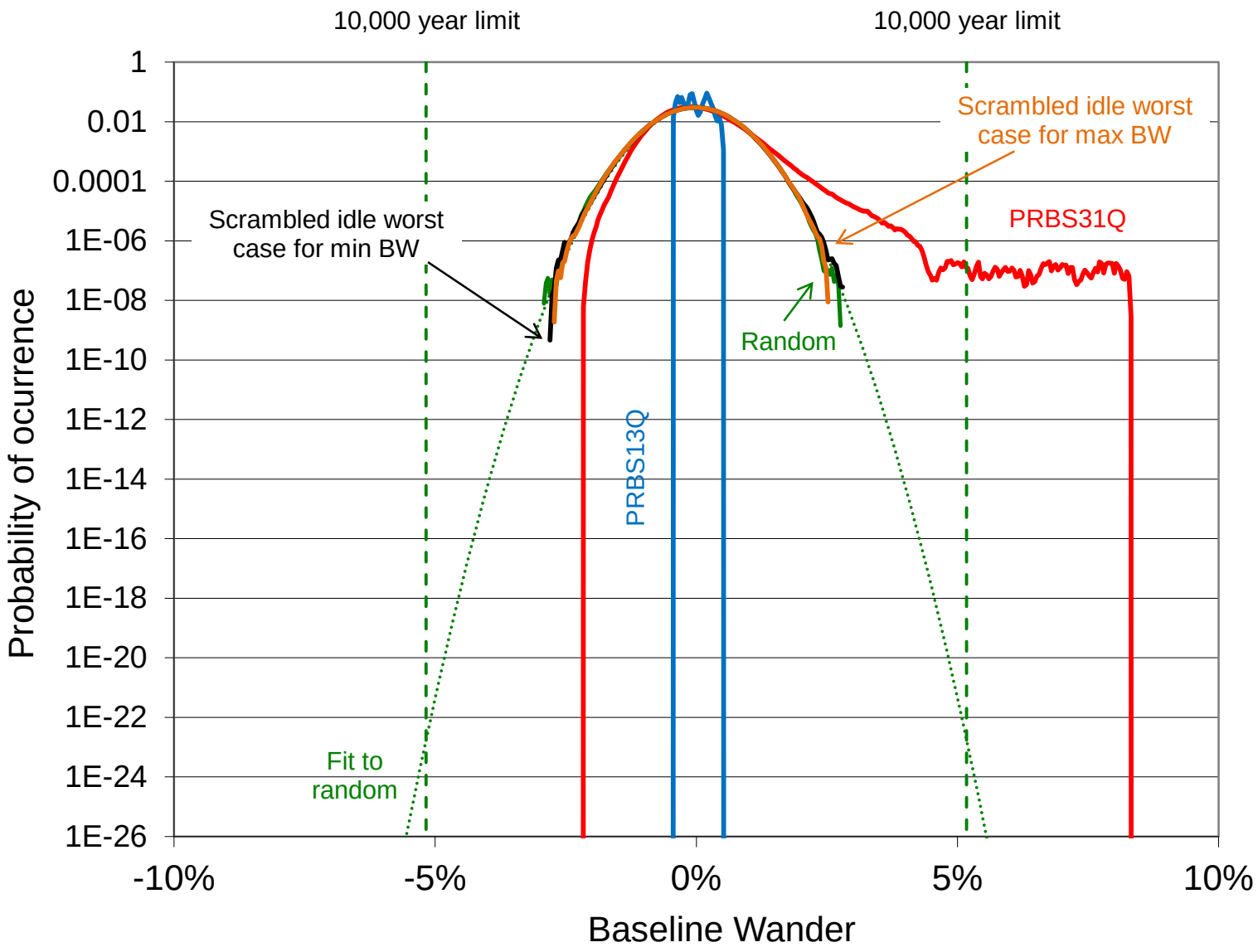
Scrambled idle construction

The scrambled idle symbol streams generated for this analysis were:

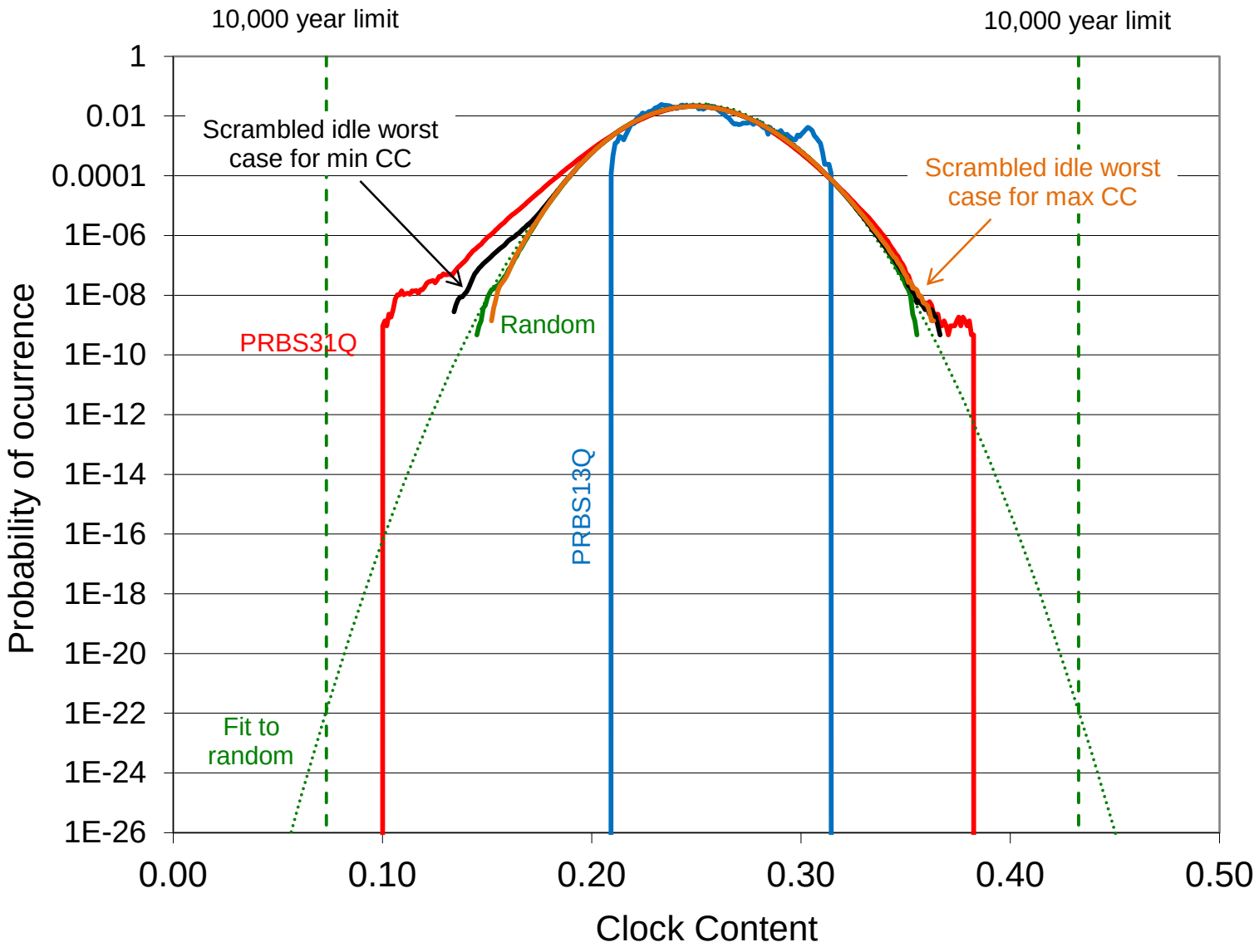
- Idle control characters
- 256B/257B transcoded
- Scrambled
- Distributed 10 bits at a time to two FEC codewords which start with alignment markers and 136 bits of PRBS9 one in every 8192 code words
- 300 bits of RS(544,514) FEC parity added
- Interleaved 10 bits at a time to form PCS lanes (option 8a)
- Bit interleaved with worst case PCS lane combinations and delays

The results for baseline wander and clock content are in slides 15 to 18 for 50 Gb/s lanes and slides 19 to 22 for 100 Gb/s lanes.

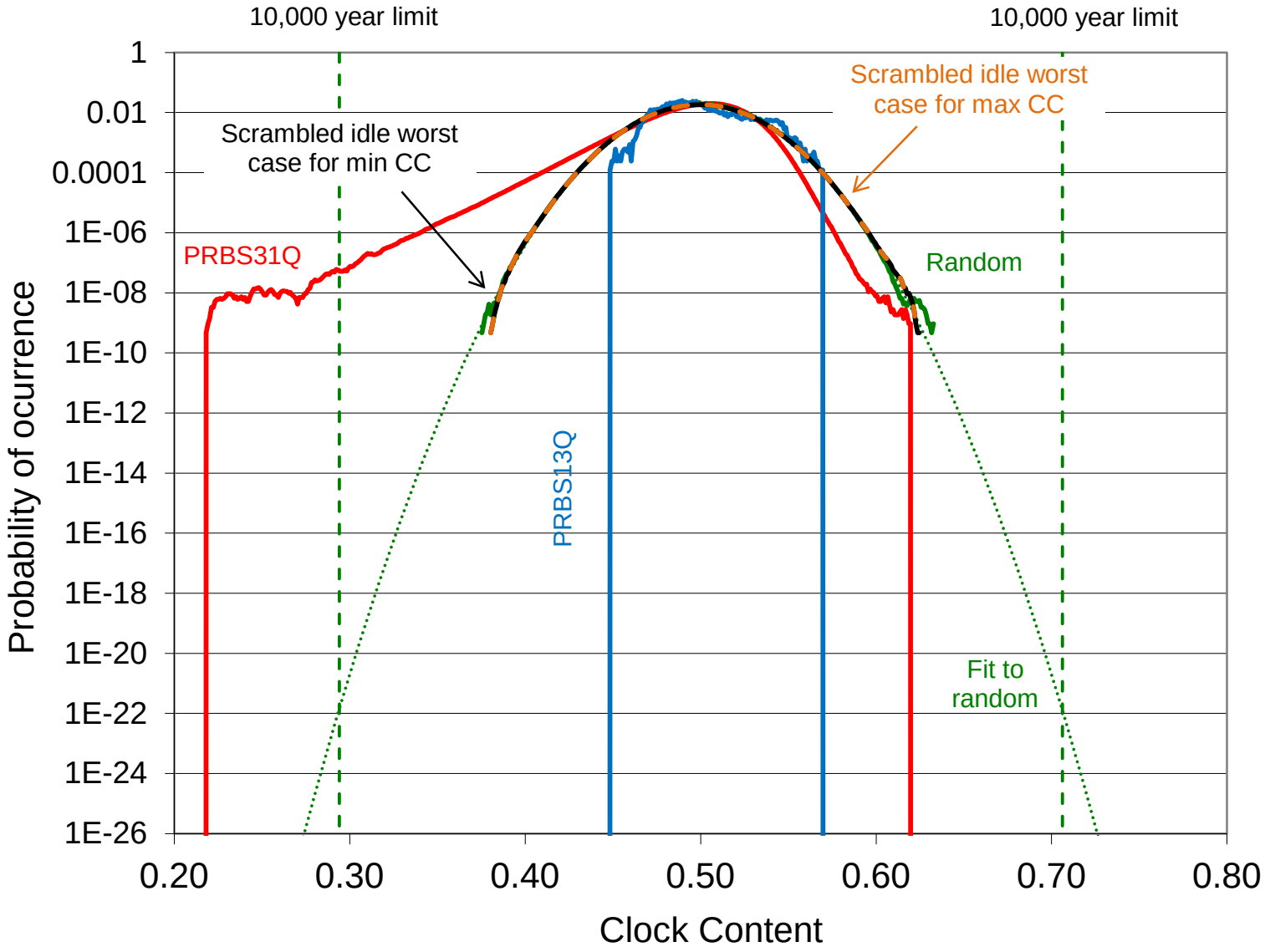
Baseline wander, 50G lanes



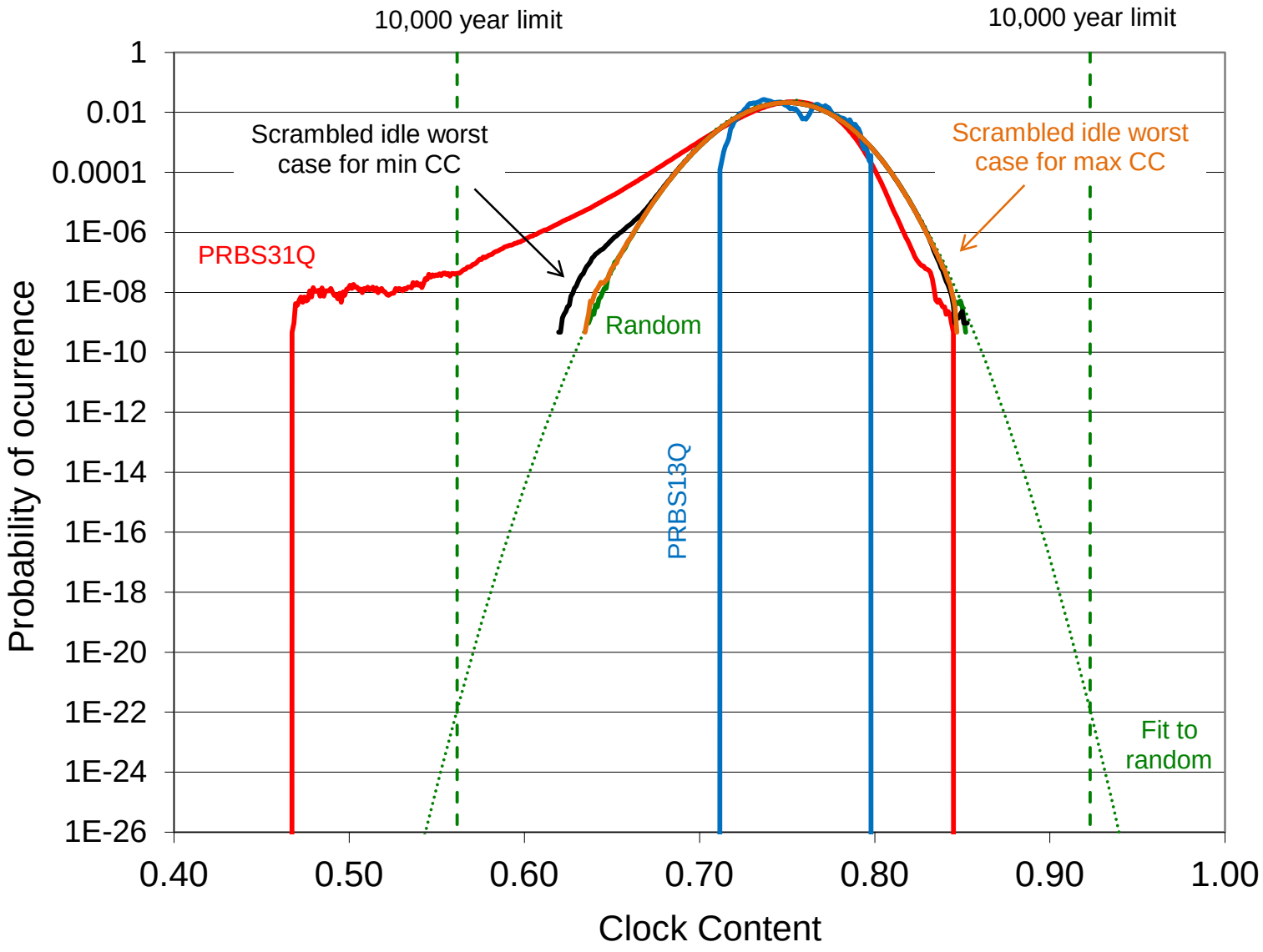
Clock, symmetric trans. through ave., 50G lanes



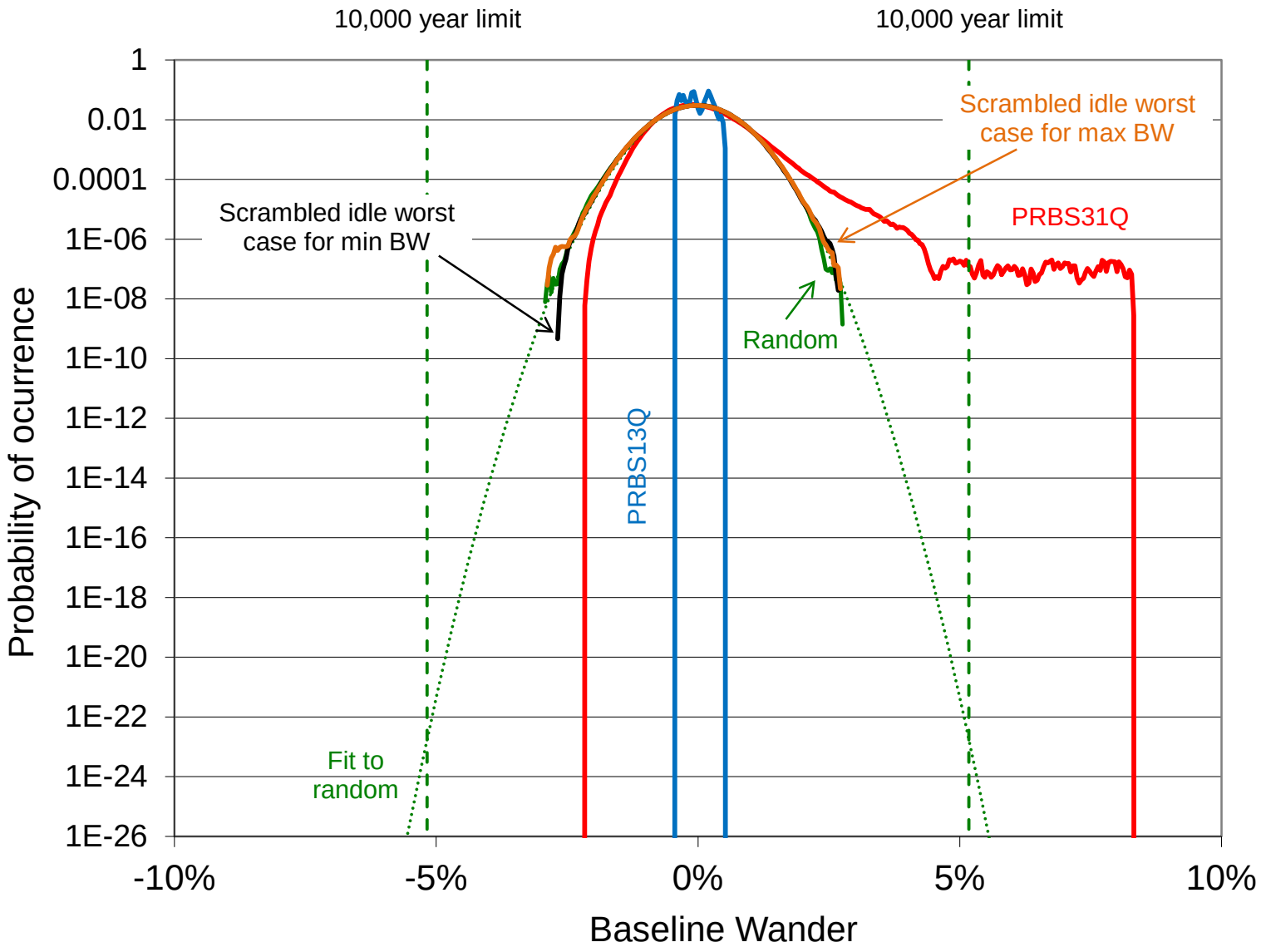
Clock, transitions through ave., 50G lanes



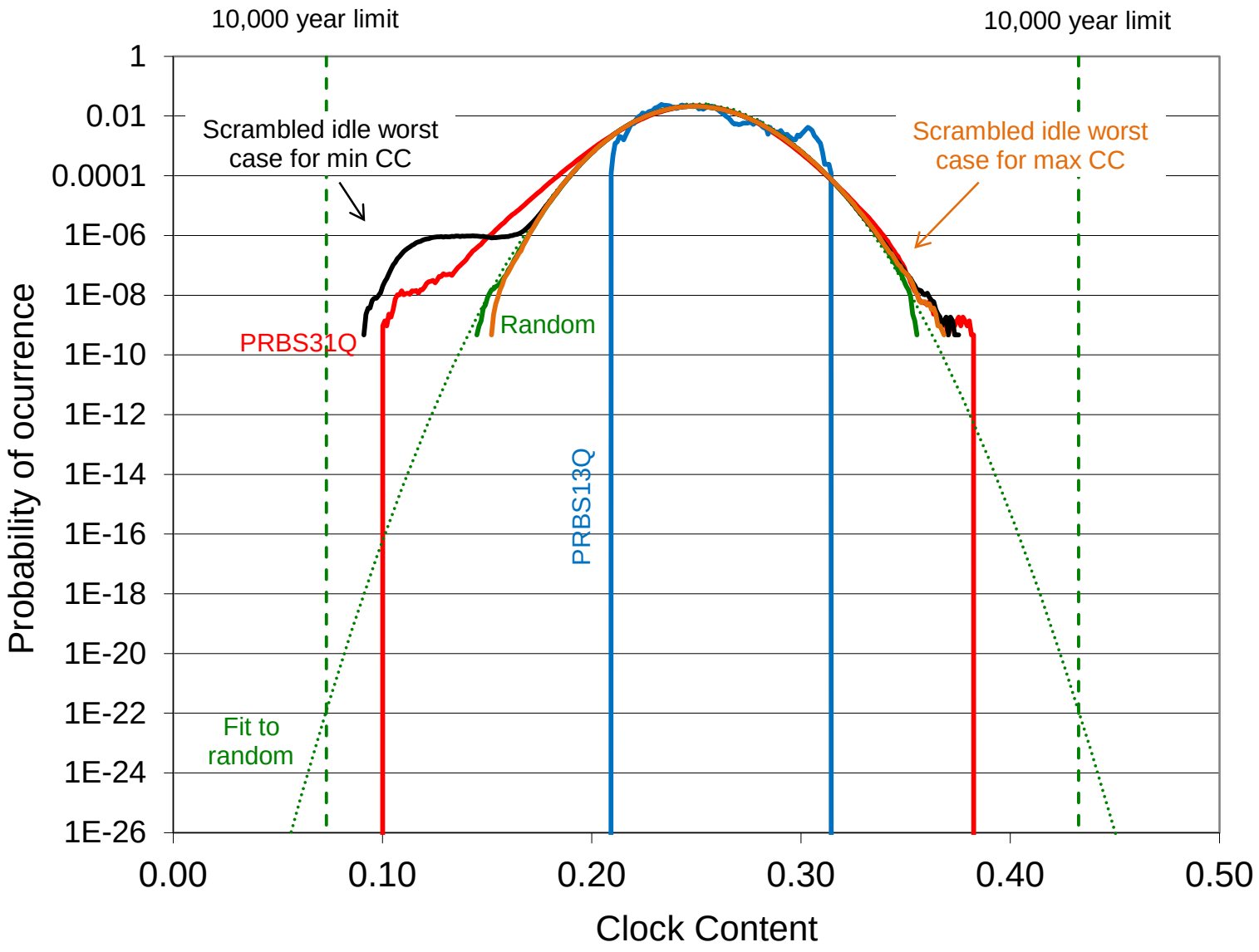
Clock, all transitions, 50G lanes



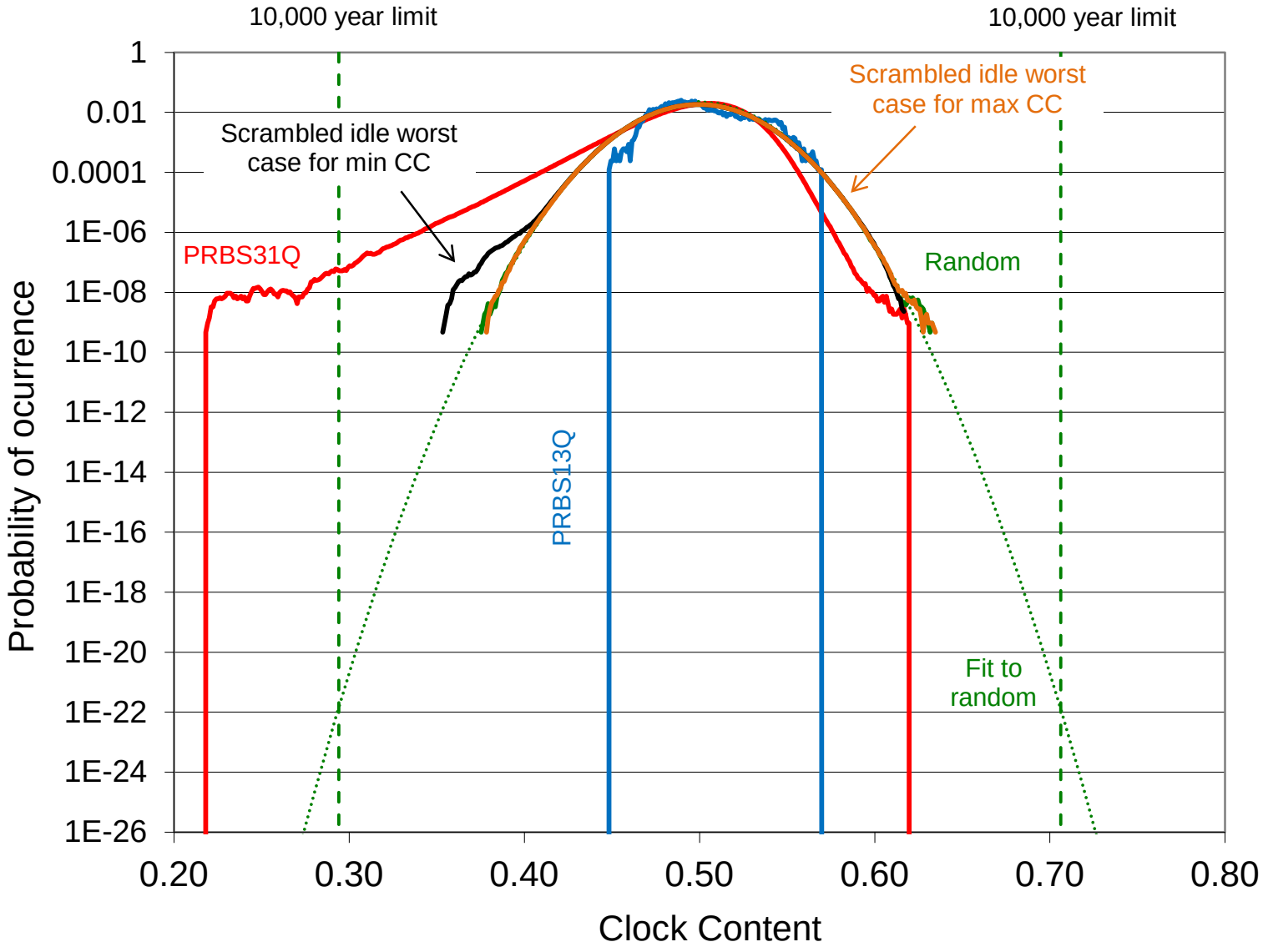
Baseline wander, 100G lanes



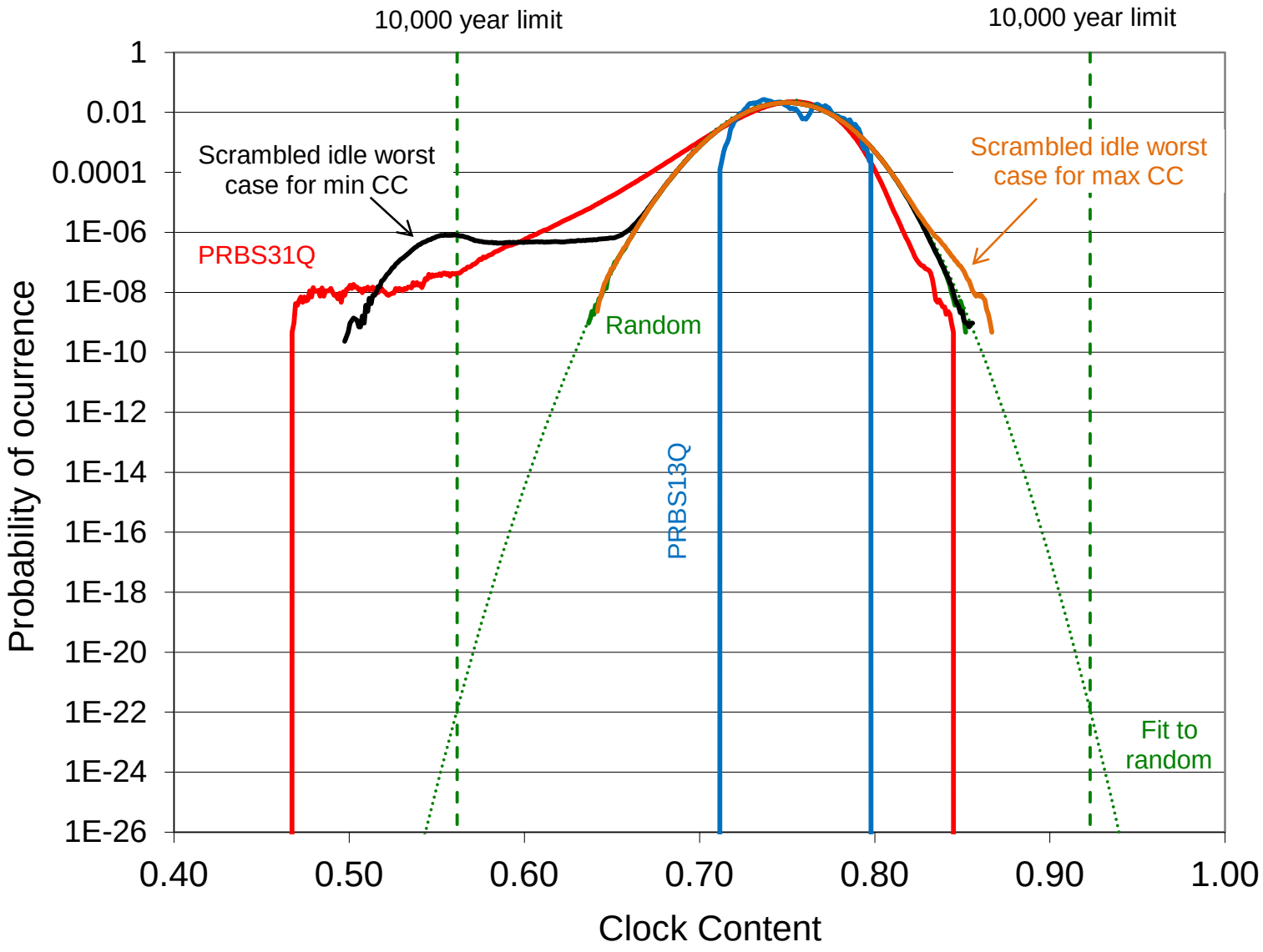
Clock, symmetric trans through ave., 100G lanes



Clock, transitions through ave., 100G lanes

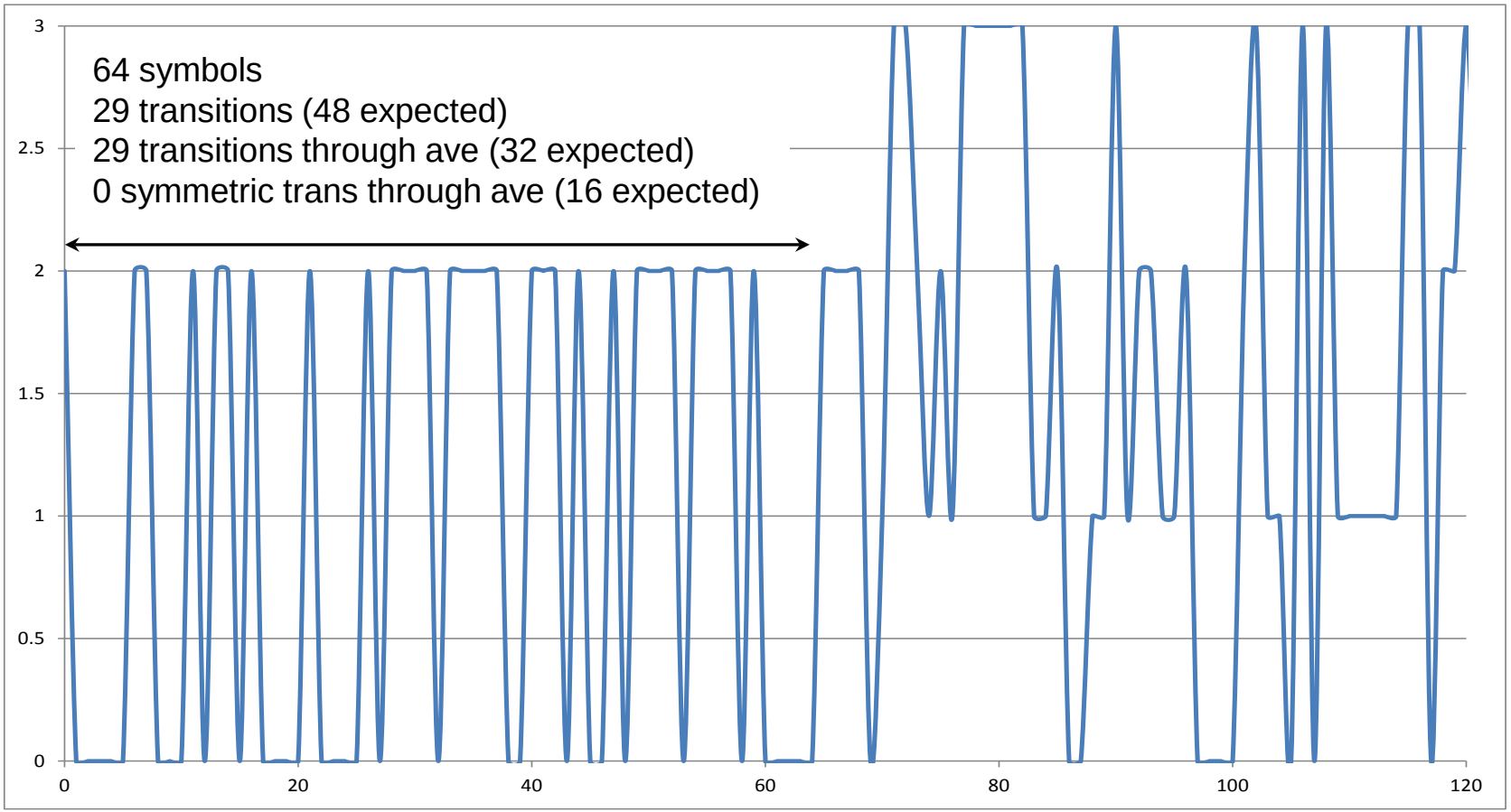


Clock, all transitions, 100G lanes



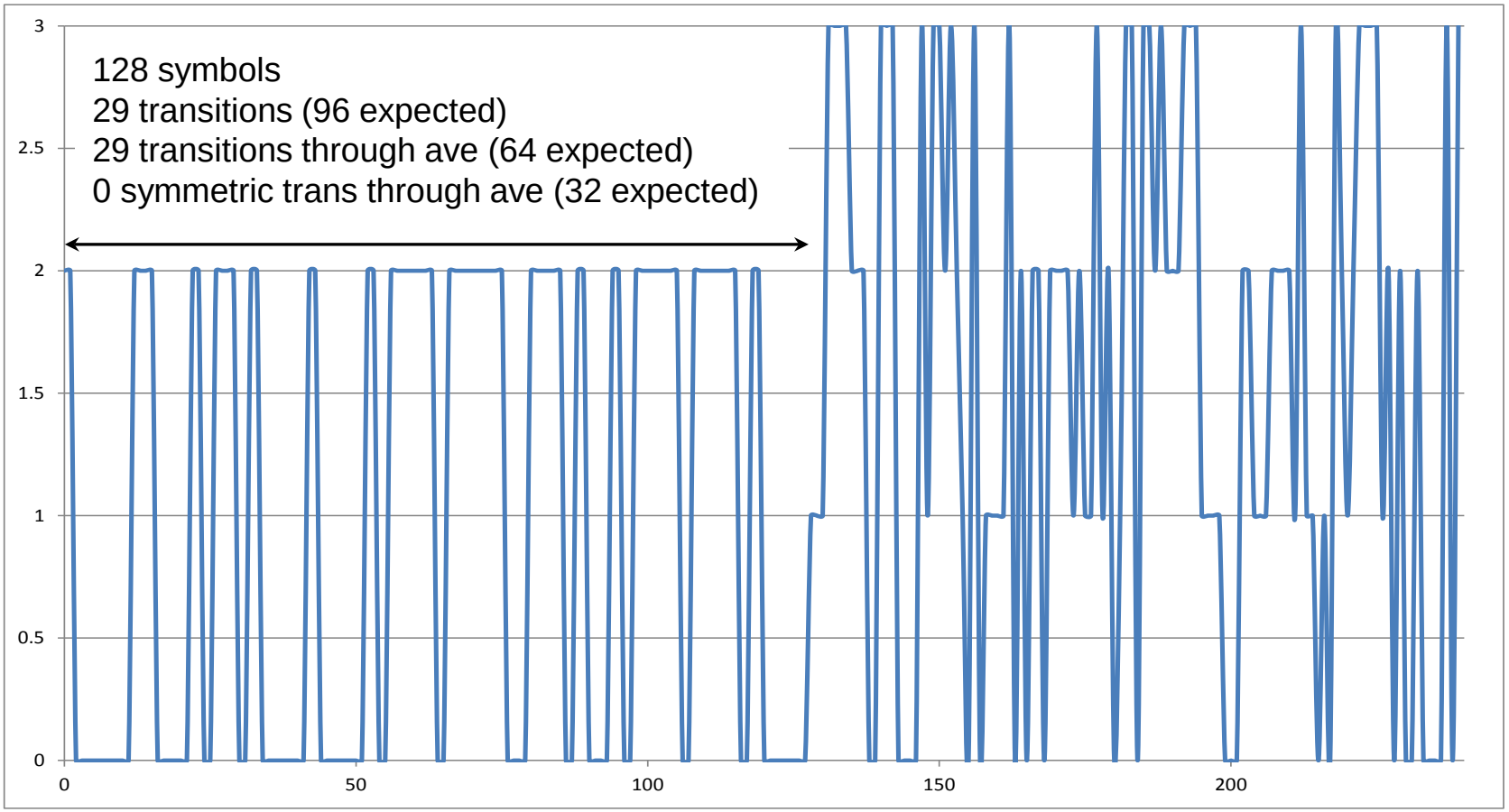
Effect of common part of lane marker, 2:1

Worst case clock content for all transitions, 50G lanes. Common part of alignment marker gives 64 symbols as below for zero skew:



Effect of common part of lane marker, 4:1

Worst case clock content for all transitions, 100G lanes. Common part of alignment marker gives 128 symbols as below for zero skew:



Conclusions

The baseline wander and clock content for 10,000 years of random data should be equalled or exceeded by test patterns used for BER testing.

PRBS31Q does this for all but the clock for symmetric transitions through the signal average, so it looks like a reasonable choice for a stressful test pattern.

PRBS13Q is much less stressful than either random data or scrambled idle, so is ok as a replacement for PRBS9, but is not suitable for BER related tests.

The common part of the 120-bit alignment markers causes a significant “shoulder” on the clock density plots for 4:1 bit interleaving for 100 Gb/s lanes.

Backup

Worst case lane combinations

2:1 bit interleaving for 50 Gb/s lanes

	First lane	Second lane	First lane delay	Second lane delay
wander_max	0	6	0	0
wander_min	3	7	0	32
clock25_max	8	11	0	-8
clock25_min	6	8	0	0
clock50_max	0	1	0	14
clock50_min	0	1	0	1
clock75_max	0	1	0	-24
clock75_min	0	11	0	0

4:1 bit interleaving for 100 Gb/s lanes

	First lane	Second lane	Third lane	Fourth lane	First lane delay	Second lane delay	Third lane delay	Fourth lane delay
wander_max	2	3	0	6	0	0	20	20
wander_min	6	14	3	7	0	11	-14	18
clock25_max	1	2	9	3	0	0	-12	-1
clock25_min	9	1	13	5	0	0	0	0
clock50_max	0	1	2	3	0	14	-12	17
clock50_min	1	0	9	2	0	1	0	1
clock75_max	3	13	9	0	0	-13	11	18
clock75_min	4	14	11	12	0	0	0	0

Thanks!