IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Logic Ad Hoc

February 16, 2017

Mark Gustlin - Xilinx

Meeting Notes

- **Any changes to the meeting minutes from the 1/26/16 call?**
- **Reminder of the patent policy: http://www.ieee802.org/3/patent.html**
  - Is anyone unfamiliar with it?
- Attendees names and affiliations will be taken from the Webex participants list. If you attend via phone only, or if your employer and affiliation are different, please send me an e-mail.
- **Logic ad hoc location:**

  http://www.ieee802.org/3/bs/public/adhoc/logic/index.shtml

Participation in IEEE 802 Meetings

All participation in IEEE 802 Working Group meetings is on an individual basis

- ***Participants in the IEEE standards development individual process shall act based on their qualifications and experience. (https://standards.ieee.org/develop/policies/bylaws/sb_bylaws.pdf section 5.2.1)***
- ***IEEE 802 Working Group membership is by individual; "Working Group members shall participate in the consensus process in a manner consistent with their professional expert opinion as individuals, and not as organizational representatives". (http://ieee802.org/PNP/approved/IEEE_802_WG_PandP_v19.pdf section 4.2.1)***
- **You have an obligation to act and vote as an individual and not under the direction of any other individual or group. Your obligation to act and vote as an individual applies in all cases, regardless of any external commitments, agreements, contracts, or orders.**
- **You shall not direct the actions or votes of any other member of an IEEE 802 Working Group or retaliate against any other member for their actions or votes within IEEE 802 Working Group meetings, see https://standards.ieee.org/develop/policies/bylaws/sb_bylaws.pdf section 5.2.1.3 and http://ieee802.org/PNP/approved/IEEE_802_WG_PandP_v19.pdf section 3.4.1, list item x**

By participating in IEEE 802 meetings, you accept these requirements. If you do not agree to these policies then you shall not participate.

Agenda

- **Restricted muxing option (update) - Mark Gustlin, Xilinx**
- **4 Lanes Muxing Limited Clock Content Analysis - Oded Wertheim, Mellanox**
- **Impact of Transition Density on CDR – Ali Ghiasi**

- Next proposed Logic ad hoc call:
  - Thursday 2/23/2017 7:30-9am PST

Thanks!