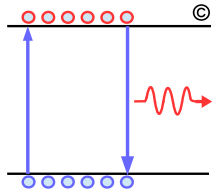


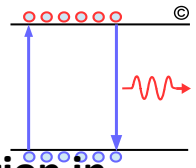
Impact of Transition Density on CDR

Ali Ghiasi

IEEE 802.3bs Logic Adhoc Meeting

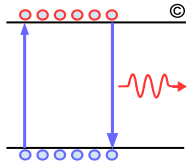
Feb 16th, 2017

Background

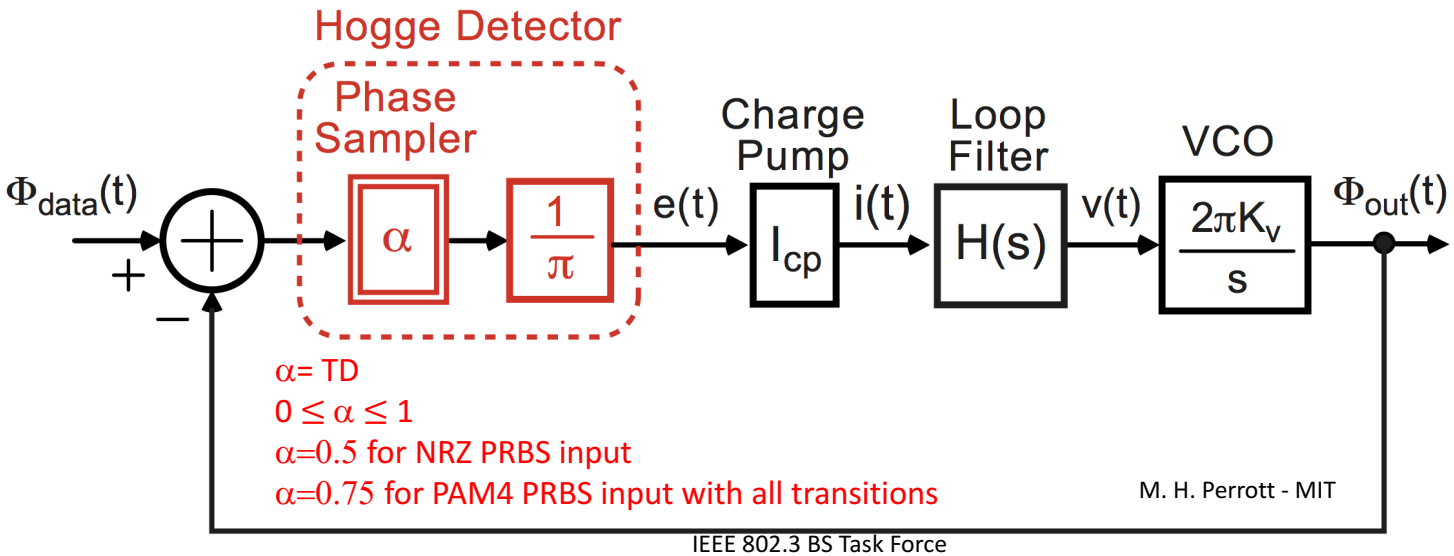


- **It has been identified that a certain PCS when muxed with specific delay causes reduction in transition density**
  - http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf
- **Above contributions analysis the clock content which reduces transition (TD) density based on transition type**
  - Symmetrical transition through the signal average – nominal TD 25% pathological PCS sequence results in 28% reduction in TD
  - All transitions through signal average – nominal TD 50% immune to TD reduction
  - All transitions – nominal TD 75% pathological PCS sequence results in 9% reduction in TD
- **This contribution analysis impact of transition density reduction on CDR operation given the CDR may use symmetrical transitions, all transitions through signal average, and all transitions.**

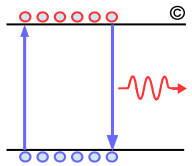
Basic Operation of the CDR



- **Key element of CDR are the phase detector, charge pump, loop filter and VCO**
  - Common implementation of phase detector is based on Hogge Detector where TD affects the loop gain and loop BW
  - $CDR\ BW = Nominal\ loop\ BW \times TD$
- A CDR designed for 802.3bs applications has a BW of 4 MHz assuming nominal PAM4 TD.

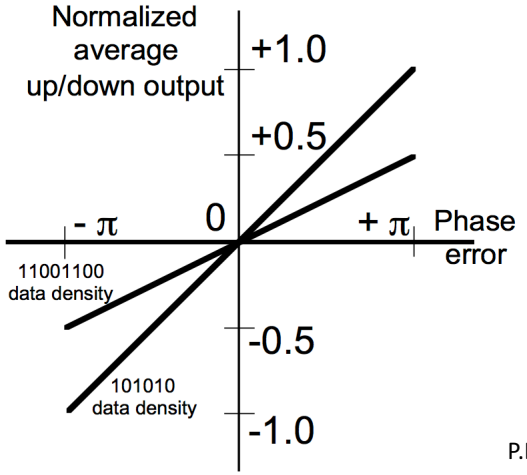


Transfer Characteristics of the Hogge Phase Detector

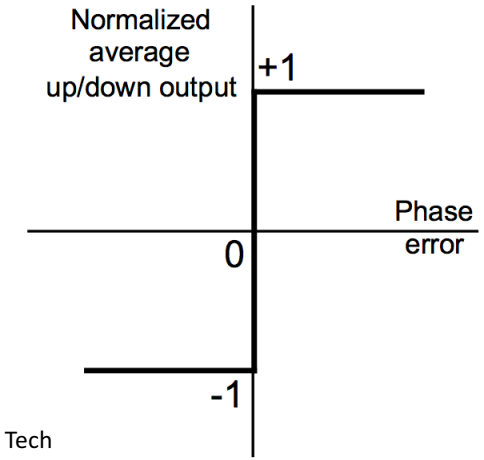


- **Example of linear and binary phase detector**
  - Linear phase detector response
    - Pattern 11001100 with TD=0.5 has gain of 0.5
    - Pattern 10101010 with TD=1.0 has gain of 1.0
- **A sophisticated CDR may have TD detector and accordingly adjust the loop gain to maintain target loop BW**
- **8B10B coding run length are limited to 5 bit but TD varies drastically or from 0.3 to 1.0!**

Linear Phase Detector

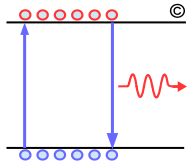


Binary Phase Detector



P.E. Allen-G. Tech

How Fibre Channel Guaranteed Interoperability Under Such Large TD Variation?



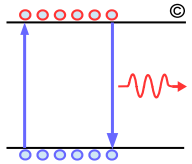
- **10's M of 1 Gig FC, 2 Gig FC, and 1 GbE products have been shipped where TD can vary from 0.3 to 1.0 based on 8B10B coding**
  - FC MJS group defined JTPAT which consist of low TD 7e pattern followed with high TD b5 pattern.

Table A.10 - JTPAT

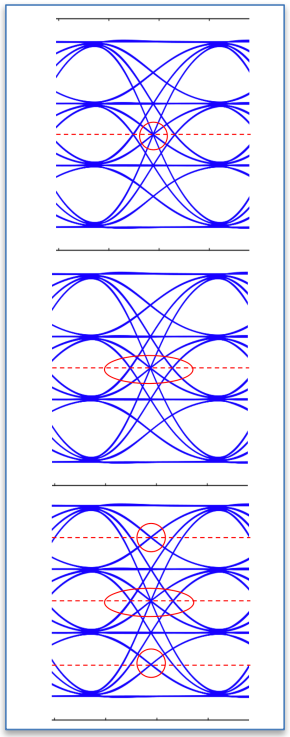
D30.3 (7e)			D30.3 (7e)		D30.3 (7e)			D30.3 (7e)	
0e1			31e		0e1			31e	
1000	0111	0001	1110	0011	1000	0111	0001	1110	0011
8	7	1	e	3	8	7	1	e	3
Byte = D30.3 is repeated > 167 times.									
D21.5 (b5)			D21.5 (b5)		D21.5 (b5)			D21.5 (b5)	
155			155		155			155	
1010	1010	1010	1010	1010	1010	1010	1010	1010	1010
a	a	a	a	a	a	a	a	a	a
Byte = D21.5 is repeated > 50 times.									

Fibre Channel - Methodologies for Jitter and Signal Quality Specification – MJSQ - 2004

PAM4 CDR Implementation



- **PAM4 CDR architecture is very similar to NRZ with addition of PAM4 to Binary convertor**



PAM4 to Binary Convertor

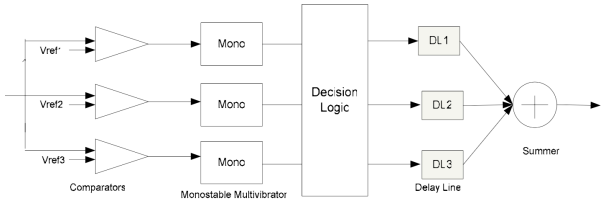
Simple PAM4 to Binary Convertor operating with 25% TD

PCS Pattern may Reduce TD to 0.18 Nominal CDR BW Reduces from 4 MHz to 2.88 MHz!

Simple PAM4 to Binary Convertor operating with 50% TD

PCS Pattern doesn't Change TD and CDR BW is not effected!

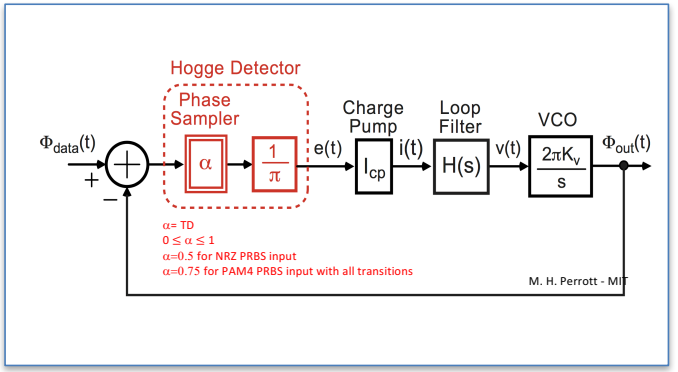
More robust implementation sampling all 3 eyes operating with 75% TD



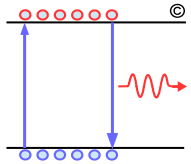
Kim, Proceeding IDEAS 2005

PCS Pattern may Reduce TD to 0.683 Nominal CDR BW Reduces from 4 MHz to 3.64 MHz!

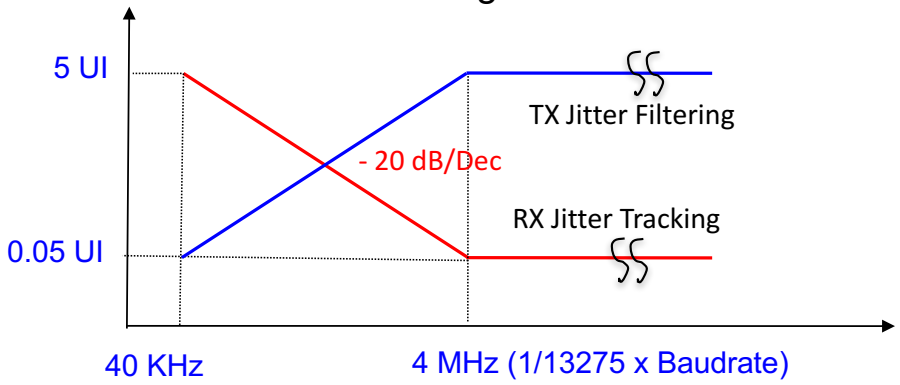
Generic CDR



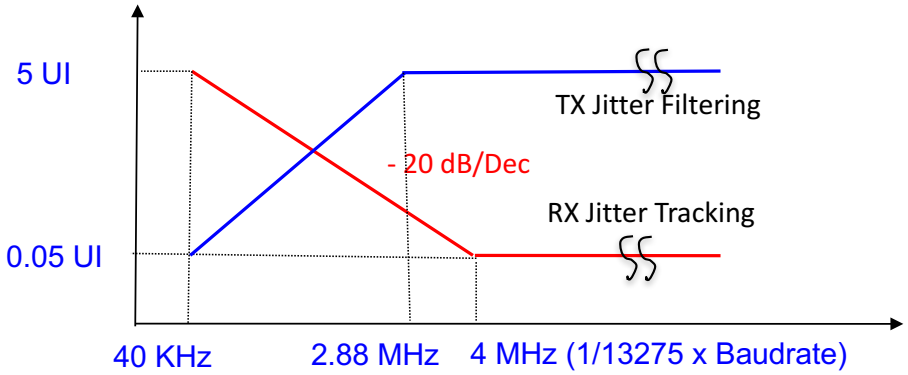
Accommodating TD Reduction with JTOL Test



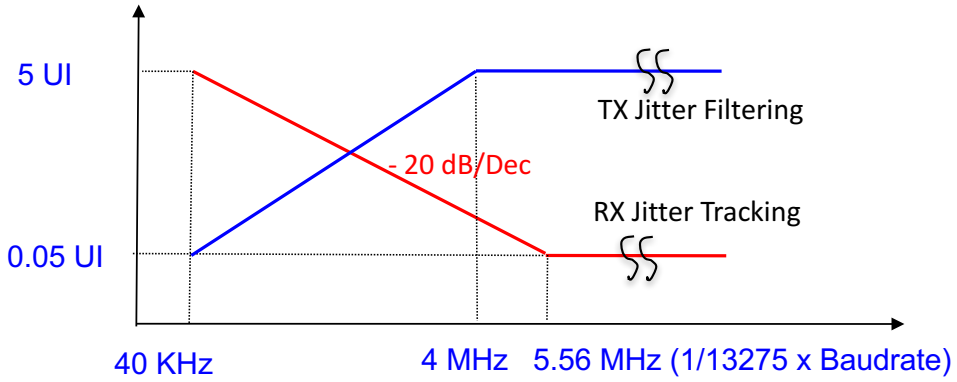
Current JTOL does not need to change if JTOL test include low TD data pattern



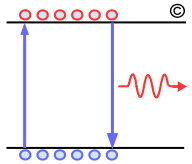
Option I: Tighten TX PLL filter but keep CDR BW at 4 MHz



Option II: Keep TX PLL BW at 4 MHz increase CDR BW to 5.56 MHz

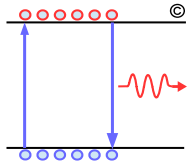


Compliance Method to Verify CDR Operation with Problematic Clock Content



- **The impact of TD reduction is reduction in the CDR BW from current 4 MHz**
  - A JTOL test with pathological PCS pattern or a weighted PRBS pattern would be sufficient to guarantee interoperability
- **An alternate approach but difficult to enforce or verify would be to require excess CDR BW given the CDR implementation**
  - CDR operating with symmetrical transition require nominal CDR BW of ~5.56 MHz
  - CDR operating with all transition through average not impacted by clock content
  - CDR operating with all transitions require only a BW of ~4.36 MHz
- **Require all CDR to have ~5.56 MHz BW while keeping TX golden PLL BW at 4 MHz does add extra burden form DSP implementations**
- **Keep CDR BW at 4 MHz but reduce transmitter golden PLL BW to ~2.88 MHz.**

Summary



- **Reduction in TD (transition density) will reduce the nominal CDR BW**
  - Reduction in CDR BW due to TD may result in JTOL failure, reduction in CDR margin, and/or BER
  - CDR BW is reduced proportional with reduction in TD
  - FC and 1 GbE links with 8b10B encoding have been operating reliably with much larger TD variation (0.3 to 1.0)
  - In comparisons an 802.3bs CDR operating on all transitions, TD drops by just 9% to 0.683!
- **Reduction in TD can be accommodated by the CDR in several ways**
  - Best option would be to add a JTOL test pattern consisting of nominal TD (0.75) section followed by low TD (0.683) section
    - We may still want to keep the PRBS31Q if the above test pattern is not as long
    - Nominal CDR corner frequency stays at current 4 MHz
  - Reduce TX golden PLL corner frequency to ~2.88 MHz and keep the 4 MHz CDR BW to allow CDR implementation based on 25%, 50%, or 75% TD
    - Does not require testing with low TD data pattern but tighten transmit jitter unnecessarily for cases where CDR operates with 50% and 75% TD nominally
  - Keep TX golden PLL corner frequency at 4 MHz and increase the CDR BW to ~5.56 MHz to allow CDR implementation based on 25%, 50%, or 75% TD
    - Does not require testing with low TD data pattern but forces CDR operating with 50% and 75% TD unnecessarily to have excess BW
    - If allowed CDR implementation must use all transition then CDR corner frequency only needs to increase to 4.36 MHz – but how do we enforce it!
- **Any of the above approaches could address clock content issue.**