

400GbE AMs revised proposal

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IEEE P802.3bs Task Force, Logic Ad Hoc, 23 February 2016

Introduction

A set of alignment markers for 400GbE was proposed in [anslow_01_1215_logic](#). The worst case performance of the proposed codes was analysed for 4:1 bit interleaving for 100 Gb/s lanes and found to have a large “shoulder” on the clock content for “all transitions” (page 22).

A revised proposal was analysed in [anslow_01_0116_logic](#) with adequate performance, but this proposal had issues with 10-bit symbol boundaries.

A proposal to change the bit positions of the alignment markers was made on page 7 of [gustlin_01_0216_logic](#)

This contribution analyses the performance of this further revised proposal.

Baseline wander

Previous NRZ contributions have used a “baseline wander” parameter

This was defined as:

Baseline wander is the instantaneous offset (in %) in the signal generated by AC coupling at the Baud rate / 10,000.

This analysis re-uses this definition unmodified, but it should be noted that for PAM4, the eye height is 1/3 that of NRZ so the effects of a given amount of baseline wander will be greater.

For NRZ contributions see:

P802.3ba [anslow_01_0108](#)

P802.3ba [anslow_06_1108](#)

P802.3bj [anslow_01a_0112](#)

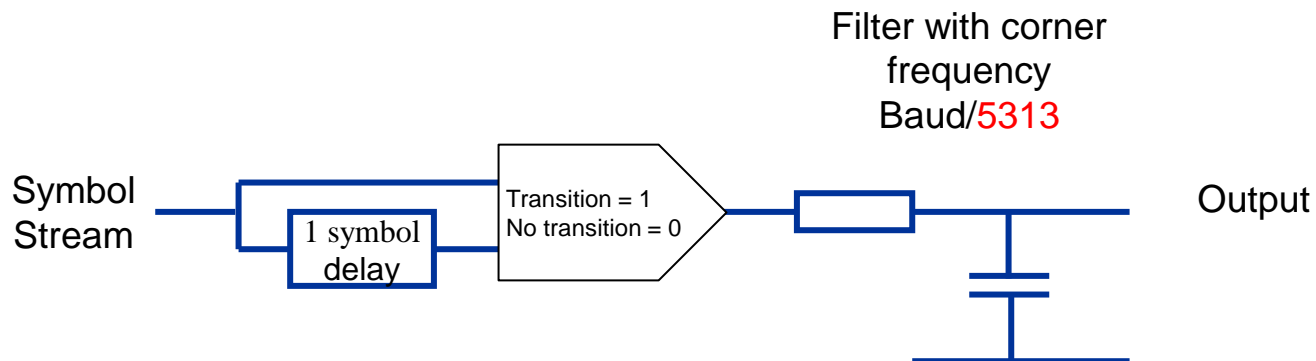
Clock content

The “clock content” parameter is defined here as:

Create a function which is a 1 for a transition and a 0 for no transition and then filter the resulting sequence with a corner frequency of Baud/5313.

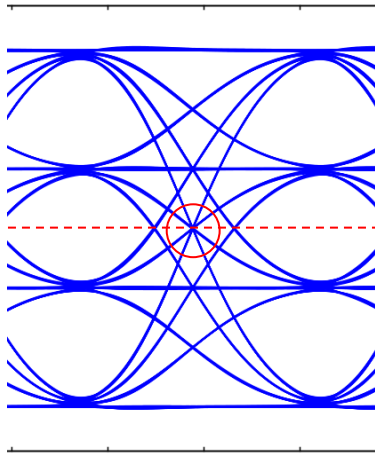
This analysis defines a transition as one of three possibilities (as per [healey_3bs_01_1115](#)):

- Symmetrical transitions through the signal average
- Transitions through the signal average
- All transitions

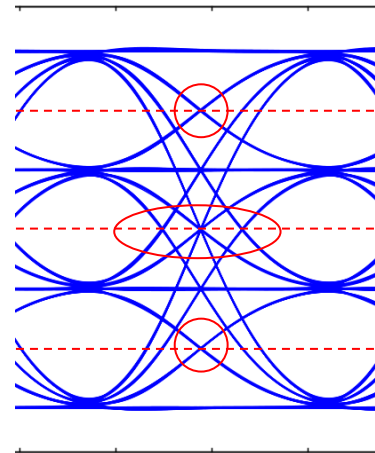
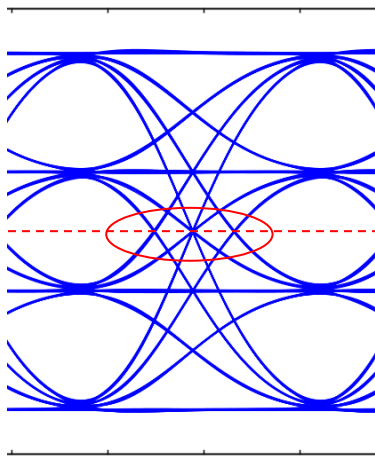


Clock content illustration

Symmetrical
transitions
through the
signal average



Transitions
through the
signal average



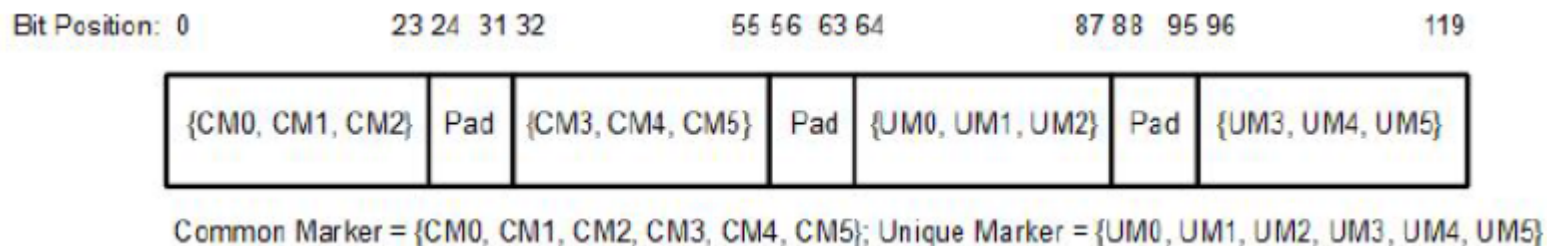
All transitions

Revised alignment markers

This contribution proposes 96-bit alignment markers with a 48-bit common part of “0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9” followed by a 48-bit unique part.

The 48-bit unique parts of the alignment markers are composed of the first three bytes of the unique parts in [anslow_01_1215_logic](#) followed by their inverse.

The alignment markers include PRBS9 pad bits as per:



(figure courtesy A. Butter)

The proposed markers are shown on the next page and the PRBS9 bit order on the following page.

Revised alignment marker proposal

Table 119–1—400GBASE-R Alignment marker encodings

PCS lane number	Encoding ^a {CM ₀ , CM ₁ , CM ₂ , CM ₃ , CM ₄ , CM ₅ , UM ₀ , UM ₁ , UM ₂ , UM ₃ , UM ₄ , UM ₅ }
0	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x9E, 0xEB, 0x27, 0x61, 0x14, 0xD8
1	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x50, 0x74, 0x88, 0xAF, 0x8B, 0x77
2	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0xB4, 0xB7, 0xEA, 0x4B, 0x48, 0x15
3	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0xE4, 0xFB, 0xF1, 0x1B, 0x04, 0x0E
4	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0xDC, 0x58, 0xEE, 0x23, 0xA7, 0x11
5	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0xBD, 0xA9, 0xBF, 0x42, 0x56, 0x40
6	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x97, 0x67, 0x77, 0x68, 0x98, 0x88
7	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x24, 0x35, 0xA5, 0xDB, 0xCA, 0x5A
8	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x57, 0x64, 0x51, 0xA8, 0x9B, 0xAE
9	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x28, 0xF9, 0x3E, 0xD7, 0x06, 0xC1
10	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0xCB, 0xD1, 0xAD, 0x34, 0x2E, 0x52
11	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x5E, 0x1E, 0x38, 0xA1, 0xE1, 0xC7
12	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x19, 0x98, 0xF9, 0xE6, 0x67, 0x06
13	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x84, 0xEC, 0x20, 0x7B, 0x13, 0xDF
14	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x13, 0xA4, 0xED, 0xEC, 0x5B, 0x12
15	0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9, 0x3F, 0x8A, 0xBE, 0xC0, 0x75, 0x41

^aEach octet is transmitted LSB to MSB.

PRBS9 bit order

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Codeword A	bit number →	0	0	10	10	20	20	30	30	40	40	50	50	60	60	70	70
		1	1	11	11	21	21	31	31	41	41	51	51	61	61	71	71
		2	0	12	12	22	22	32	32	42	42	52	52	62	62	72	72
		3	1	13	13	23	23	33	33	43	43	53	53	63	63	73	73
		4	1	14	14	24	24	34	34	44	44	54	54	64	64	74	74
		5	0	15	15	25	25	35	35	45	45	55	55	65	65	75	75
		6	0	16	16	26	26	36	36	46	46	56	56	66	66	76	76
		7	1	17	17	27	27	37	37	47	47	57	57	67	67	77	77
		8	0	18	18	28	28	38	38	48	48	58	58	68	68	78	78
		9	1	19	19	29	29	39	39	49	49	59	59	69	69	79	79
Codeword B	bit number →	80	0	90	90	100	100	110	110	120	120	130	130	140	140	150	150
		81	1	91	91	101	101	111	111	121	121	131	131	141	141	151	151
		82	0	92	92	102	102	112	112	122	122	132	132	142	142	152	152
		83	0	93	93	103	103	113	113	123	123	133	133	143	143	153	153
		84	1	94	94	104	104	114	114	124	124	134	134	144	144	154	154
		85	0	95	95	105	105	115	115	125	125	135	135	145	145	155	155
		86	0	96	96	106	106	116	116	126	126	136	136	146	146	156	156
		87	1	97	97	107	107	117	117	127	127	137	137	147	147	157	157
		88	1	98	98	108	108	118	118	128	128	138	138	148	148	158	158
		89	0	99	99	109	109	119	119	129	129	139	139	149	149	159	159
		160	0	170	170	180	180	190	190	200	200	210	210	220	220	230	230
		161	1	171	171	181	181	191	191	201	201	211	211	221	221	231	231
		162	0	172	172	182	182	192	192	202	202	212	212	222	222	232	232
		163	0	173	173	183	183	193	193	203	203	213	213	223	223	233	233
		164	0	174	174	184	184	194	194	204	204	214	214	224	224	234	234
		165	1	175	175	185	185	195	195	205	205	215	215	225	225	235	235
		166	2	176	176	186	186	196	196	206	206	216	216	226	226	236	236
		167	3	177	177	187	187	197	197	207	207	217	217	227	227	237	237
		168	4	178	178	188	188	198	198	208	208	218	218	228	228	238	238
		169	5	179	179	189	189	199	199	209	209	219	219	229	229	239	239
	240	98	250	250	260	260	270	270	280	280	290	290	300	300	310	310	
	241	99	251	251	261	261	271	271	281	281	291	291	301	301	311	311	
	242	1	252	252	262	262	272	272	282	282	292	292	302	302	312	312	
	243	0	253	253	263	263	273	273	283	283	293	293	303	303	313	313	
	244	1	254	254	264	264	274	274	284	284	294	294	304	304	314	314	
	245	0	255	255	265	265	275	275	285	285	295	295	305	305	315	315	
	246	0	256	256	266	266	276	276	286	286	296	296	306	306	316	316	
	247	1	257	257	267	267	277	277	287	287	297	297	307	307	317	317	
	248	1	258	258	268	268	278	278	288	288	298	298	308	308	318	318	
	249	0	259	259	269	269	279	279	289	289	299	299	309	309	319	319	

Marker bit value

PRBS9 bit number

⋮

Simulations

Using these alignment codes, all possible combinations of PCS lanes for 4:1 bit interleaving for 100 Gb/s lanes were then analysed to find the worst cases for Baseline Wander (BW) and Clock Content (CC) after Gray coding to PAM4 symbols. These searches included lane delays of -20 to +20 as per the previous analysis for the 4:1 case.

The worst case PCS lane combinations and delays were then used to generate the worst case PDFs for 400 GbE scrambled idle 100 Gb/s lanes.

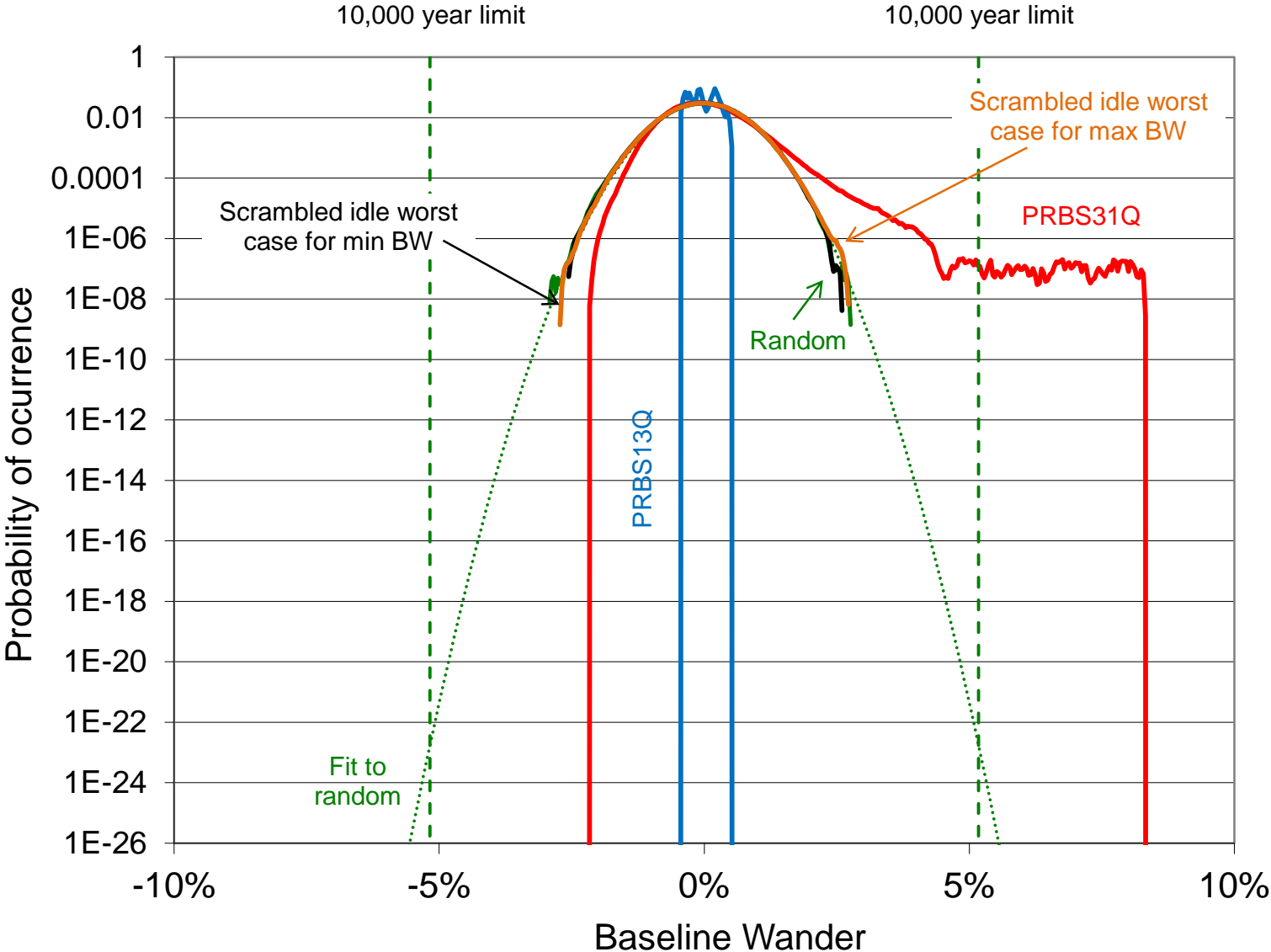
Scrambled idle construction

The scrambled idle symbol streams generated for this analysis were:

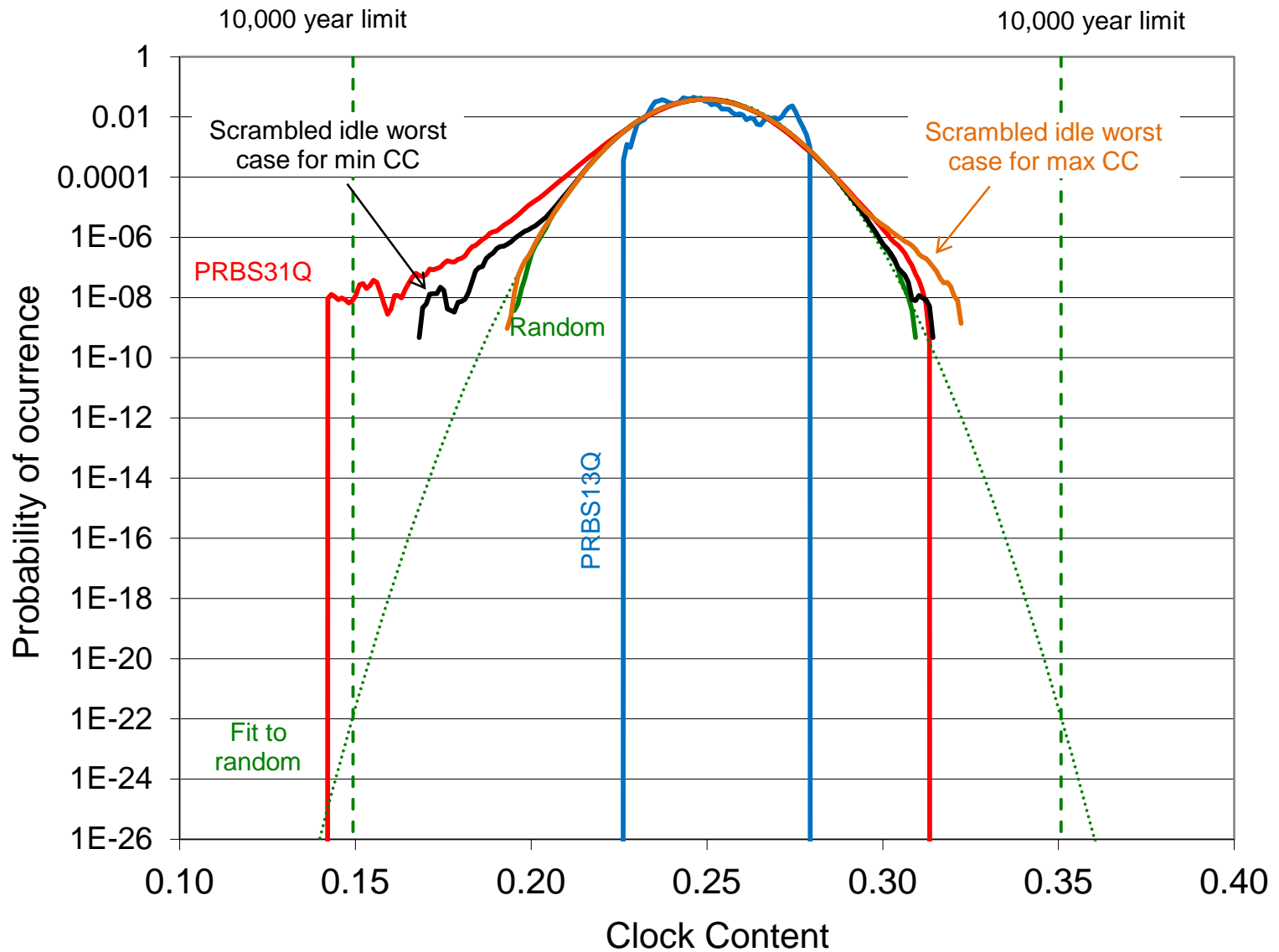
- Idle control characters
- 256B/257B transcoded
- Scrambled
- Distributed 10 bits at a time to two FEC codewords which start with alignment markers PRBS9 one in every 8192 code words
- 300 bits of RS(544,514) FEC parity added
- Interleaved 10 bits at a time to form PCS lanes (option 8a)
- Bit interleaved with worst case PCS lane combinations and delays

The results for baseline wander and clock content are in the following slides.

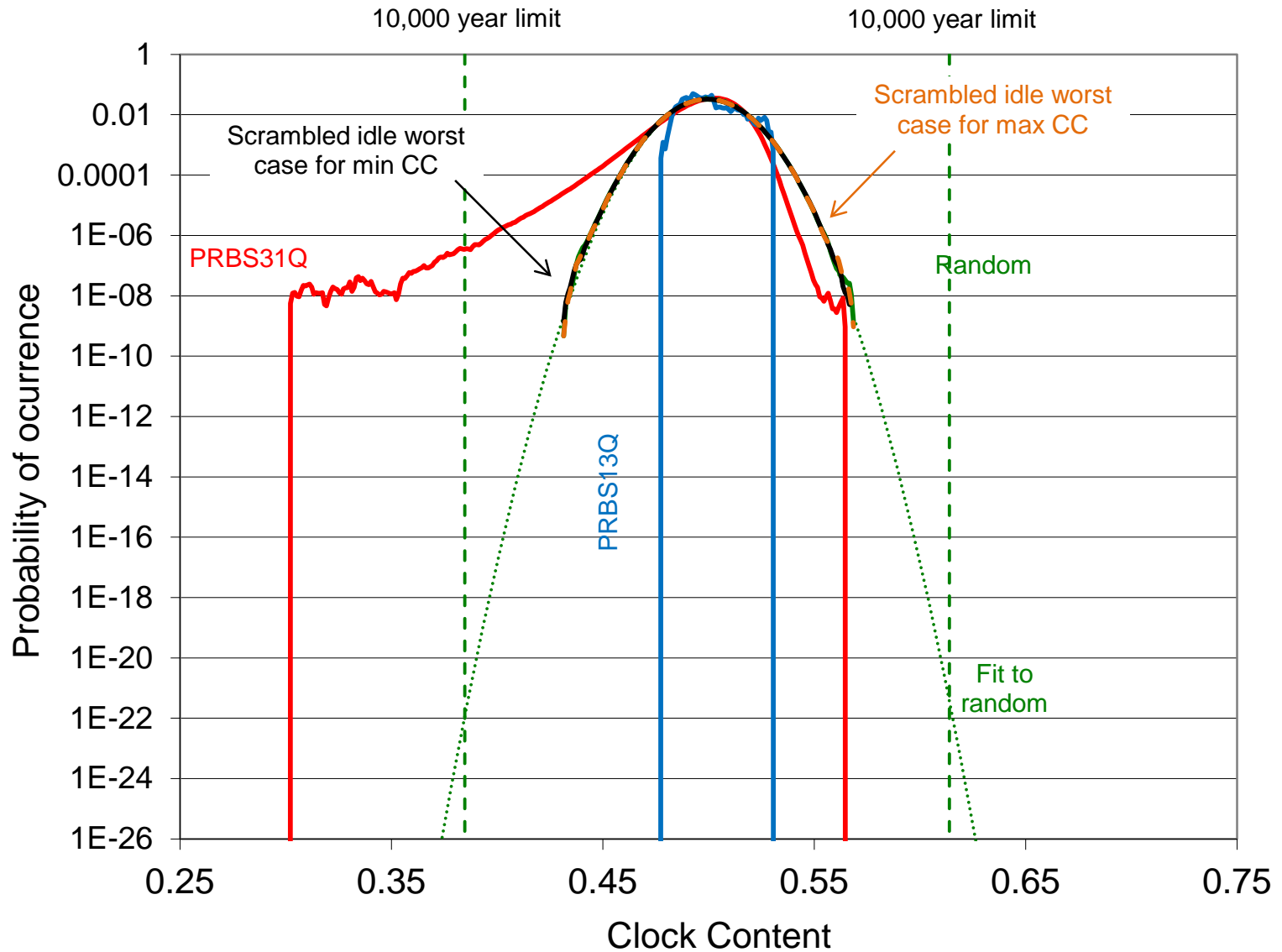
Baseline wander, 100G lanes



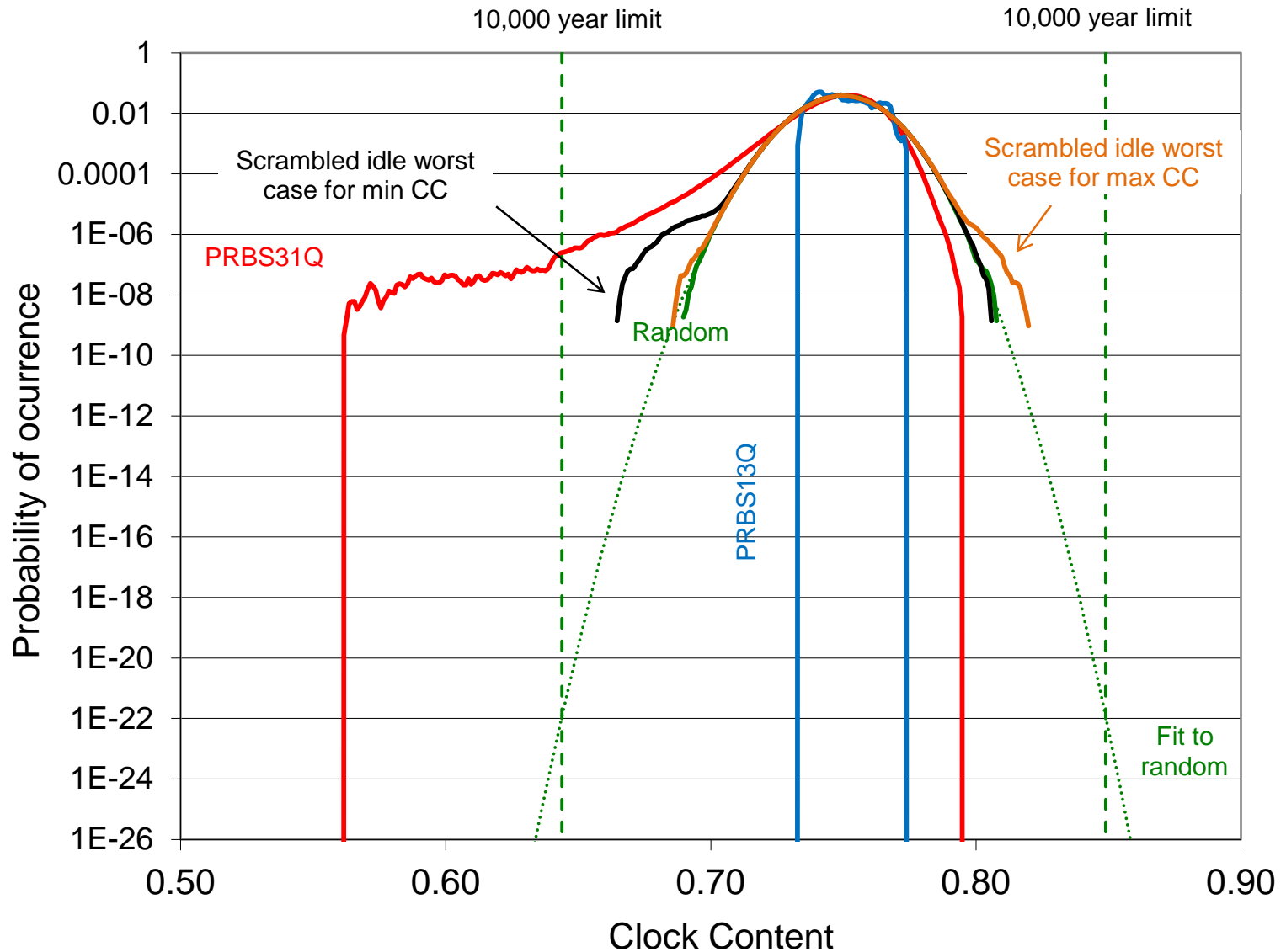
Clock, sym trans through ave, 100G lanes



Clock, trans through ave, 100G lanes



Clock, all transitions, 100G lanes



Conclusion

The baseline wander and clock content for the revised alignment marker proposal still show a “shoulder”, but they remain within the baseline wander and clock content for the PRBS31Q test pattern.

It is therefore proposed to use this alignment marker scheme for 400 Gb/s Ethernet.

Backup

Worst case lane combinations revised proposal

4:1 bit interleaving for 100 Gb/s lanes

	First lane	Second lane	Third lane	Fourth lane	First lane delay	Second lane delay	Third lane delay	Fourth lane delay
wander_max	5	15	8	6	0	0	20	20
wander_min	5	13	6	0	0	-1	20	-12
clock25_max	5	6	13	0	0	2	-2	1
clock25_min	0	13	5	15	0	0	0	0
clock50_max	1	0	3	2	0	-1	-6	12
clock50_min	5	0	15	1	0	15	0	17
clock75_max	1	4	15	10	0	-1	-2	0
clock75_min	0	12	6	11	0	0	0	0

Thanks!