Skew in 400GbE

IEEE P802.3bs 400 Gb/s Ethernet Task Force

Introduction

- Draft 1.2 currently have all skew numbers in magenta
- The values are all copied directly from 100GbE
- This looks at 400GbE and should we leave the numbers as is or change them?

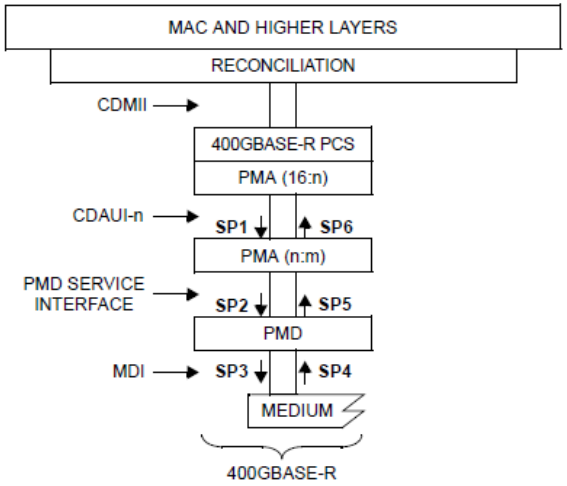
Draft 1.2 Skew Table

- Numbers straight from 100GbE
- Original numbers from: http://www.ieee802.org/3/ba/public/jul08/giannakopoulos_01_0708.pdf

Table 116–4—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 400GBASE-R PCS lane (UI)[b]	Notes[c]
SP1	29	≈ 770	See 120.5.3.1
SP2	43	≈ 1142	See 120.5.3.3, 121.3.2, 122.3.2, or 123.3.2
SP3	54	≈ 1434	See 121.3.2, 122.3.2, or 123.3.2
SP4	134	≈ 3559	See 121.3.2, 122.3.2, or 123.3.2
SP5	145	≈ 3852	See 121.3.2, 122.3.2, or 123.3.2
SP6	160	≈ 4250	See 120.5.3.5
At PCS receive	180	≈ 4781	See 119.2.5.1

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI for 400GBASE-R, based on 1 UI equals 37.64706 ps at PCS lane signaling rate of 26.5625 GBd.
[c]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.



Draft 1.2 Skew Variation Table

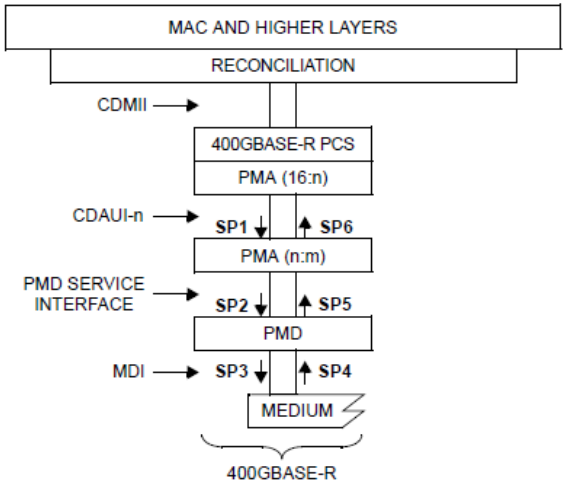
- Numbers straight from 100GbE
- Original numbers from: http://www.ieee802.org/3/ba/public/jul08/giannakopoulos_01_0708.pdf

Table 116–5—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 26.5625 GBd PMD lane (UI)[a]	Notes[b]
SP1	0.2	≈ 5	See 120.5.3.1
SP2	0.4	≈11	See 120.5.3.3, 121.3.2, 122.3.2, or 123.3.2
SP3	0.6	≈ 16	See 121.3.2, 122.3.2, or 123.3.2
SP4	3.4	≈ 90	See 121.3.2, 122.3.2, or 123.3.2
SP5	3.6	≈ 96	See 121.3.2, 122.3.2, or 123.3.2
SP6	3.8	≈ 101	See 120.5.3.5
At PCS receive	4	≈ 106	See 119.2.5.1

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 400GBASE-R, based on 1 UI equals 37.64706 ps at PMD lane signaling rate of 26.5625 GBd.

[b]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.



PMD Skew

- Below are the numbers for current PMDs
- Max skew of 79ns, the current budget for SP3 to SP4 is 80ns, so just 1ns of margin here
- Max Dynamic skew is 2.4ns, budget is 2.8ns for SP3 to SP4, so just 0.4ns of margin
  - Though it is suspected that the 100G-PSM4 spec set their numbers just under the 100G spec is does not reflect what is really needed
- So recommend keeping SP3 to SP4 numbers as is (and changing to black from magenta)

PMD	Description	Max Skew	Max Dynamic Skew
400GBASE-SR16[1]	100M MMF	4.537ns (120.5 UI)	0.676ns (18UI)
400GBASE-LR8[2]	10k SMF	1.19ns (63.3UI)	0.13ns 6.8UI
400GBASE-DR4[3]	500M SMF	79ns	2.4ns

1. From Jonathan King, based on Paul Kolesar's model
2. From anslow_02_0216_smf.xls
3. From Brian Welch, 100G-PSM4-Specification-2.0.pdf

Work to be Done

- Look at skew and skew variation at other skew points
  - My inclination for the skew is to leave them as is, 4.7kb x 16 lanes = 75kb of memory, very trivial for an ASIC or FPGA
- Does anyone have data? Should we revisit the skew variation at other skew points?

Thanks!