Restricted muxing option (natural pairs)

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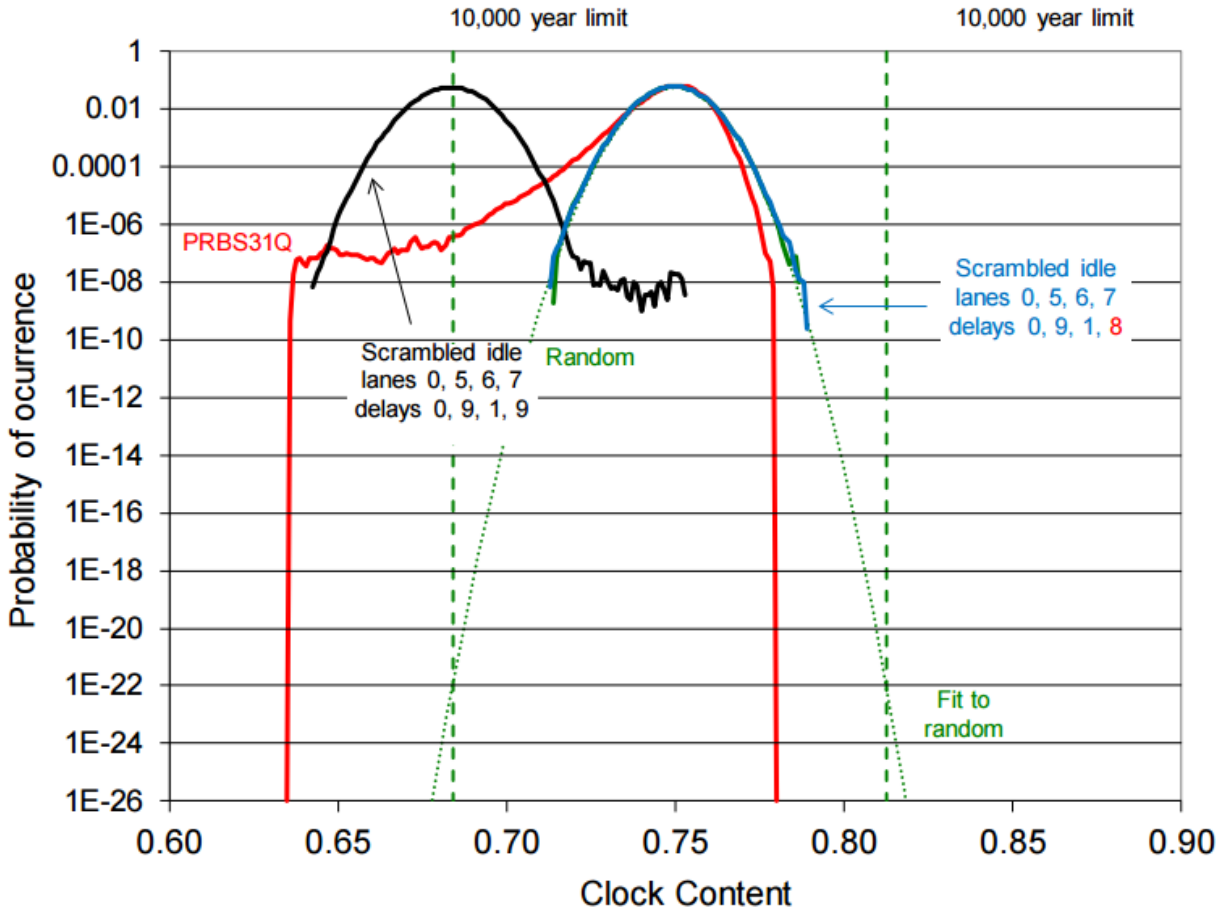
Overview

- Pete Anslow shared the clock content issue, originally found by Ryan Wong

http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf

200GbE clock, all transitions, 0, 5, 6, 7



Possible Solution Direction

- Can we take advantage of the fact most ports will start with 50G lanes even at the MAC/PCS?
- But still support 16x25G lanes for instance for test equipment etc.?
- A 50G lane will have a natural muxing set, 0+1 and 2+3 and 4+5 etc.

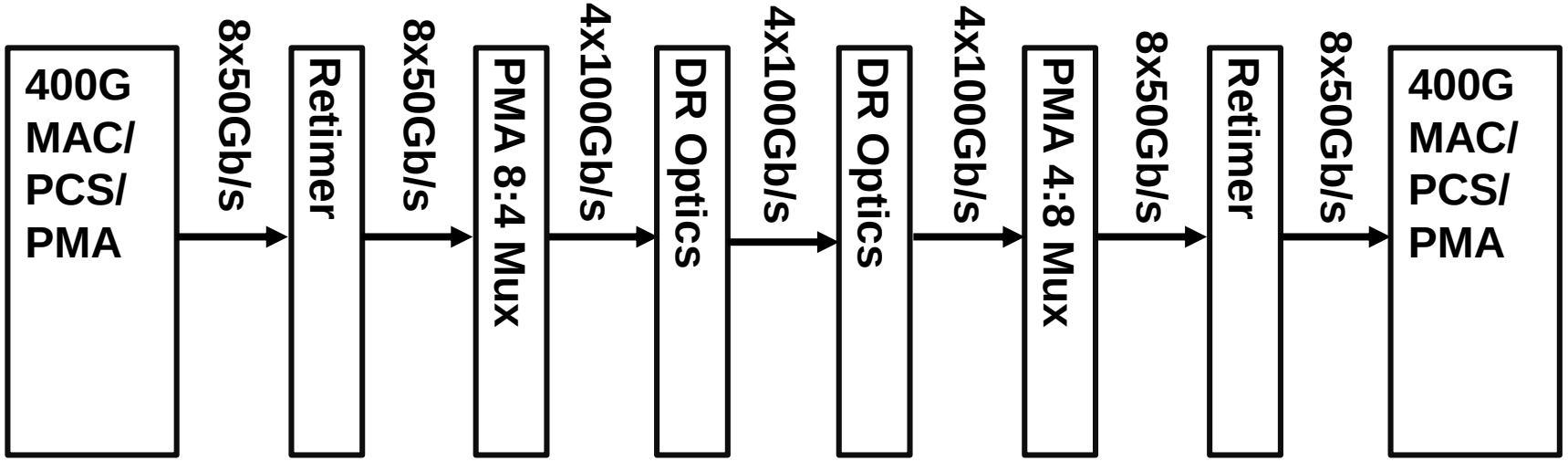
Analysis of Rogue Cases

- Pete Anslow created a spreadsheet with the rogue cases he has found
  - http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_02_121916_elect.xlsx
- In this spreadsheet there are many examples of naturally muxed lane pairs (0+1 etc), but there are no cases with two naturally muxed pairs (0+1 and 2+3).
- Highlight below….

		Natural Pair		Non-natural Pair										
2558	lanes	12	13	0	6	delays	0	5	-4	-3	average clock	0.217149	0.499628	0.716676
2559	lanes	12	13	0	6	delays	0	5	-3	-2	average clock	0.216747	0.499228	0.716115
2560	lanes	12	13	1	7	delays	0	-5	-9	-8	average clock	0.215482	0.500016	0.715619
2561	lanes	12	13	1	7	delays	0	-5	-8	-7	average clock	0.216532	0.500801	0.715629
2562	lanes	12	13	6	0	delays	0	5	-3	-4	average clock	0.216743	0.498685	0.715953
2563	lanes	12	13	7	1	delays	0	-5	-8	-9	average clock	0.215472	0.501171	0.715488

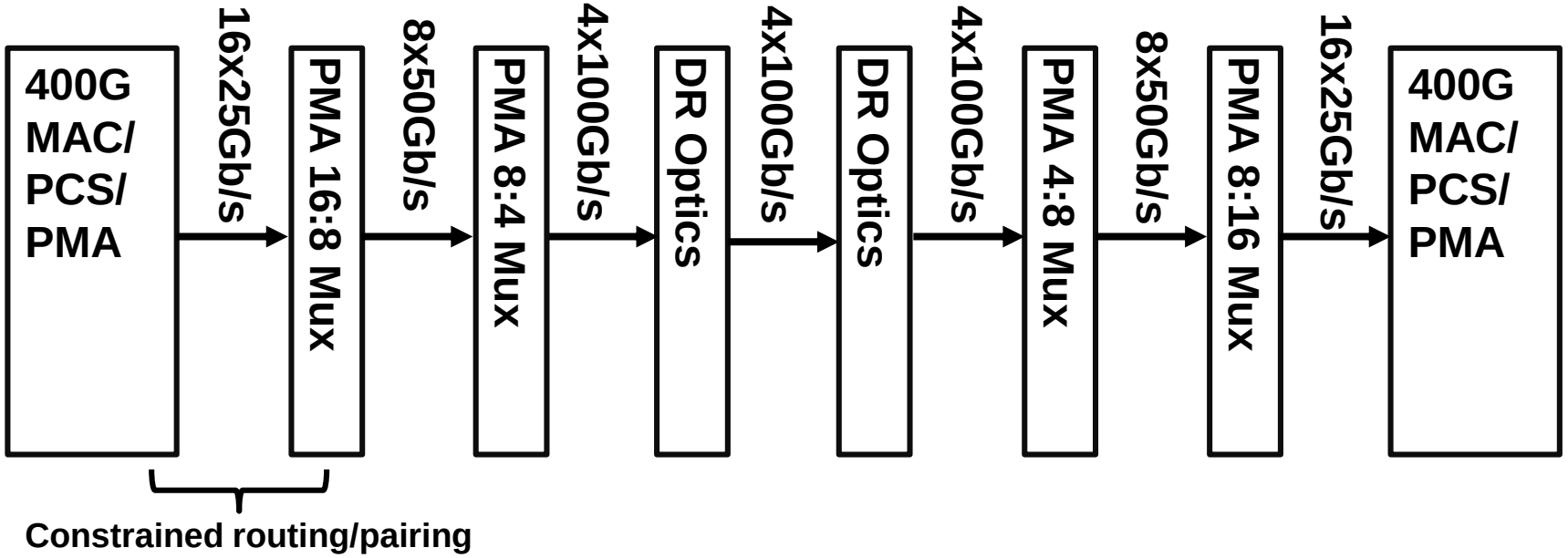
50Gb/s or faster Lanes only

- State that the TX PMA (16:8) must bit mux PCS Lane 0+1, 2+3, 4+5 etc (natural pairings)
- If there is a retimer in the path, it must keep the same paired PCS lanes together
  - This is natural anyhow
- TX PMA (8:4) mux (50G to100G) must keep natural pairs of PCS lanes together
- RX PMA (4:8) from 100G to 50G will be blind and won't necessarily keep the desired PCS lane pairings, but at that point it won't matter, we don't have 2:1 muxing concerns



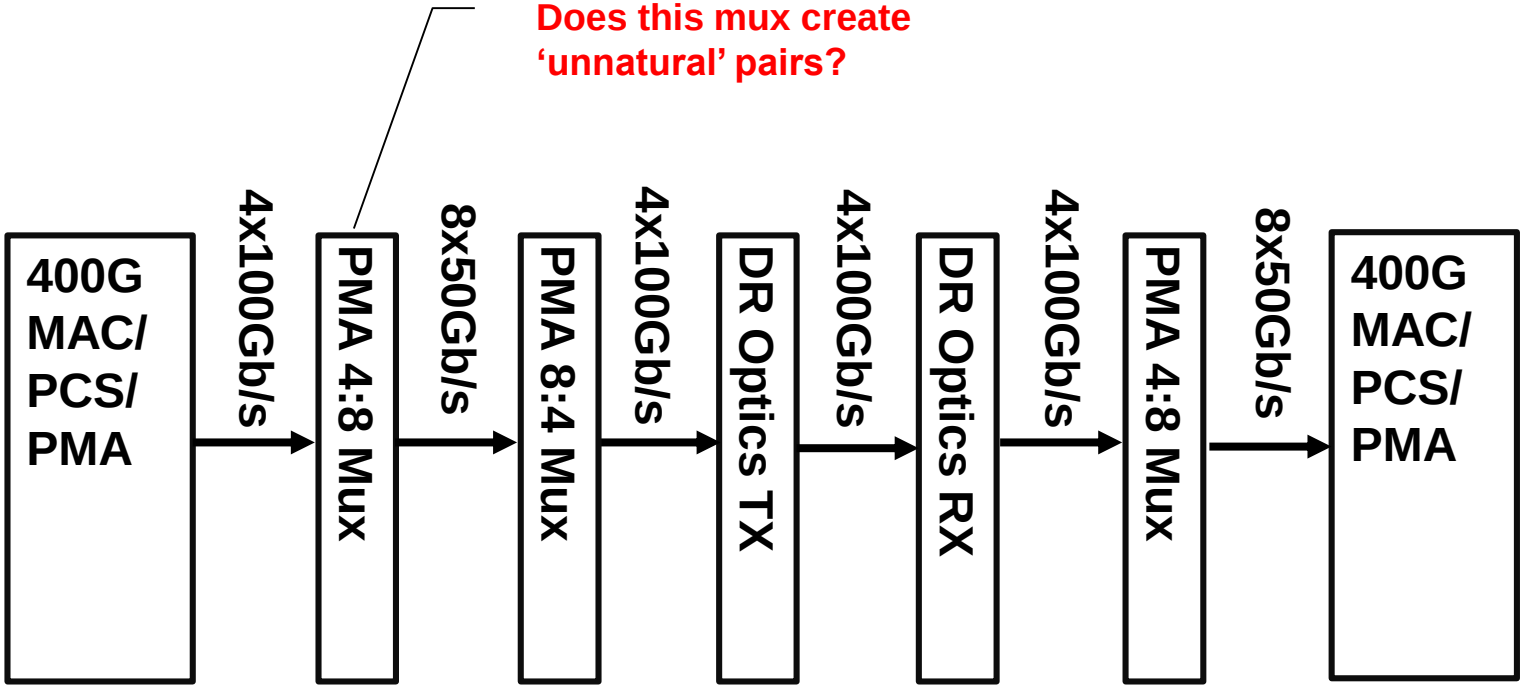
Systems with 25Gb/s Lanes

- The TX MAC/PCS/PMA (16:16) must have properly constrained lane mapping/routing to the TX PMA (16:8) device
- The TX PMA (16:8) must then bit mux PCS Lane 0+1, 2+3, 4+5 etc (natural pairings)
- See previous slide for the other constraints



Mix of 50Gb/s and 100Gb/s Lanes (future)

- What happens in the future, if 100G electrical lanes can use the same FEC/PCS?
- Is the scenario below realistic?
- The 4:8 mux would have a problem and might create ‘unnatural’ pairs?



Next Steps

- Any concerns with mux or other devices that are in the market or coming soon over these constraints?
- Any concern with implemented systems (25G or 50G based)?
- Simulations are limited in scope (small skew offset) due to the complexity of the runs, are there more cases we don’t know about?
- Are there cases between the simulation threshold and average clock content that we have not identified and will be a problem, but are not solved by the proposed pairing constraint?
- Understand is we can solve the future muxing concerns with 100G electrical lanes

Thanks!