On clock content issue over four lane interleaving

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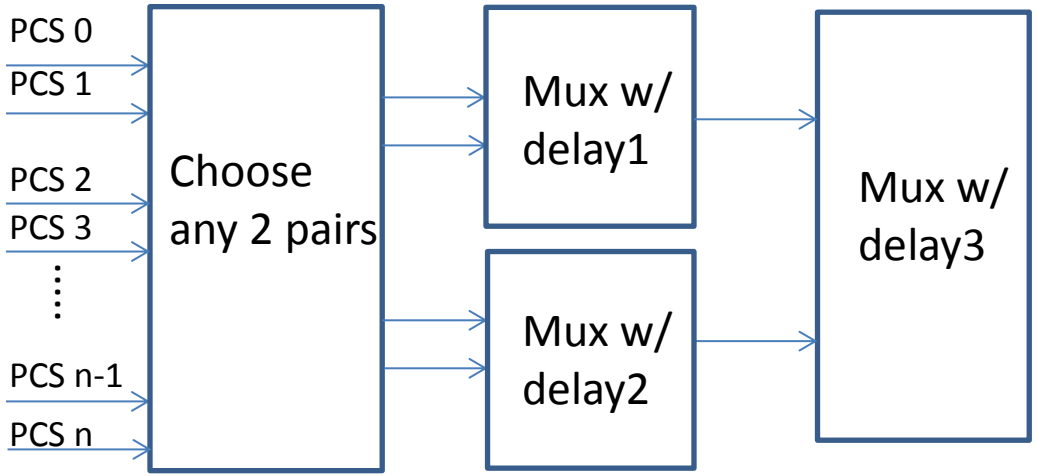
PART I : RESTRICTED BITMUXING

Restricted bitmuxing with larger delays

- Interleaving of “natural pairs” was investigated (FECL [0, 1], [2, 3]…[14, 15])
- For 400GbE, a search for all possible 4:1 restricted bit interleaving together with delays of -50 to +50 bits to form a 100 Gb/s lane shows NONE of them have the clock content curve-shift issue.
- For 200GbE, a search for all possible 4:1 restricted bit interleaving together with delays of -100 to +100 bits to form a 100 Gb/s lane shows NONE of them have the clock content curve-shift issue.



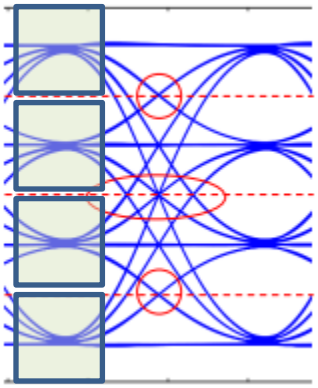
For 200G
- n=7
- -100 <= delay1,delay2,delay3 <= 100

For 400G
- n=15
- -50 <= delay1,delay2,delay3 <= 50

PART II : TURNING OFF GRAY CODING

Why turning off Gray coding doesn't help?

All transitions



Gray coding	Binary coding
(1,0) -> +3	(1,1) -> +3
(1,1) -> +1	(1,0) -> +1
(0,1) -> -1	(0,1) -> -1
(0,0) -> -3	(0,0) -> -3

GC	BC
-3 -> -3	-3 -> -3
-3 -> -1	-3 -> -1
-3 -> +1	-3 -> +3
-3 -> +3	-3 -> +1

GC	BC
-1 -> -3	-1 -> -3
-1 -> -1	-1 -> -1
-1 -> +1	-1 -> +3
-1 -> +3	-1 -> +1

GC	BC
+1 -> -3	+3 -> -3
+1 -> -1	+3 -> -1
+1 -> +1	+3 -> +3
+1 -> +3	+3 -> +1

GC	BC
+3 -> -3	+1 -> -3
+3 -> -1	+1 -> -1
+3 -> +1	+1 -> +3
+3 -> +3	+1 -> +1

- Every transition has been accounted for and no new transitions are created

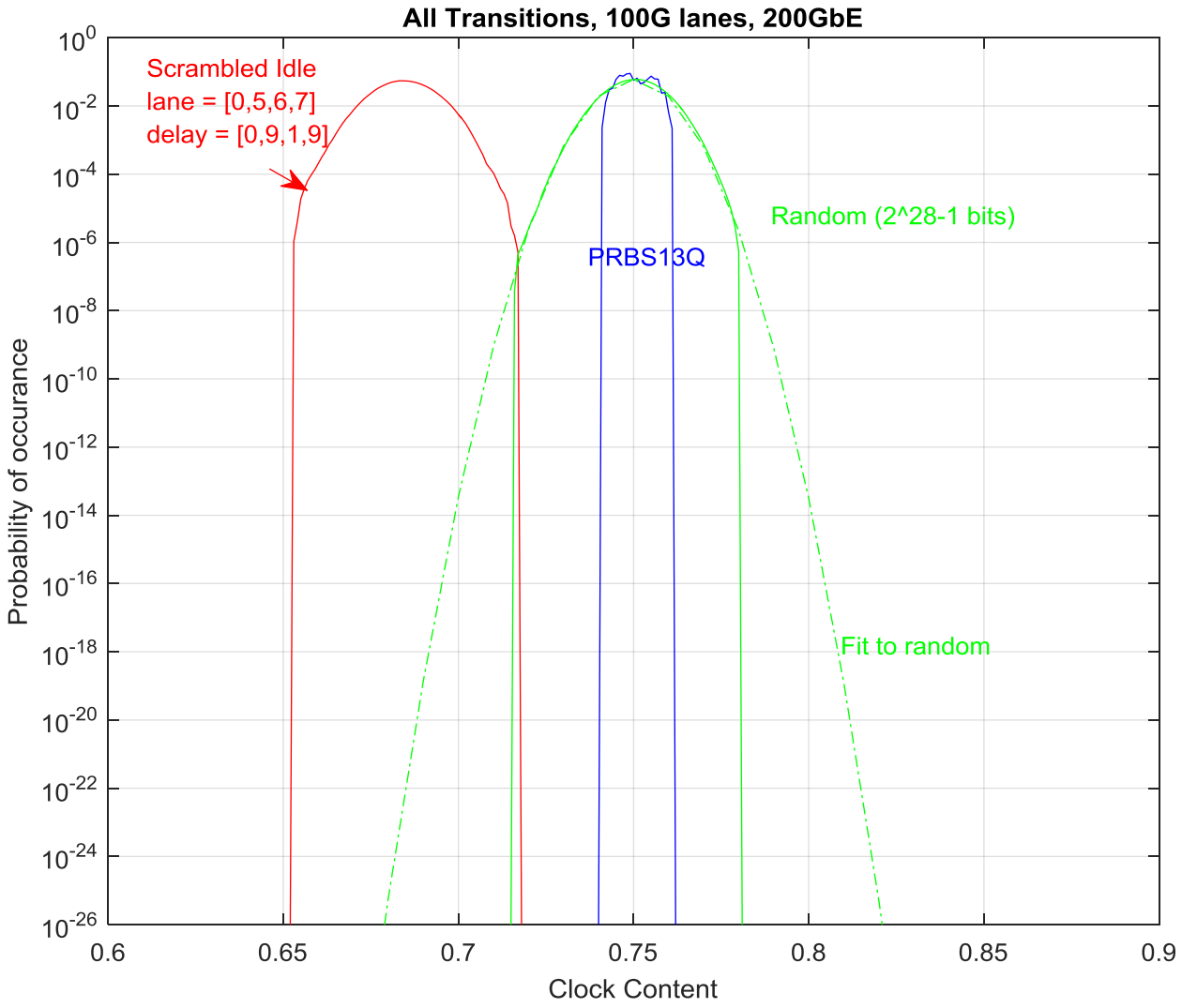
PART III: FOUR LANE INTERLEAVING WITH PRECODING

Baseline results

- With no changes to 802.3bs PCS
  - Lane = [0, 5, 6, 7]/ Delay = [0, 9, 1, 9] experiences cc curve shift
  - Lane = [0, 5, 6, 7]/ Delay = [0, 9, 1, 8] does NOT experience cc curve shift and aligns well with random data
  - Lane = [0, 5, 6, 7]/ Delay = [0, 9, 1, 10] does NOT experience cc curve shift but is slightly wider than random data

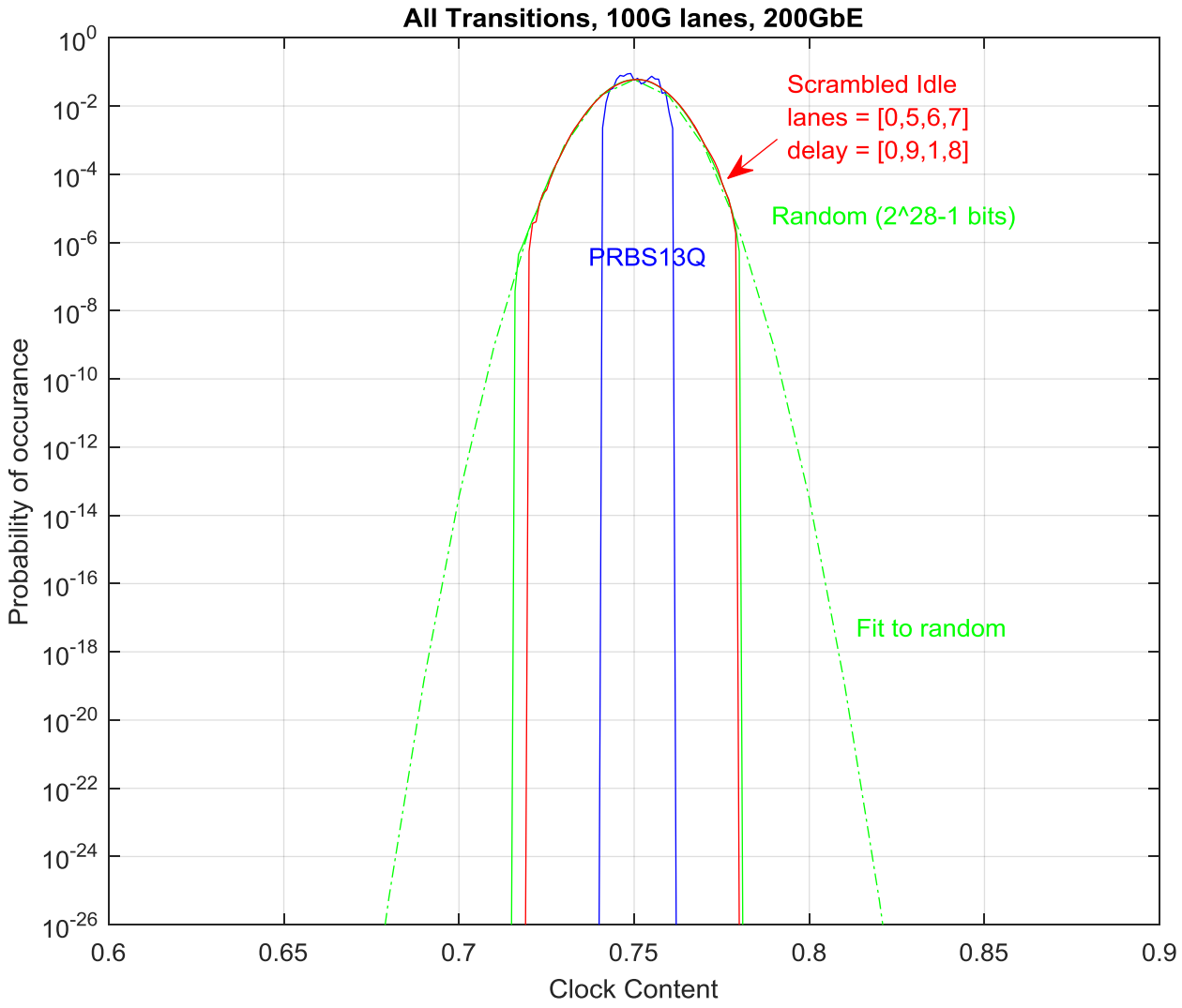
200GbE clock, all transitions (baseline behavior)

-Lane=[0, 5, 6, 7]/Delay=[0, 9, 1, 9]



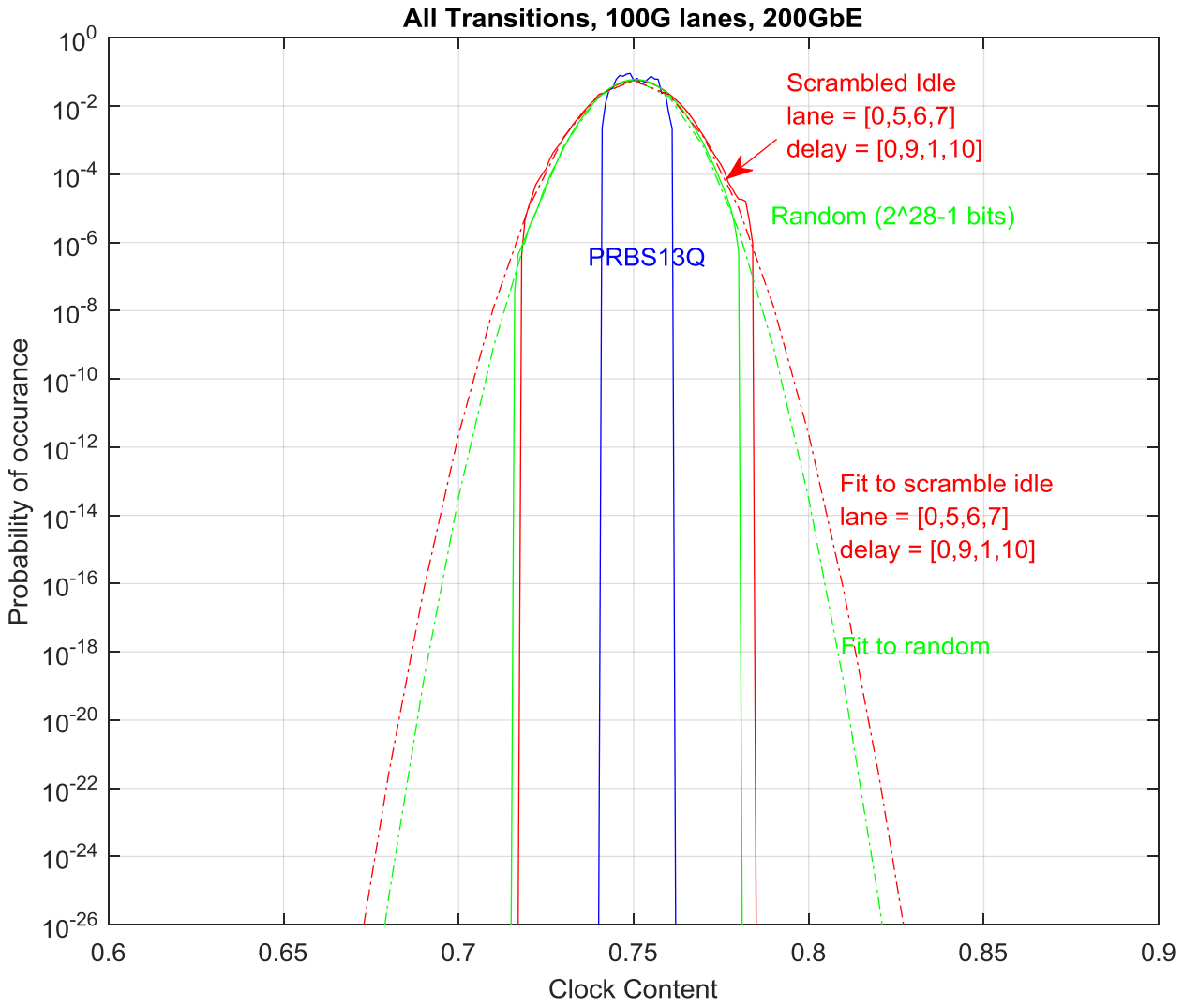
200GbE clock, all transitions (baseline behavior)

-Lane=[0, 5, 6, 7]/Delay=[0, 9, 1, 8]



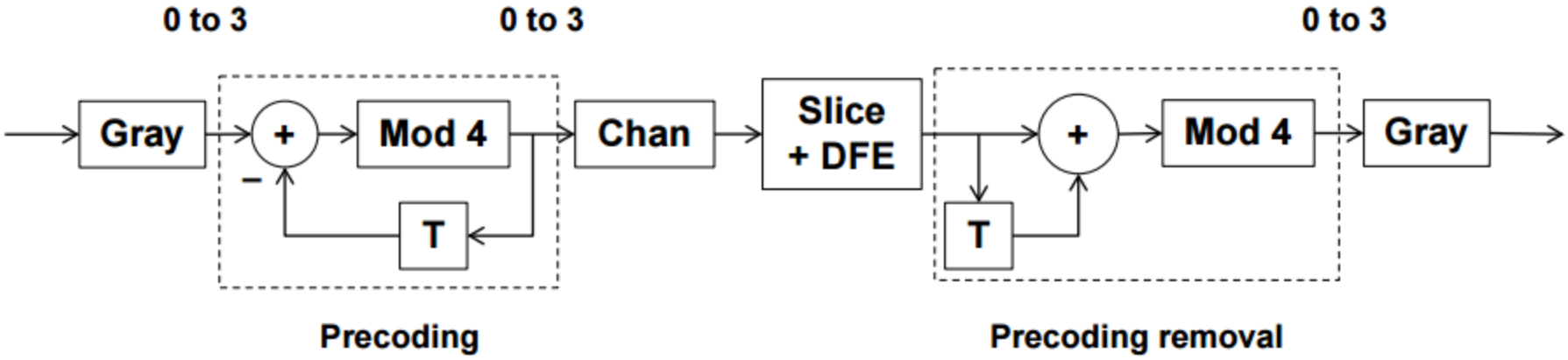
200GbE clock, all transitions (baseline behavior)

-Lane=[0, 5, 6, 7]/Delay=[0, 9, 1, 10]



A proposed fix to the cc shift through precoding

- Precoding is used to mitigate burst errors, as defined in 135.5.8 for 802.cd.



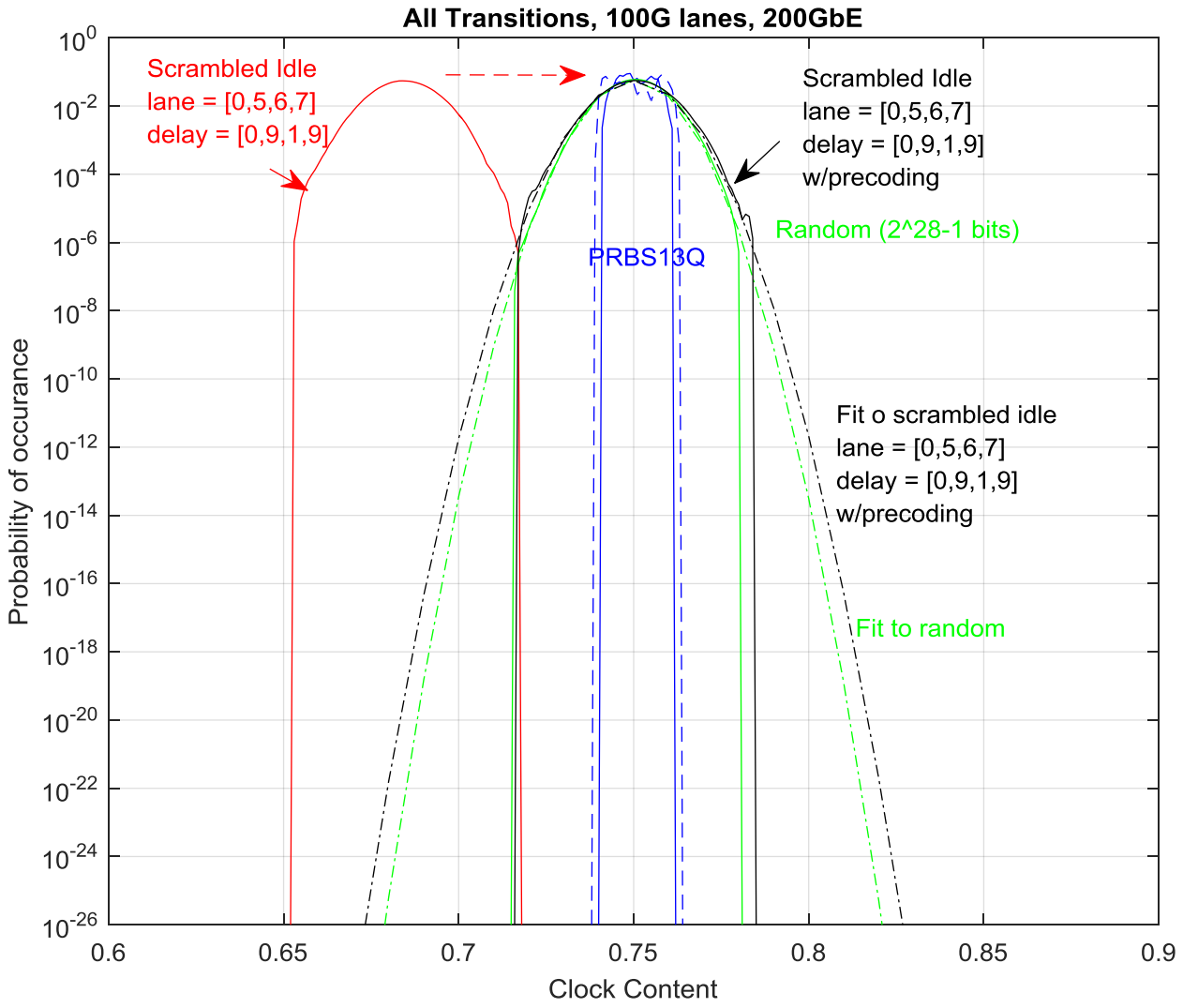
  - See p.5 of parthasarathy_01_0911 for a worked example
  - See anslow_070616_3cd_01_adhoc for FEC analysis
- Included as optional to use, mandatory to implement in 802.3cd
- Can be seen as a “scrambler” on each physical lane to remove the cc shift behavior.

Results of precoding

- With precoding,
  - Lane = [0, 5, 6, 7]/ Delay = [0, 9, 1, 9] is shifted back but slightly wider than random data
  - Lane = [0, 5, 6, 7]/ Delay = [0, 9, 1, 8] is unchanged and still aligns well with random data
  - Lane = [0, 5, 6, 7]/ Delay = [0, 9, 1, 10] is slightly widened than without precoding

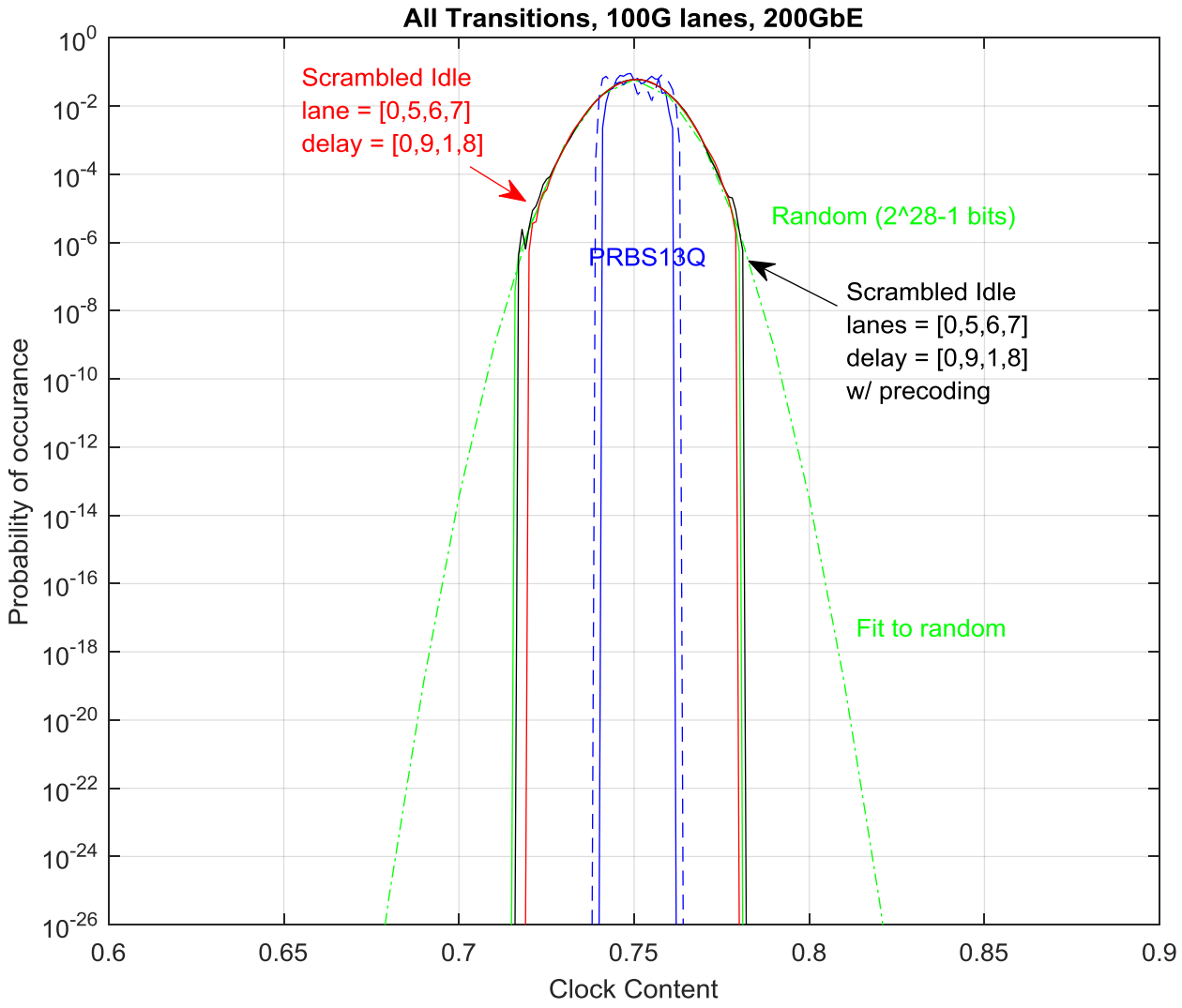
200GbE clock, all transitions

-Lane=[0, 5, 6, 7]/Delay=[0, 9, 1, 9]



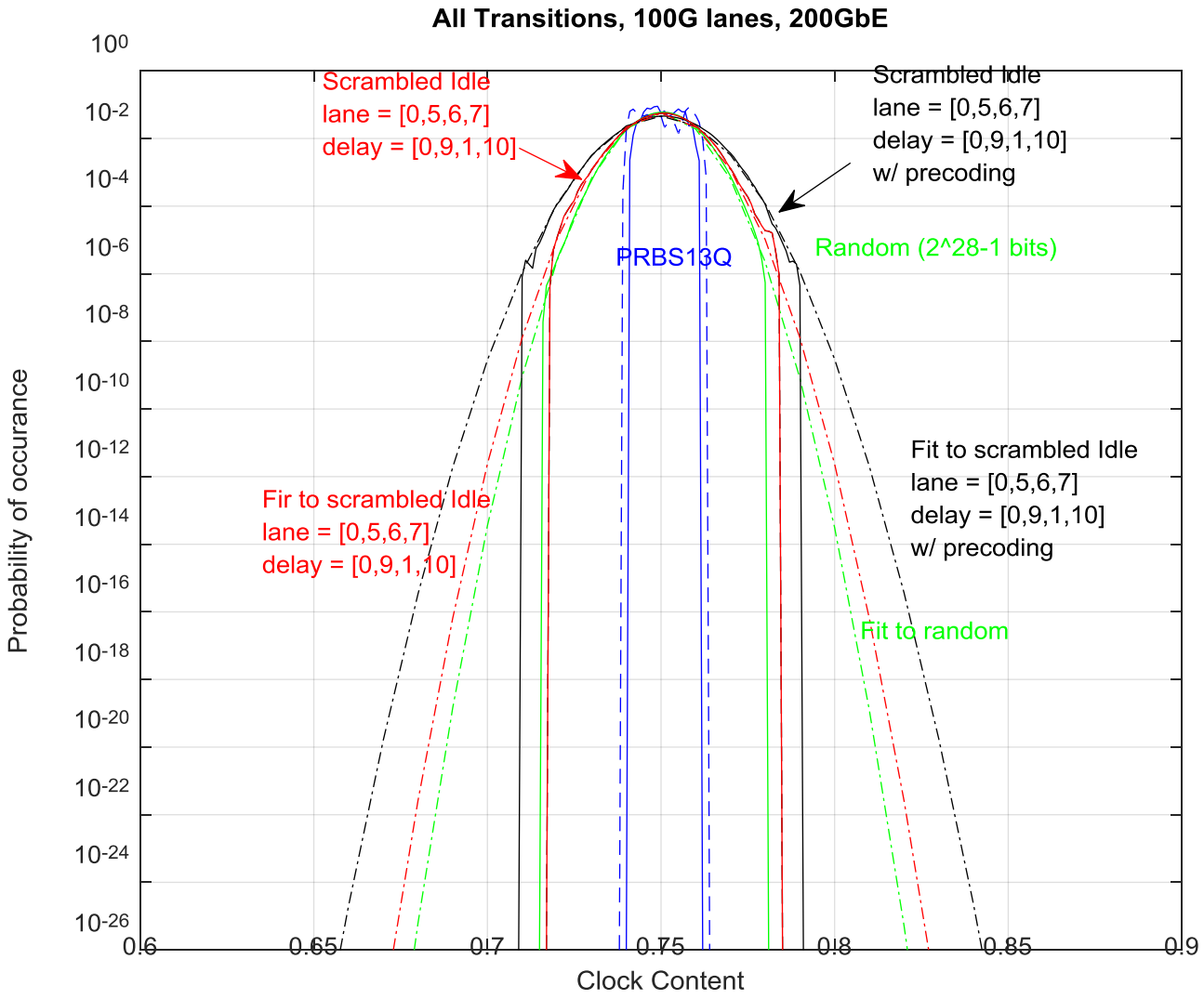
200GbE clock, all transitions

-Lane=[0, 5, 6, 7]/Delay=[0, 9, 1, 8]



200GbE clock, all transitions

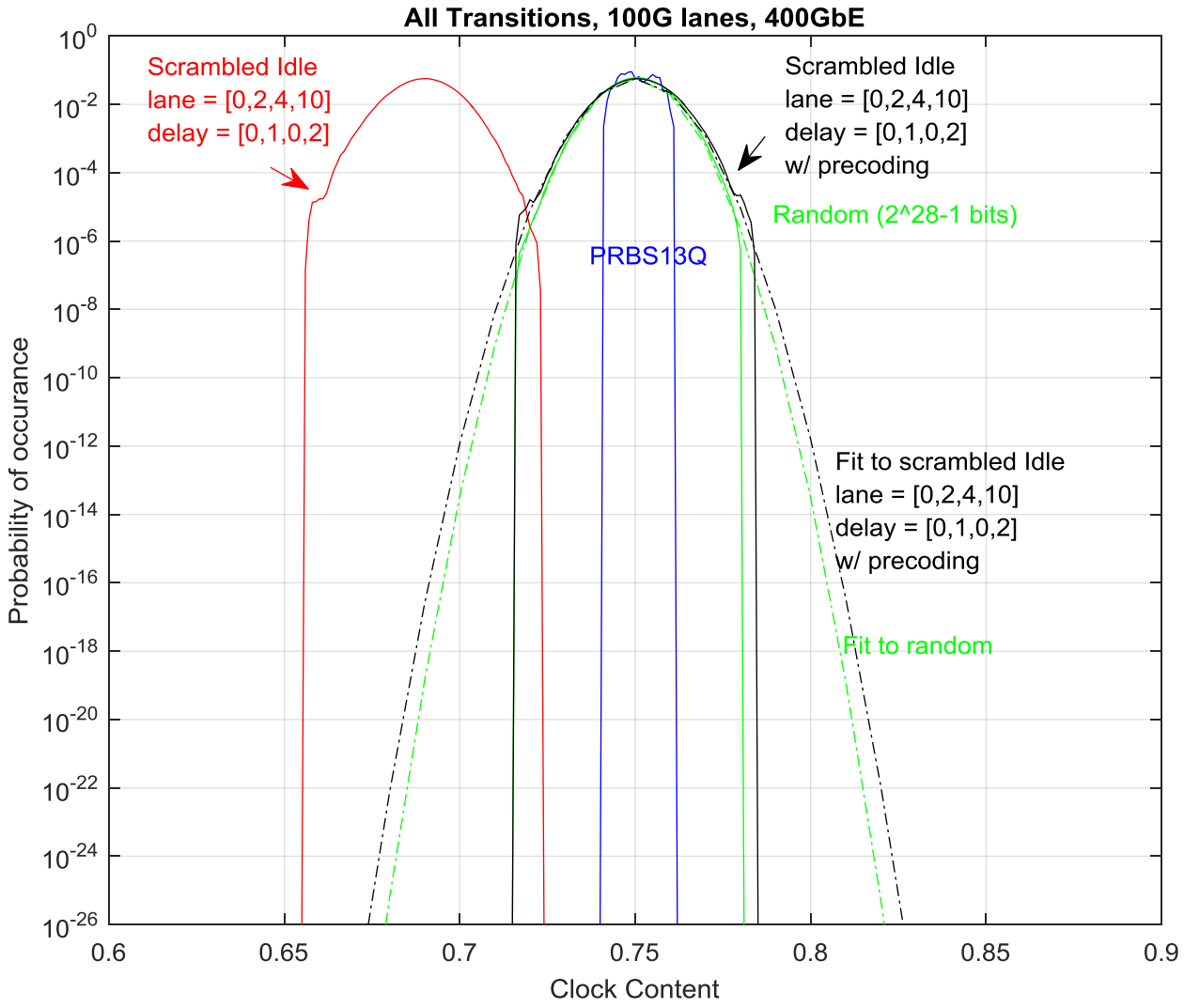
-Lane=[0, 5, 6, 7]/Delay=[0, 9, 1, 10]



400GBE RESULTS

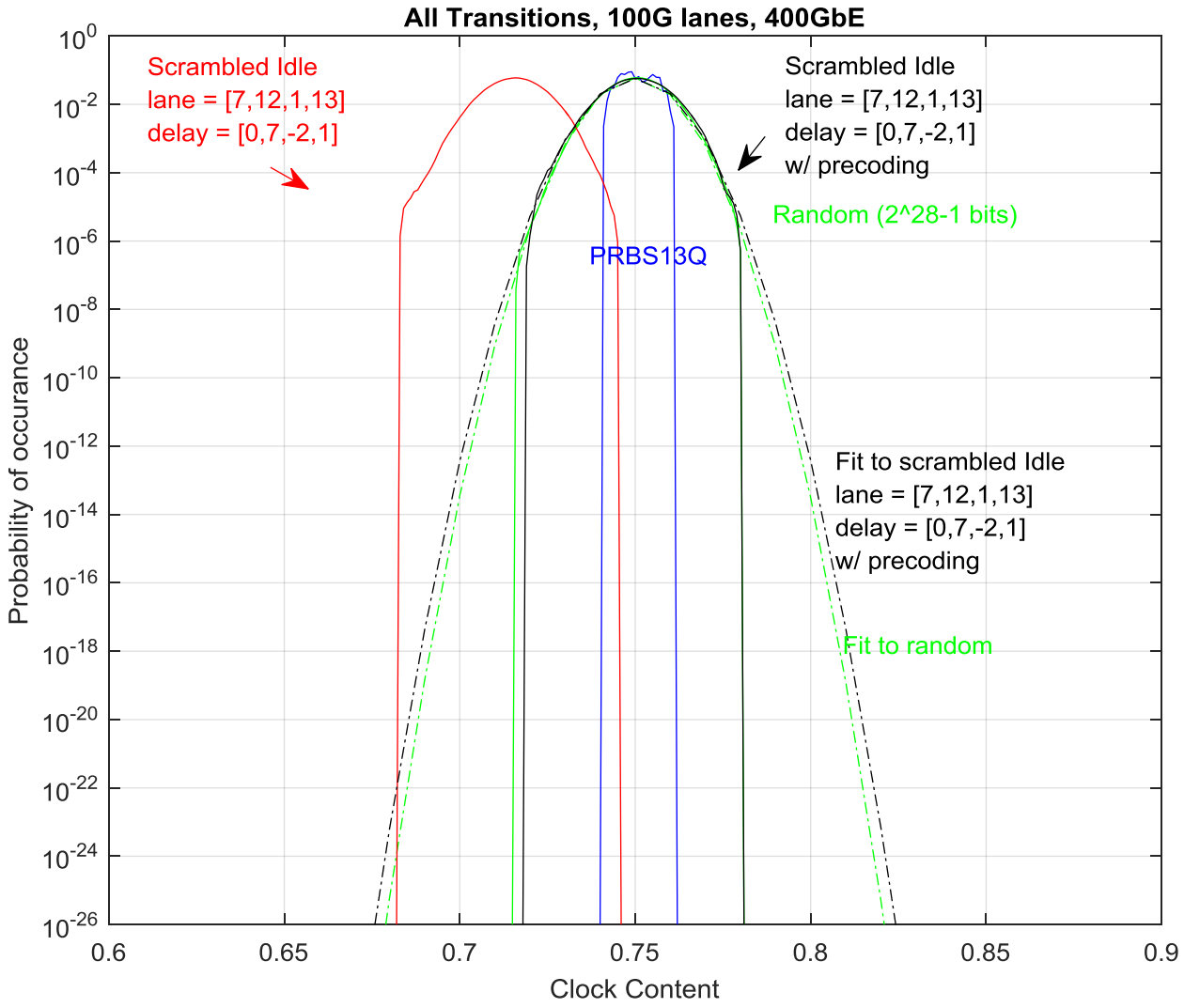
400GbE clock, all transitions

-Lane=[0, 2, 4, 10]/Delay=[0, 1, 0, 2]



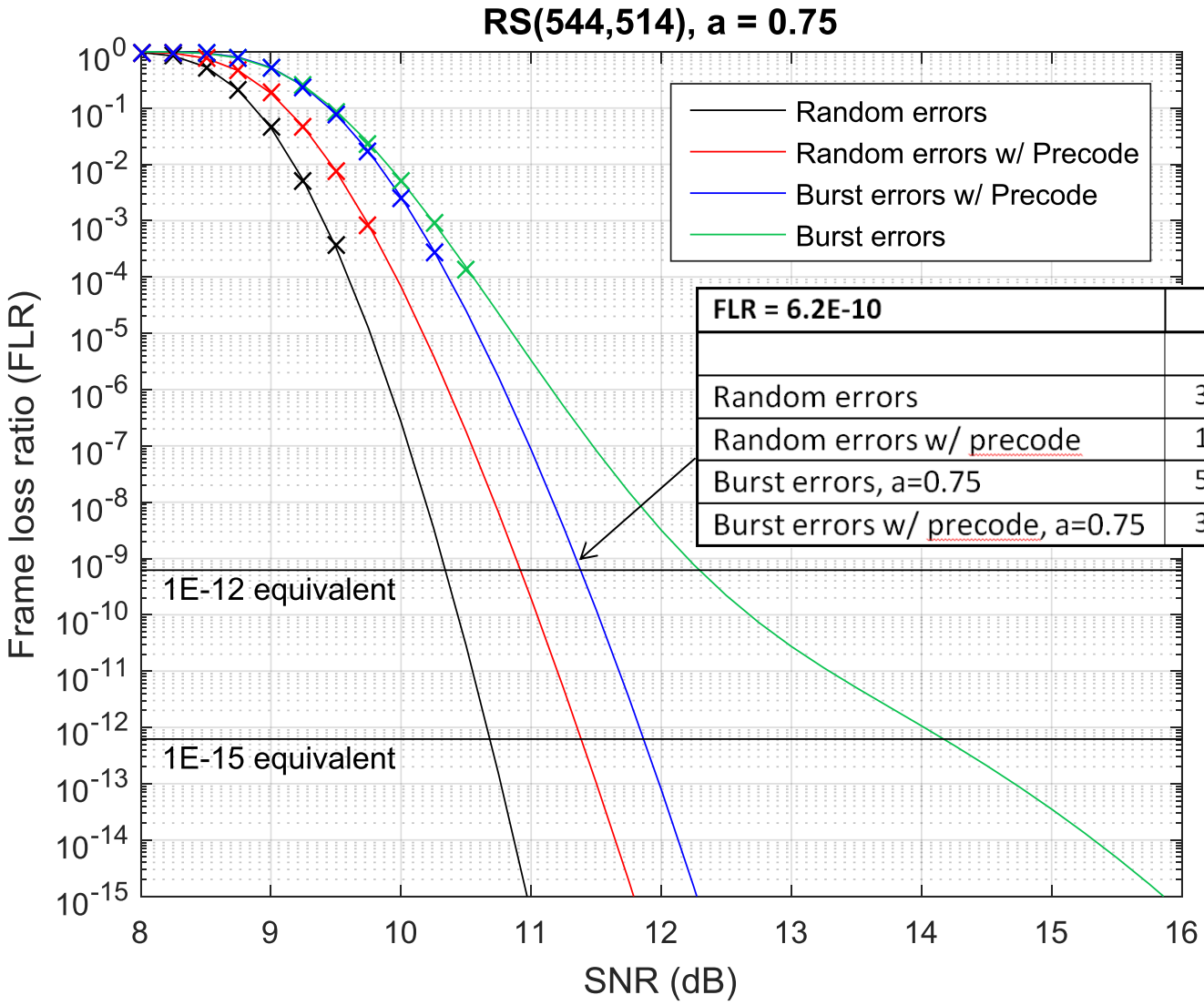
400GbE clock, all transitions

-Lane=[7, 12, 1, 13]/Delay=[0, 7, -2, 1]



Effect of error multiplication of precoding

-~0.5dB degradation in terms of SNR (single part link)



FLR = 6.2E-10	RS(544,514)	
	BER	SNR (dB)
Random errors	3.7677e-04	10.3438
Random errors w/ precode	1.6504e-04	10.9219
Burst errors, a=0.75	5.7878e-05	12.2968
Burst errors w/ precode, a=0.75	3.1334e-04	11.3828

Precoding Summary

- A search of all possible combinations of 200GbE PCS lanes for 4:1 bit interleaving together with delays of -40 to +40 bits to form a 100 Gb/s lane shows NONE of them have the curve-shift issue with the inclusion of precoding.
- A search of all possible combinations of 400GbE PCS lanes for 4:1 bit interleaving together with delays of -10 to +10 bits to form a 100 Gb/s lane shows NONE of them has the curve-shift issue with the inclusion of precoding.
- With precoding, the distribution may be slightly widened for some combinations, see the previous slides for such an example.
- With precoding, error multiplication brings a performance degradation of ~0.5dB in terms of SNR (electrical domain).

THANK YOU