Unapproved minutes

IEEE P802.3bs 400 Gb/s Ethernet Task Force Logic Ad Hoc

Teleconference July 1st, 2014

Minutes taken by Mark Gustlin, Xilinx
The meeting started at 8:01 am Pacific chaired by Mark Gustlin, the attendee list was taken from the WebEx attendee list.

Documentation for the call can be found at the Ad Hoc web page:
http://www.ieee802.org/3/bs/public/adhoc/logic/index.shtml

Mark showed the patent slides and asked if anyone wanted to disclose a patent, no one responded.

Presentation #1
Title: FOM Bit Mux, Architecture, Challenge and Solution - Xinyuan Wang

By: Xinyuan Wang, Tongtong Wang, Wenbin Yang - Huawei

See: wangx_01_0714_logic.pdf

It was asked if FOM assumes all PMDs will use the RSFEC? Was stated that FOM assumes that RSFEC is used, but if another FEC is used for a given PMD then that would need to be looked at.

It was asked if the 4x100GbE breakout shown would be compatible with SR4? Yes.

It was asked if the proposal would preclude breakout of individual 25G lanes. It has not yet been a consideration. It was also noted that while a CFI is being prepared, a 25G MAC is not defined. In addition it was noted that there is no objective to support breakout for P802.3bs.

Presentation #2
OTN Support Update – Steve Trowbridge

By: Steve Trowbridge - ALU

See: trowbridge_01_0714_logic.pdf

It was pointed out that CRC is one form of end to end notification.

There was a discussion on the pros and cons of end to end vs. segment by segment error indications. Was pointed out that sync header errors can provide this, but not if transcoding occurs.

Presentation #3
Title: FEC considerations for 400GbE

By: Zhongfeng Wang - Broadcom

See: wangz_01_0714_logic.pdf
Some discussion and agreement that if the RSFEC gain is enough, then that is what we should use.

Was asked about the definition of complexity, it is gate complexity comparison.

It was clarified that the gain stated is for random errors, not enough information yet on the channels to do anything else.

There was a lot of discussion around the tradeoffs that can be made between latency, gain and overclocking.

Attendees (taken from webex, please let me know if you have a correction):
Adam Healey, Avago Technologies
Ahmet Balcioglu, Hittite
Alan Tipper, Semtech
Alex Umnov, Fujitsu
Ali Ghiasi, Independent
Andre Szczepanek, Inphi
Brian Teipen, Adva
Charlie Chen, Titan Photonics
Daniel Koehler, MorethanIP
Dave Lewis, JDSU
David Estes, Spirent
David Law, HP
Derek Cassidy, BT
Don Oconnor, Fujitsu
Eugen Dai, Cox
Frank Chang, Inphi
Ghani Abbas, Ericsson
Guylain Barlow, JDSU
Jeff H?, Ranovus
Jeff Slavick, Avago Technologies
John D'Ambrosia, Dell
John Ewen, IBM
Juan-Carlos Calderon, Cortina
Keisuke Kojima, Mitsubishi Electric
Kenneth Jackson, Sumitomo
Ky Piper, Cisco
Mark Gustlin, Xilinx
Martin Bouda, Fujitsu
Martin Langhammer, Altera
Megha Shanbhag, TE

Michael Ressl, Hitachi Cable
Mike Dudek, Qlogic
Mike Li, Altera
Oded Wertheim, Mellanox
Paul Kolesar, Commscope
Paul Mooney, Spirent
Pete Anslow, Ciena
Peter Stassar, Huawei
Pi Boson, ?
Piers Dawe, Mellanox
Pirooz Tooyserkani, Cisco
Ramm Rao, Oclaro
Raymond Nering, Cisco
Rich Mellitz, Intel
Rick Rabinovich, Alcatel-Lucent
Robert Coenen, Intel
Salvatore Rotolo, ST Microelectronics
Sam Sambasivan, AT&T
Steve Gorshe, PMC-Sierra
Steve Trowbridge, Alcatel-Lucent
Susan Bueti, IBM
Thananya Baldwin, Ixia
Tom Issenhuth, Microsoft
Tom McDermott, Fujitsu
Tom Palkert, Xilinx, Luxtera, Molex
Tongtong Wang, Huawei
Ullas Kumar, Rakon
Wheling Cheng, Ericsson
Xihua Fu, ZTE
Xinyuan Wang, Huawei
Zhongfeng Wang, Broadcom
Vasu Parthasarathy, Broadcom