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FEC Considerations for 400Gbps Ethernet

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- **FEC possible latency target**
- **Overclocking ratio vs. FEC coding gain**
- **FEC complexity, power, and coding gain tradeoffs.**
- **Summary**

- FEC for 100G-KR4 is well defined. Overclocking ratio (OCR) is 0%.
- For 400GbE, latency, power/complexity, and (target) coding gain can be quite different from simple scaling.
- The presentation has no intention to define FEC scheme (e.g., single vs. multiple mode, 6dB or 8dB gain) unless and until 400Gbps channel is defined and link budget shortfall is understood
- This presentation aims at clarifying some technical issues related to high-gain FEC in 400Gbps.

- In 802.3bj, we target FEC-related latency to be less than **100ns**, where the receive time for a FEC frame takes about **50ns** and the rest time budget is mainly used for decoding.
 - ✓ This goal has been proved to be reasonable and achievable.
- For 400GbE, if using same or similar FEC code, we can achieve lower latency. In case a higher coding gain FEC is desired (e.g., at PMD level), we can trade off FEC latency for coding gain.
- Thus it may be a good option to keep similar latency target (**~ 100ns**) while pushing for higher coding gain of FEC.

- Assume PAM4 modulation is adopted.
- According to previous presentations in 400GE meetings, the target coding gain (CG) of FEC can be over **8dB**.
- Soft-decision FEC are not suited for 400GE applications due to excessive power consumption. With conventional block codes under the limited latency, we need higher overclocking ratio to achieve the target.
- Assume a transcoding scheme similar to what we used in 802.3bj is included. The overclocking ratio is better to be less than **10% (or even lower)** to minimize the increase of line rate while ensuring enough coding gain with limited latency.

■ BCH Codes (Based on 256/257b transcoding)

➤ Ex-1: BCH(2880, 2570, t=25), OC~= 9.09%, CG ~ 8.8dB (PLL=72/66)

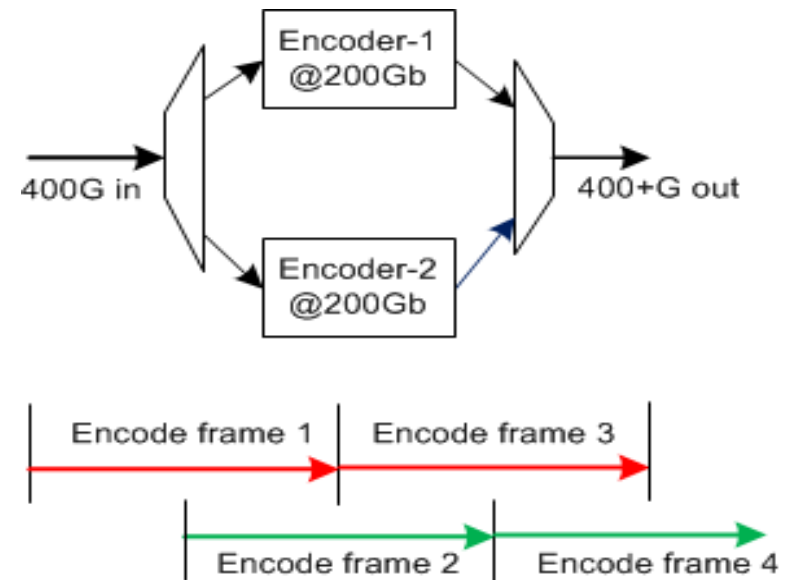
- Power ~> 35X (100G-KR4 FEC)
- HW complexity: ~> 30X (100G-KR4 FEC)
- Latency: 45~ 50cyc or 72~80 ns (assume 1.6ns/cyc)
- **Note:** parallel encoders may be needed to achieve 400Gbps.

➤ Ex-2: BCH(4416, 4112, t=23), OC~= 4.55%, CG ~ 8.3dB (PLL=69/66)

- Power ~> 35X (bj FEC)
- HW complexity: ~> 30X (bj FEC)
- Latency: 50~55cyc or 80 ~ 88ns
- **Note:** parallel encoders may be needed.

It causes extra delay.

- **Note:** latency is related to HW complexity. If we increase parallelism level, the decoding latency will be reduced while HW complexity will be increased.



- **RS Codes** (Based on 256/257b transcoding)

- Ex-1: RS(576, 514, t=31, m=10), OC_~= 9.09%, CG ~ 8.6dB

- Power ~ 24X (100G-KR4 FEC)
- HW complexity: > 16X (100G-KR4 FEC)
- Latency: ~ 90cyc or 144 ns (assume 1.6ns/cyc)
- **Note:** parallel encoders may be needed. Multiple code interleaving is another option.

■ Single block Code

- Total delay \approx encoder delay + receive time + decoder delay
- The receive time is proportional to the size of FEC block when data rate is fixed.

■ M Interleaved block Codes

- Total delay \approx M x (encoder delay + receive time) + decoder delay

- For 400G applications, the receive time is not very large for the previously considered code sizes (**6 ~ 13 ns**). Thus it may be worthwhile to consider **2 or more interleaved block codes** to ease implementation. Another option is **to independently encode data across 200G (or 100G) data stream** instead of 400G data stream.

- Under the constraints of about 100ns latency and less than 10% (or even 5%) overclocking ratio, the FEC codes with about 8.5dB coding gain are feasible for 400GE.
- Rather than employing parallel encoders to achieve 400G throughput, using M ($M > 1$) independent encoders for M -interleaved block codes may be an attractive option.
- The power consumption for a single BCH or RS code with CG of around 8.5dB can be very significant for 400GE.

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THANK YOU