1x400GE FEC Implementation

Martin Langhammer

Altera Corporation

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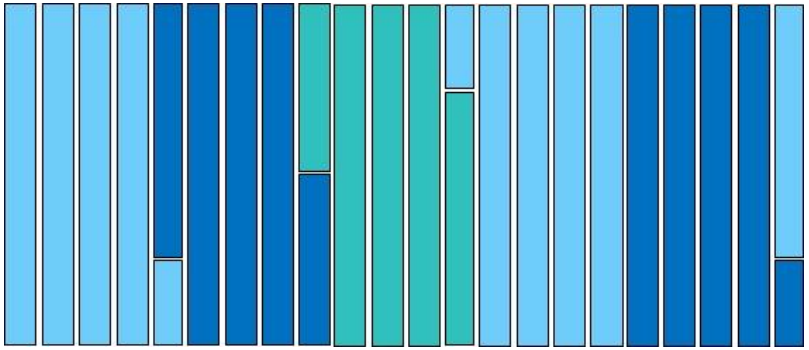
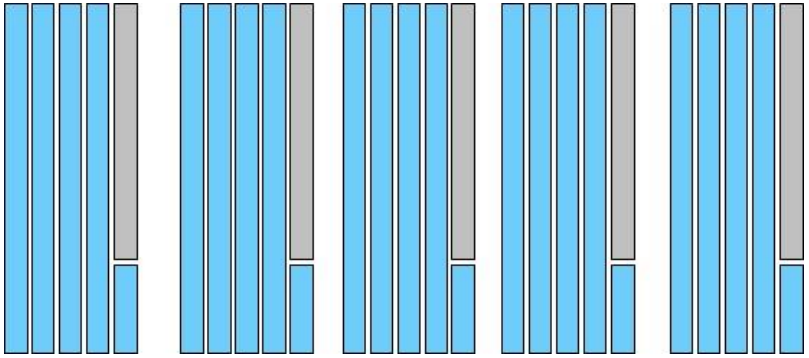
1x400GE Problem (and a fix)

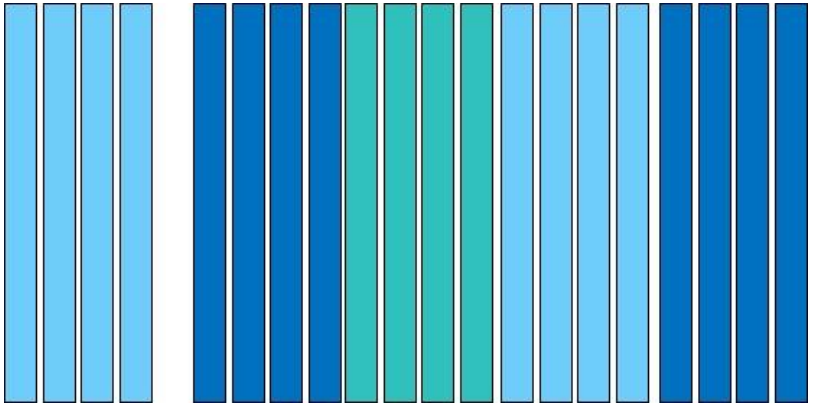
(544%128)!=0



Gearbox in Time
(run faster to have a constant input pattern)
128 width



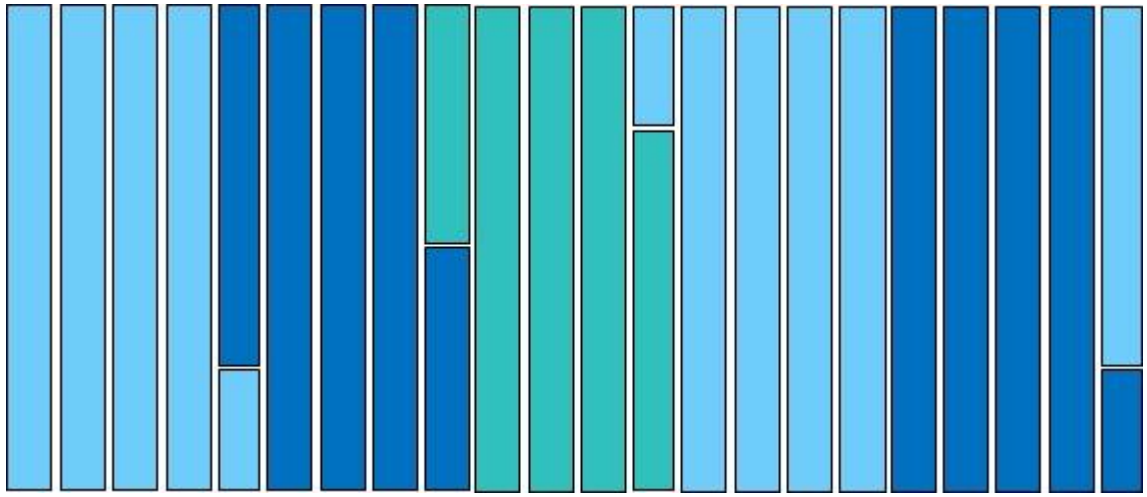
Gearbox in Width
(run faster to have a constant input pattern)
136 width



Requires Gearbox(es)
Requires Multi-clocks

Or

- Build Decoder with continuous input pattern
  - 128 symbol width
  - Direct interface to PMA and PCS
- Now working – functionally and FPGA fit



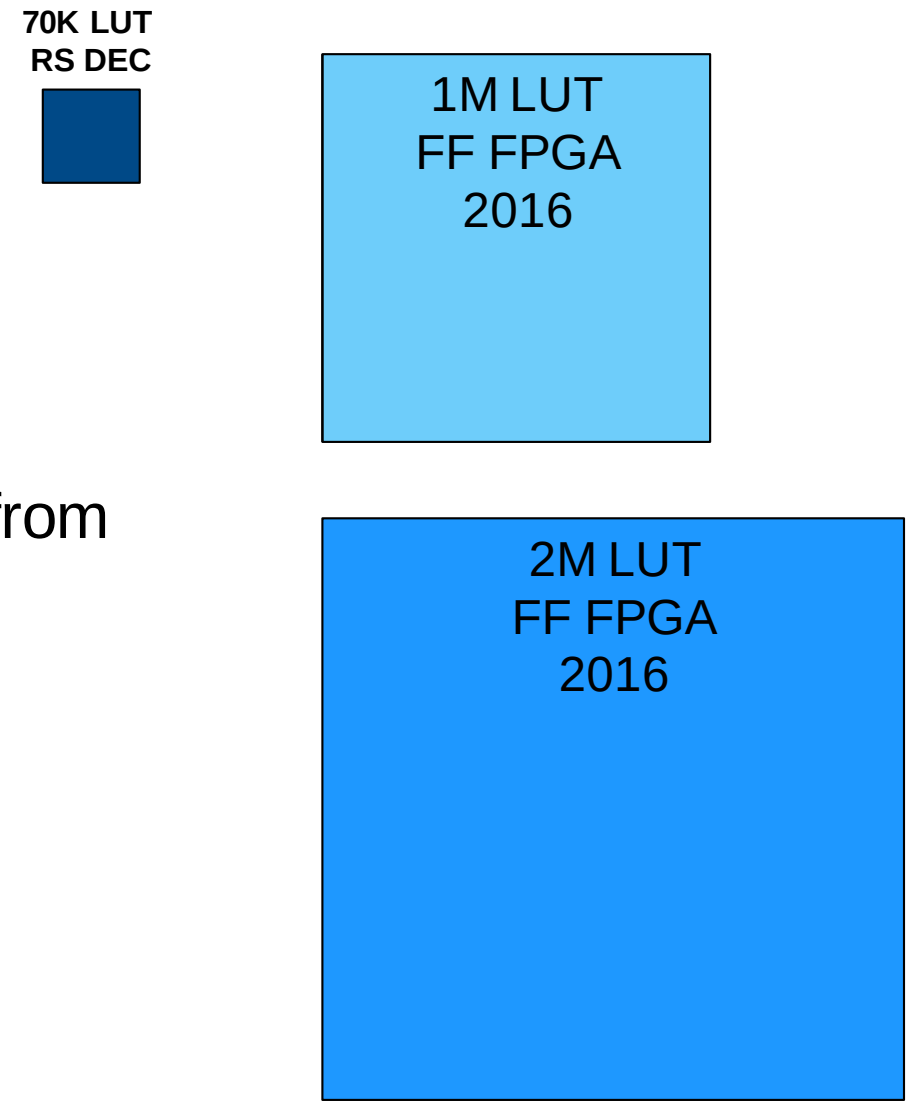
FPGA KP4 Resources (ALM ≙ 6LUT)

- 100G KP4 : 19K ALMs
  - 4x100G: 78K ALMs
  - Improved from November 2014 results
- 400G KP4 (4 x 136 symbols): 70K ALM
- 400G KP4 (128 symbol continuous): 70K ALM
- 1x400G continuous throughput same size as simple input styles
  - More complex algorithm and logic
  - Offset by slightly smaller datapath
- 1x400G slightly smaller than 4x100G

FPGA Use Considerations

- FPGA system implications
  - Area of 1x400G smaller than 4x100G
  - But 4x100G has a more decomposable routing congestion
    - Easier to fit automatically, possibly lower speed grade device
      - Time and cost consideration
  - Probably not significant reason, especially consideration likely production device technology

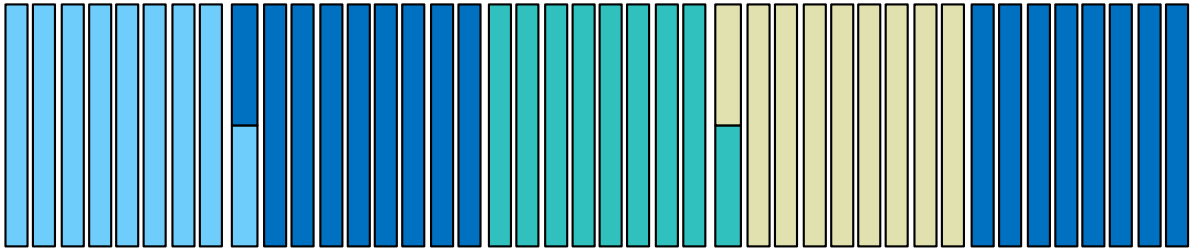
FPGA Resource Ratios



- 1x400G KP4 decoder fraction of likely target FPGAs
- Similar area roadmap from all major FPGA manufacturers

1x400GE FEC ASIC

- ASIC continuous throughput simpler pattern than FPGA continuous throughput
  - Largely because of 2x clock rate
- Simpler design
  - Simpler control structure
  - Narrower datapaths



Conclusions

- 1x400G KP4 FEC can be made integration friendly
  - Direct connect interface with a single clock domain
- 1x400G FEC options relatively constant area
- FPGA fitting may be more difficult at 1x400G
- Advantages of choosing 1x400G appear to outweigh disadvantages

Comments? Questions?

Thank You