400GE FEC Breakout

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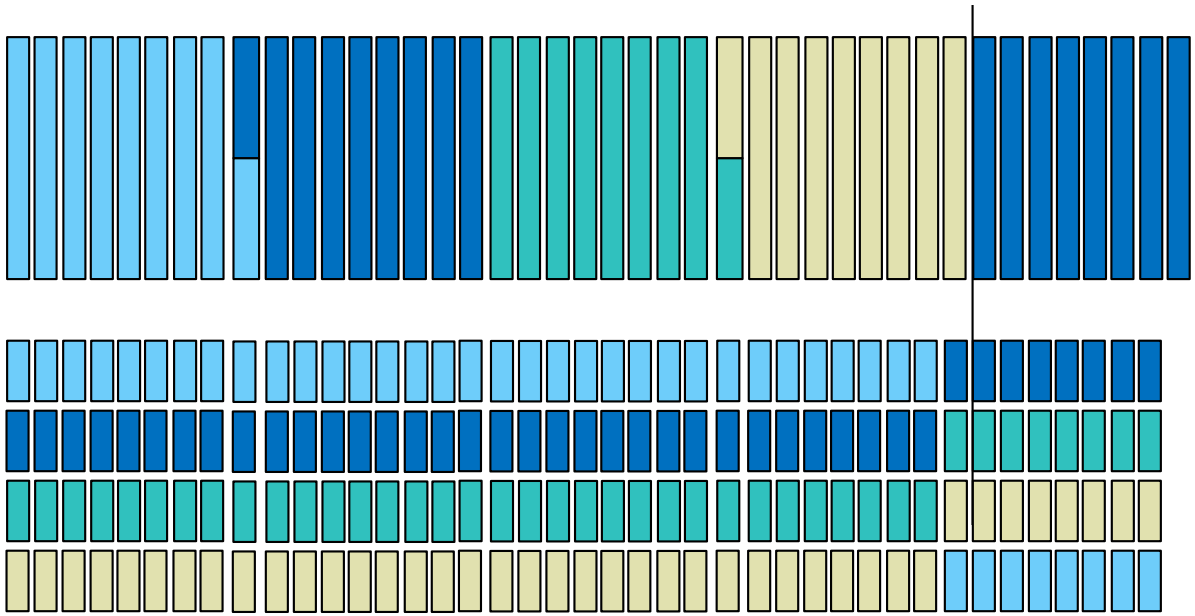
1x400GE ASIC Breakout Problem



1x400G KP4 RS(544,514) requires 8.5 clocks per codeword @ 64 symbols per clock
4x100G KR4 RS(528,514) requires 33 clocks per codeword @ 4x16 symbols per clock

1x400G FPGA Breakout Problem

- There is none
  - Just reconfigure device with required FEC
- Still important for FPGA market
  - Hard embedded FECs

Method

- Build ASIC Decoder
  - 64 symbol width
  - 1x400G, 8.5 clocks per KP4 codeword
  - ASIC pipeline depth for correct area model
- Fit into FPGA
  - Only relative sizing needed for options
  - Large reported area variance between ASIC cores anyways

Results

- 1x400G KP4 ASIC: 55645
- 1x400G KP4 & 4x100G KR4 ASIC: 61518
- 11% area increase
- Recoverable to 5% area increase
  - Some duplicated calculations due to schedule

- ***Caveats***
  - ***Treat size as dimensionless number***
    - ***Don't compare to FPGA results – very different component structures***
  - ***Preliminary Design: optimization possible, especially latency***

Latency

- Similar to reported individual core results
- Proportional to KES architecture
  - Codeword input time constant for any architecture
- 2 KES ASIC options
  - 1 clock per check symbol (KP4 = 30 clocks, KR4 = 14 clocks)
    - Simplest, lowest latency
  - 2 clocks per check symbol (KP4 = 60 clocks, KR4 = 28 clocks)
    - Easier to for timing closure, longer latency
- Latency : 2 clock KES
  - 1x400G KP4 RS(544,514) = 137ns
  - 4x100G KR4 RS(528,514) = 120ns
- Latency : 1 clock KES
  - 1x400G KP4 RS(544,514) = 90ns
  - 4x100G KR4 RS(528,514) = 74ns

Un-optimized latencies
Optimized latencies 10ns-15ns less

Architecture Notes

- Direct Breakout Supported
  - Based on 1x400G Core
  - Dynamic Switching between 1x400G and 4x100G
    - Using the same datapath elements
  - No TDM
  - No additional memory
  - No material latency change (<< 5 clocks)
- Currently Breakout Lanes are in Lockstep
  - Straightforward to make completely independant

Other considerations

- Wiring and Mux density
  - Will be increased for breakout support
  - Effect TBD
- Timing closure
  - 1x400G architecture likely more difficult than 4x100G
    - ASIC or FPGA
  - Breakout support will further increase bus length and width
- Other breakout possibilities
  - 4x100G KP4 may be possible using very little additional hardware

Conclusions

- 1x400G and 4x100G breakout directly supportable
  - Using a single core architecture
  - 5%-10% larger than 1x400G monolithic
    - Based on both achieved results and architectural analysis

Comments? Questions?

Thank You