Analysis on 400G FEC Architecture

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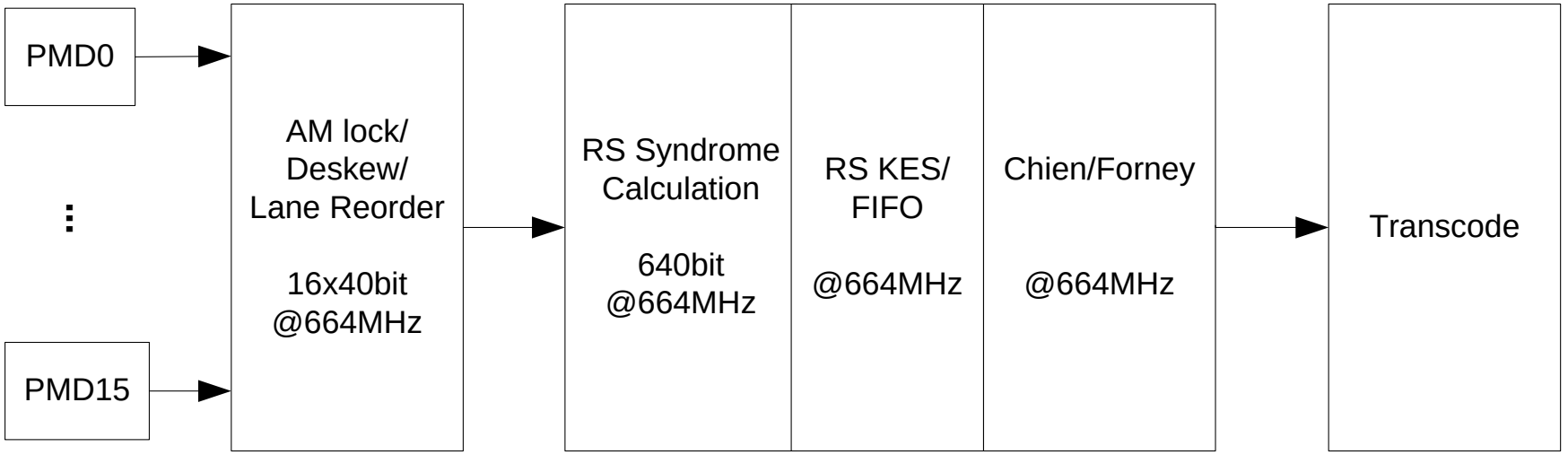
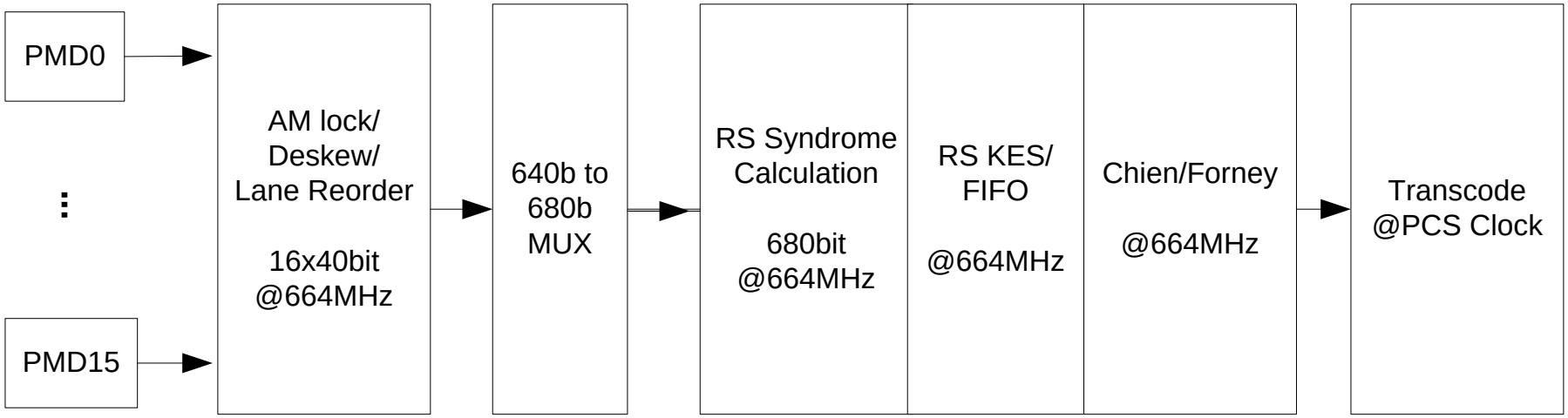
1x400G FEC: 640 bit buswidth



Block diagram for 16x25G PMD

- Easy clock scheme. Clean data path MUX for 4x100G, 8x50G, and 16x25G PMD.
- Frame latency is 8.5 cycles. Syndrome calculator: pipelined architecture with 2 engines to run at 664MHz and avoid external glue logic.
- FEC decoder latency: 8+1=9 cycles for syndrome calculation, 30 cycles for KES, 8+1 cycles for Chien/Forney.
- 320b@1328MHz will be possible?

1x400G FEC: 680 bit buswidth



Block diagram for 16x25G PMD

- RS frame can be received in 8 (5440/680) cycles, simple syndrome calculator.
- Lane alignment block has 640bit buswidth to avoid the half cycle issue (wang_z_3bs_01_0515.pdf). If this buswidth is 680b:
  - For 8x50G PMD, AM buswidth is 85bit. One extra cycle is needed to merge lanes as 85 is not a multiple of RS symbol size.
  - For 16x25G PMD, lane alignment logic needs to deal with 42.5bit per cycle and is complicated.
- Latency: 1 cycle for 640b/680b MUX, 8 cycles for syndrome calculation, 30 cycles for KES, 8+1 cycles for Chien/Forney.

1x400G FEC: Implementation Analysis

- Decoder clock frequency: 664MHz

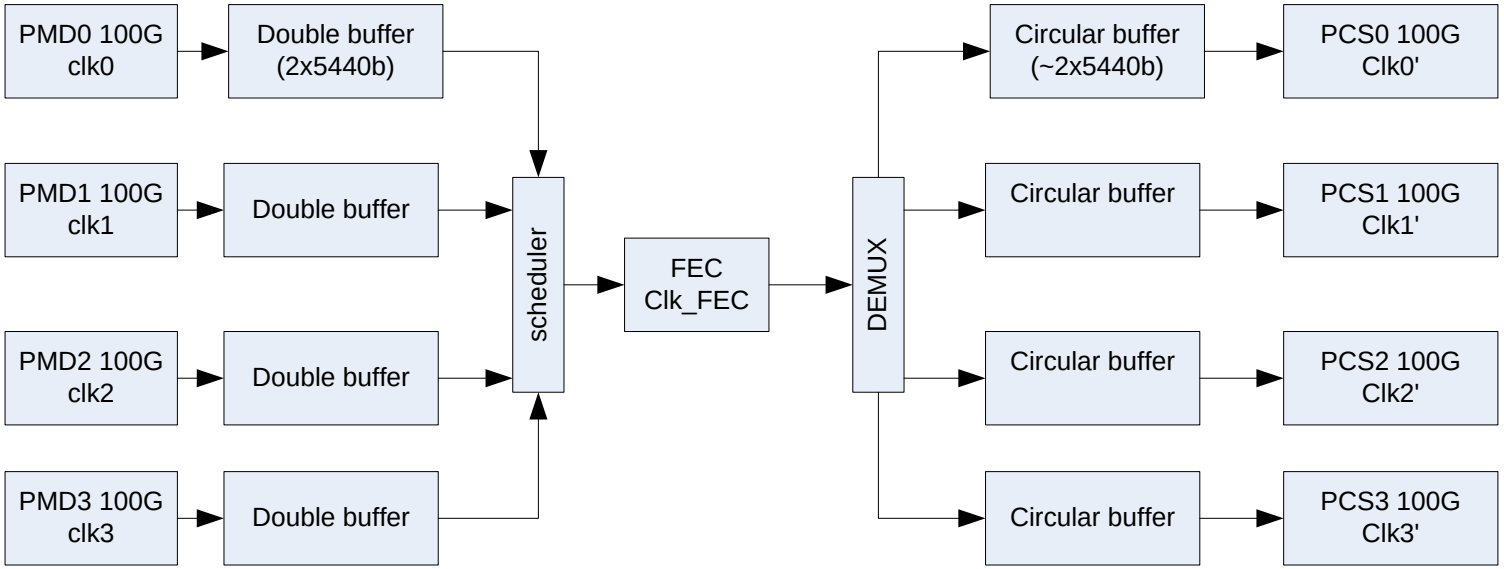
- Hardware complexity:
  - 4 RS KES engine is needed to keep 400Gb/s throughput.
  - RS Chien/Forney: 68 parallel engines
  - Encoder: ~4x Parallelism compared to a 100G FEC

- Latency:
  - Decoder: ~72 ns; Encoder: ~3ns

1x400G FEC: Breakout

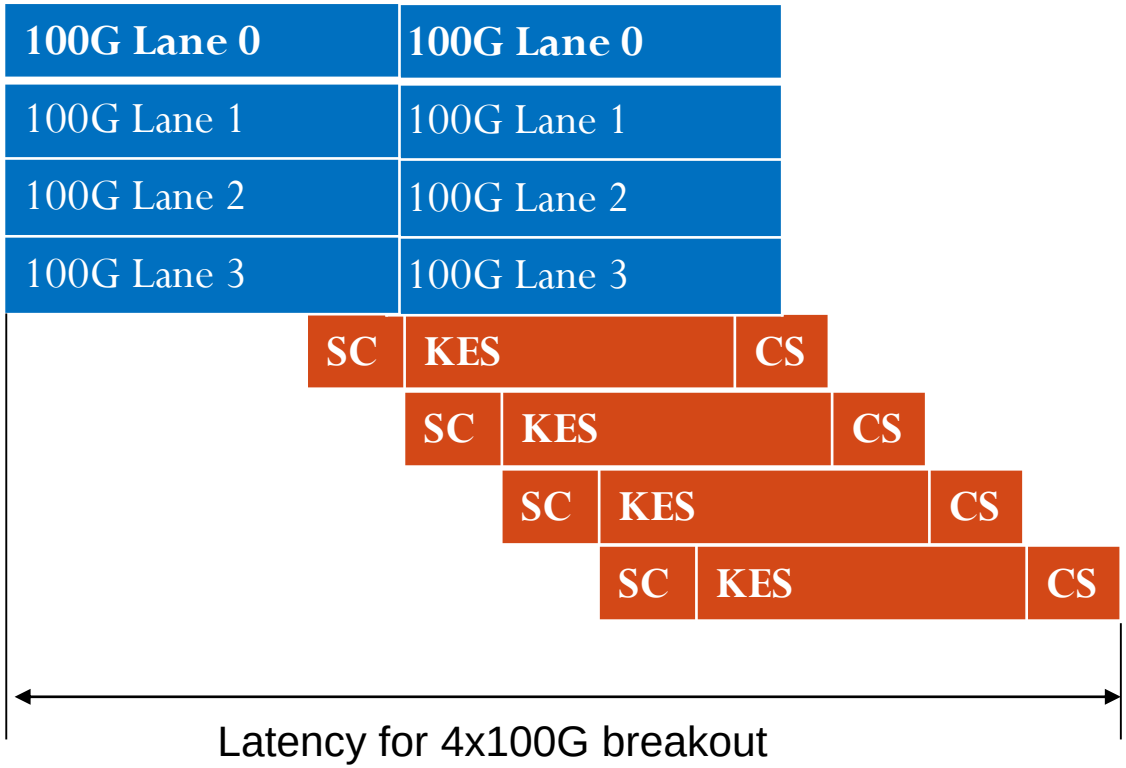
- Breakout for n low speed ports, 4x100G, 8x50G, or 16x25G?
  - Logic sharing: extra logic (or engines) of encoder and syndrome calculator for 4x100G breakout, more expensive for 8x50G and 16x25G breakout.
  - Time sharing: extra latency and memory.
  - For a basic time sharing decoder, latency is roughly:

    frame latency+ (n-1)*8+KES+CS+ Tb cycles, Tb is the latency of the second buffer.

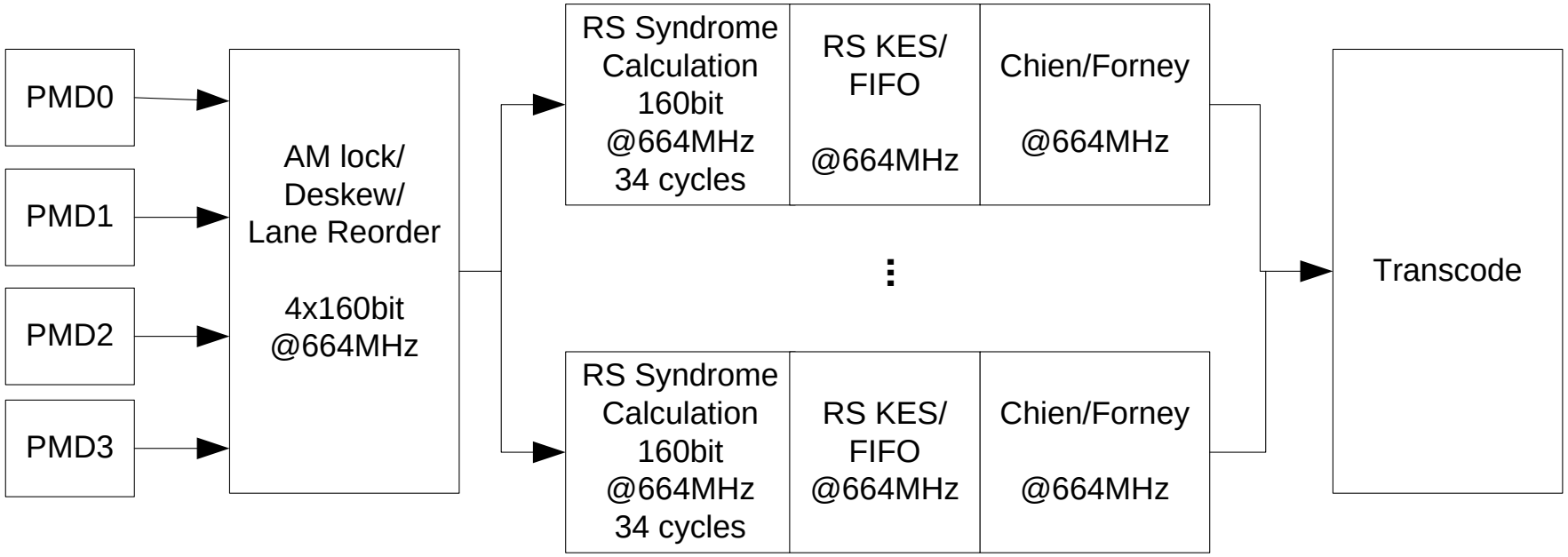


1x400G FEC: Breakout

- Latency illustration:



4x100G FEC: Architecture



- Easy clock scheme. Clean data path MUX to support 4x100G, 8x50G, and 16x25G.
- Frame latency is 5440/160=34 cycles.
- Latency: 34 cycles for syndrome calculation, 30 cycles for KES, and 8+1 cycles for Chien/Forney.

4x100G FEC: Implementation Analysis

- clock scheme: 160bit@664MHz
- Latency: decoder 110ns, encoder 3ns
- Complexity:
  - 4x1 KES
  - RS Chien/Forney: 4 copies if assuming the same processing time as 1x400G FEC
  - Encoder: 4 copies
- Breakout?
  - 4x100G: Natural.
  - 8x50G: similar to 1x400G FEC.
  - 16x25G: similar to 1x400G FEC.

Latency and Complexity

- Decoder Latency: 1x400G FEC has shorter latency w/o breakout, longer latency is needed for breakout by time sharing.

Breakout	1x400G	4x100G
1x400G FEC Latency (ns)	72	198 by time sharing 146 by logic sharing
4x100G FEC Latency (ns)	110	110

- Complexity: 1x400G FEC is smaller if assuming the same processing time. Extra logic is needed for breakout by logic sharing.
- Memories needed for breakout by time sharing:

Breakout	1x400G	4x100G
1x400G FEC Memory	0	8
4x100G FEC Memory	0	0

- Encoder: 1x400G FEC needs extra logic for breakout without latency penalty from time sharing.

Conclusions

- 1x400G FEC has shorter latency
- 1x400G FEC has less complexity for this low latency implementation.
- 4x100G FEC has less latency for breakout.