1x400G vs 4x100G FEC Implications

IEEE P802.3bs 400 Gb/s Ethernet Task Force

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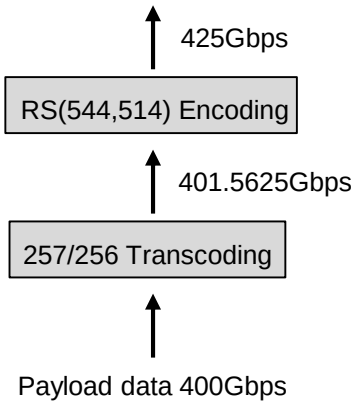
Introduction

- This presentation takes a look at the differences in implementation of a 1x400G and a 4x100G FEC architecture
- This implementation type/style is just one valid option, there are many ways to implement the architecture
- The sizing data presented is a combination of real design data and the results from micro architecture analysis and extrapolation

Data Rates

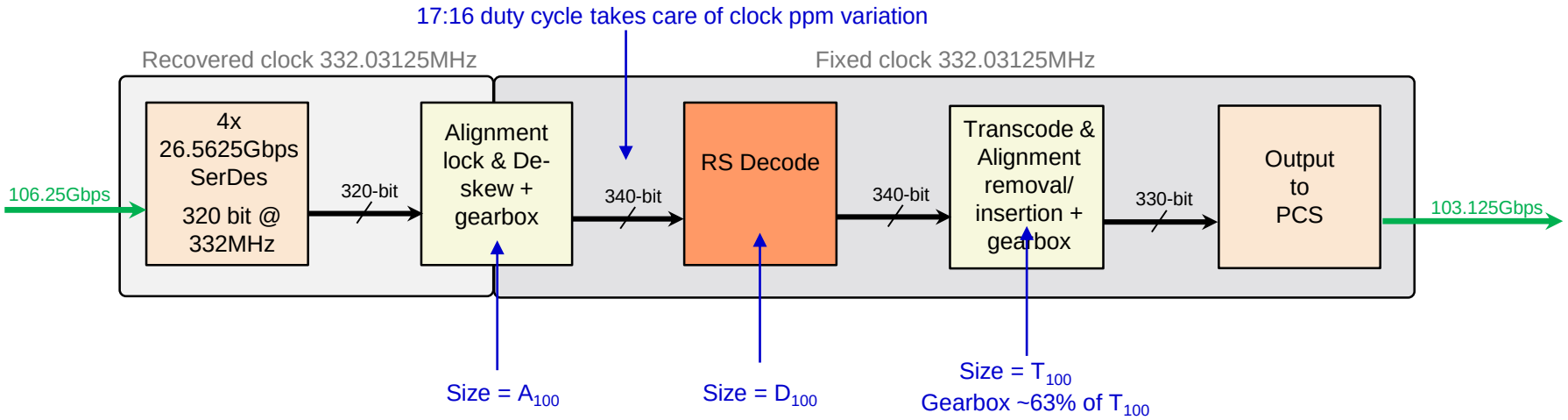
- These bus widths, clock frequencies and data rates are investigated in this presentation



Input	Input Data Rate	Input Width	Nominal Input Clock Frequency	Cycles per RS Codeword
KP4 400Gbps FPGA	425Gbps	1280	332.03125MHz	4.25
FPGA RS Decoder	451.5625Gbps	1360	332.03125MHz	4
KP4 400Gbps ASIC	425Gbps	640	664.0625MHz	8.5
ASIC RS Decoder	451.5625Gbps	680	664.0625MHz	8

4x 100G Datapath: 340-bit Decoder

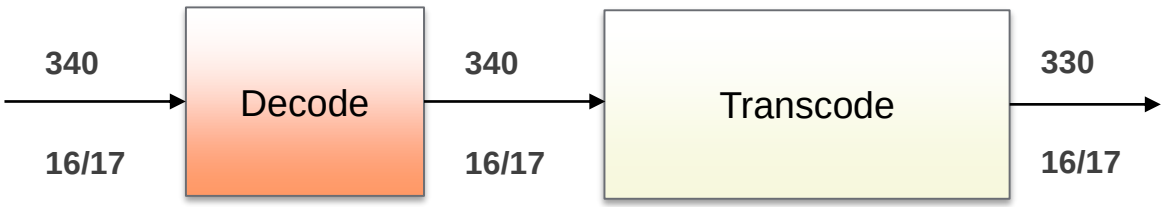
- Current FPGA appropriate bus widths and clock frequencies
- Uses free running local clock for most of the circuitry
  - Running off a local clock with periodic gaps eases design issues with unstable clocks
- Gearboxing from 320b to 340b is essentially free since this logic is used for alignment, re-ordering etc.

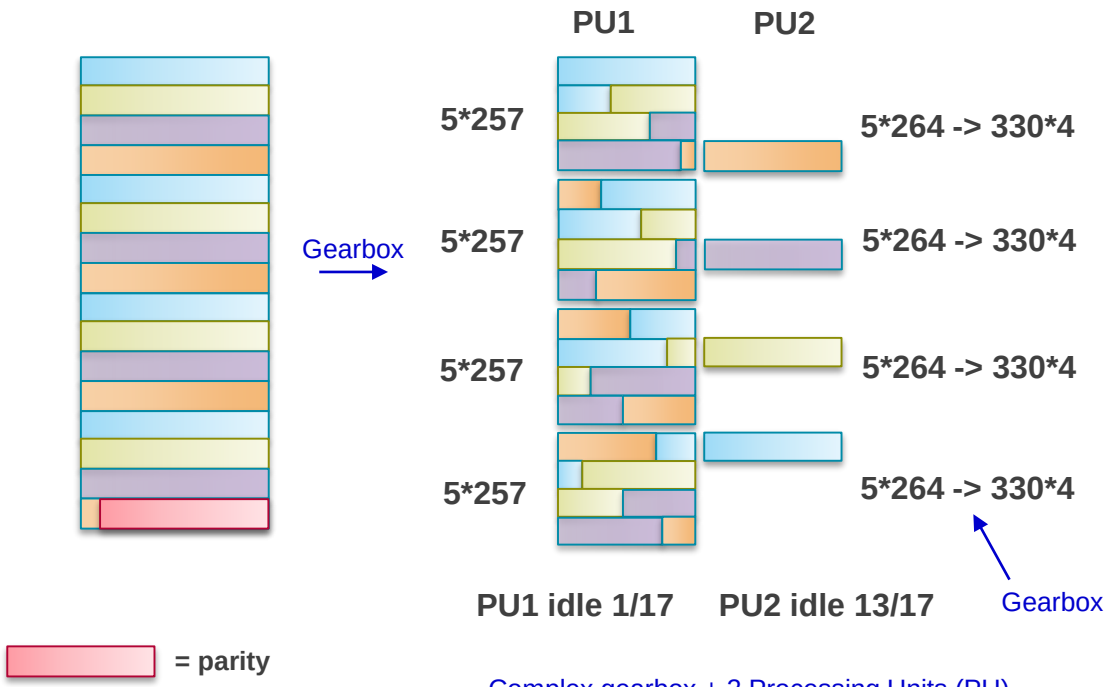


x4

100G Transcode Gearboxing: 340-bit Decoder

- Gearbox complexity is high for this option



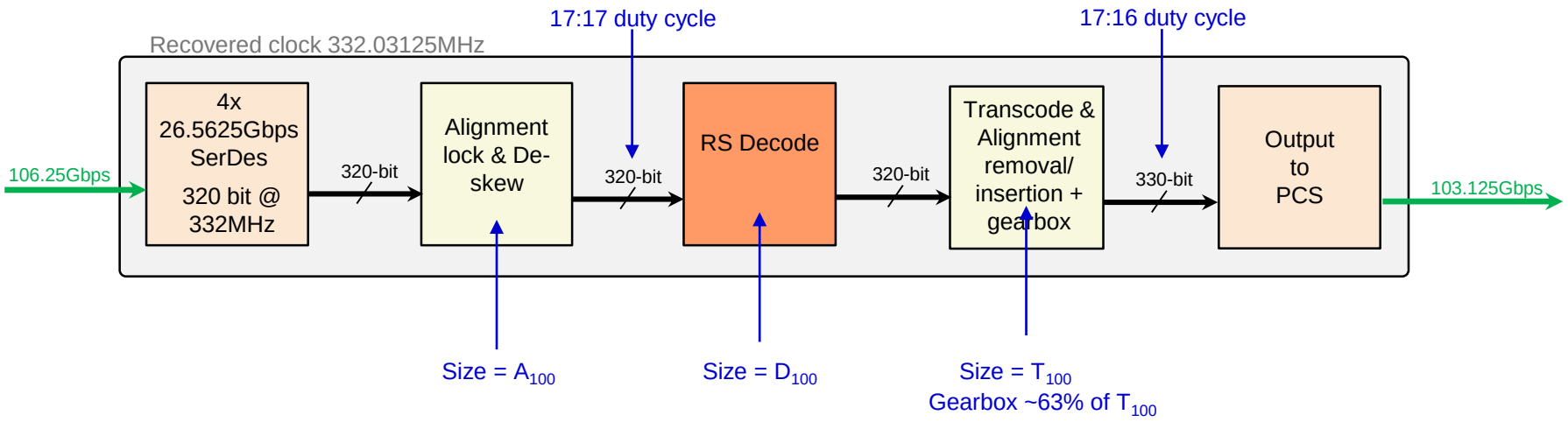


Buffer input mux is 16:1
PU1 Gearbox mux is 16:1
PU2 Gearbox mux is 4:1
Output gearbox needed.to convert from 5*264 to 4*330

Complex gearbox + 2 Processing Units (PU)

4x 100G 332MHz Datapath: 320-bit Decoder

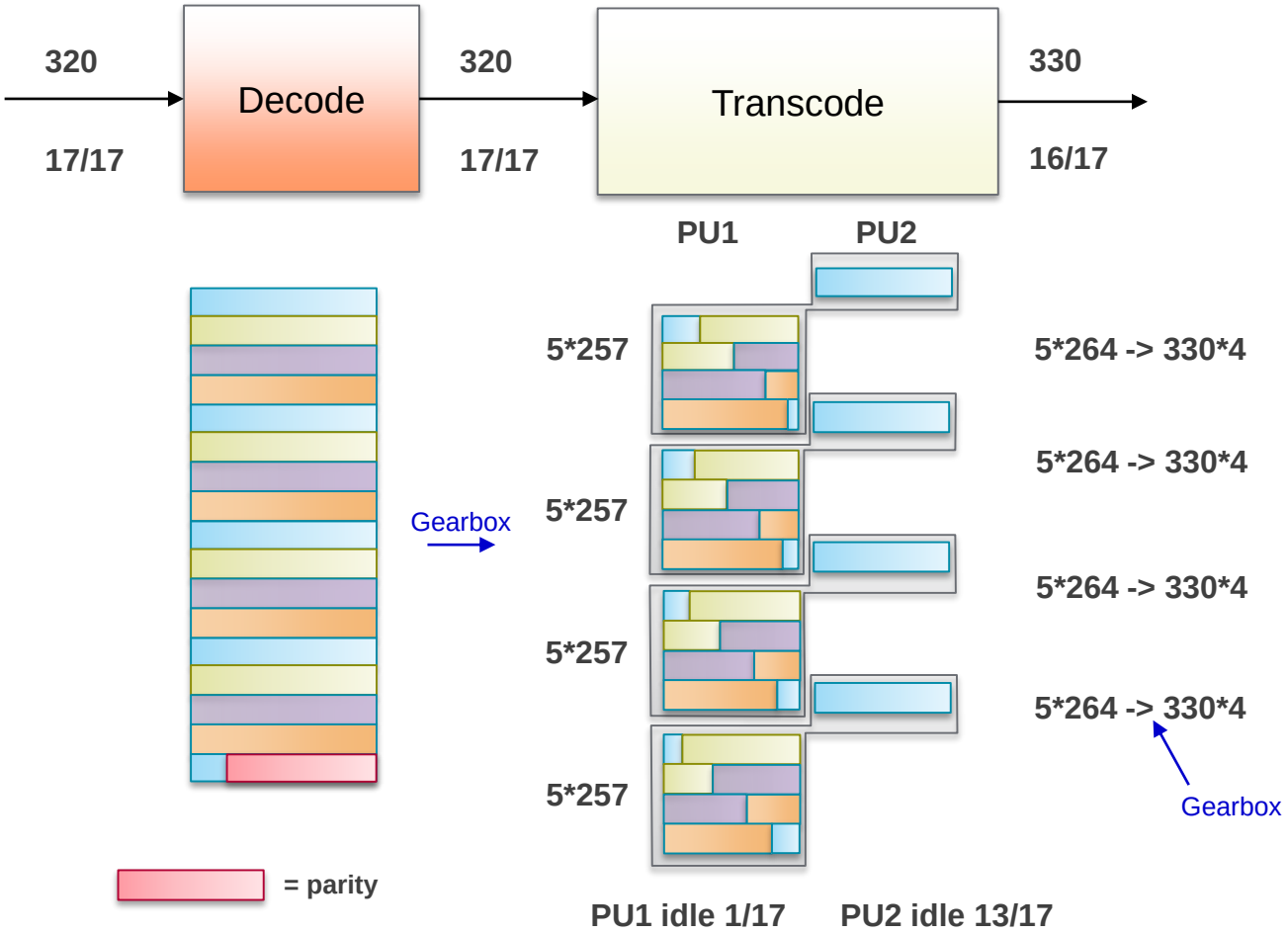
- Current FPGA appropriate bus widths and clock frequencies
- Uses recovered clock for all of the circuitry
  - Drawback of dealing with a potentially unstable clock
- No gearbox required on Alignment lock and De-skew



x4

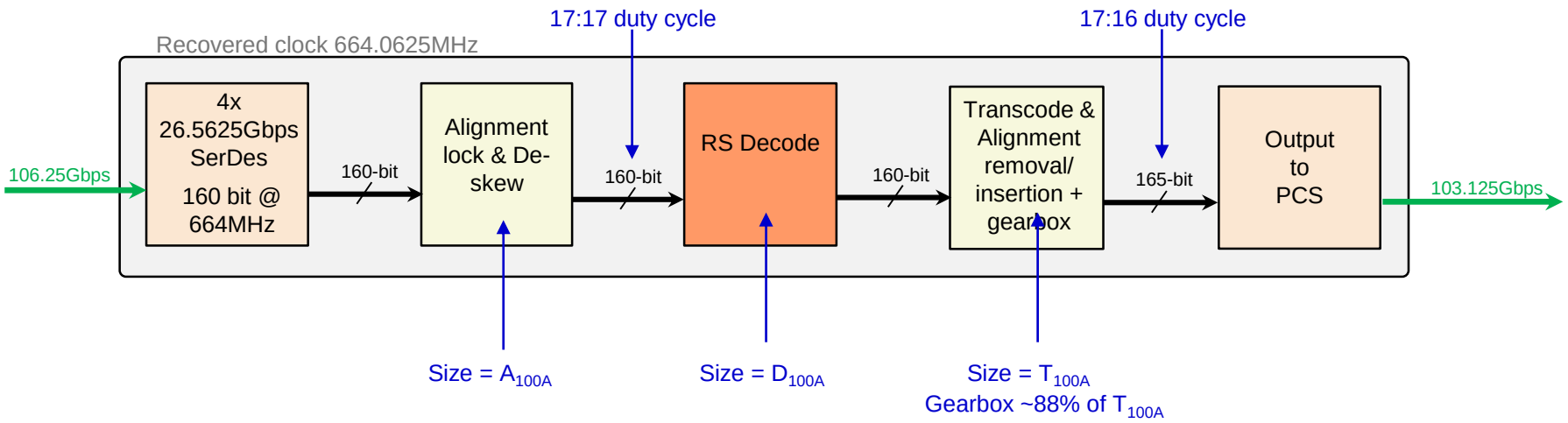
100G Transcode Gearboxing: 320-bit Decoder

- Gearbox complexity is high for this option, similar to the 340b decoder



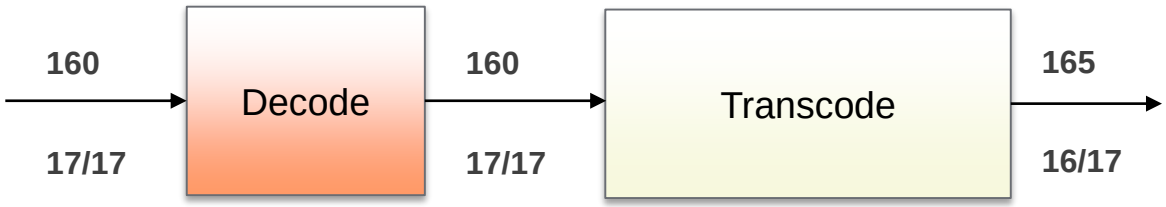
4x 100G 664MHz Datapath: 160-bit Decoder

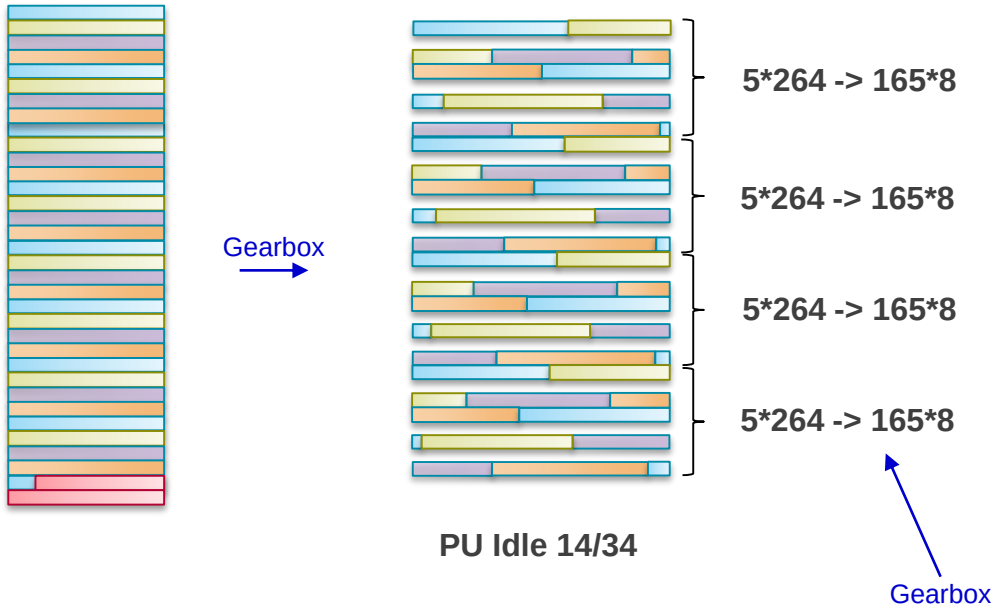
- Current ASIC and future FPGA appropriate bus widths and clock frequencies
- Uses recovered clock for all of the circuitry
  - Drawback of dealing with a potentially unstable clock
- No gearbox required on Alignment lock and De-skew



100G Transcode Gearboxing: 160-bit Decoder

- Gearbox complexity is high for this option

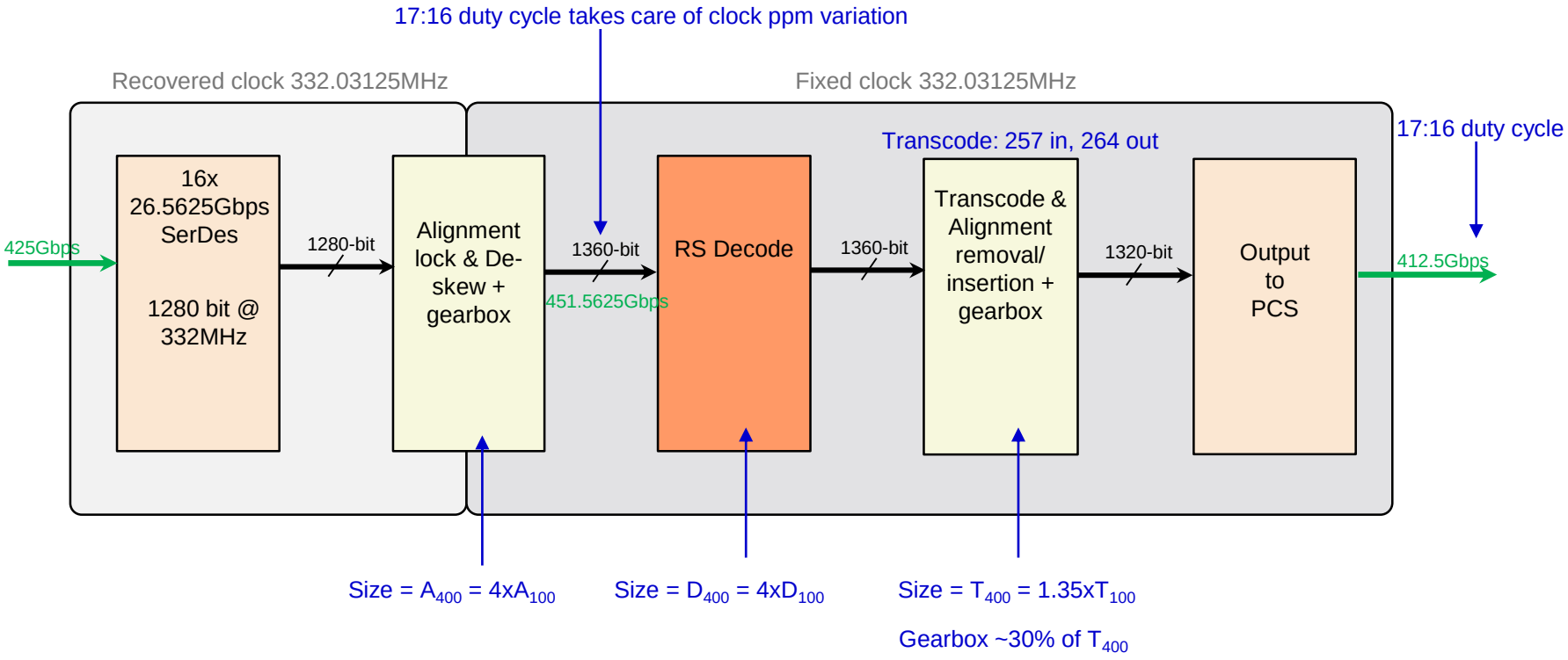




Buffer input mux is 33:1
PU Gearbox is 20:1 mux
Output gearbox needed.to convert from 5*264 to 8*165

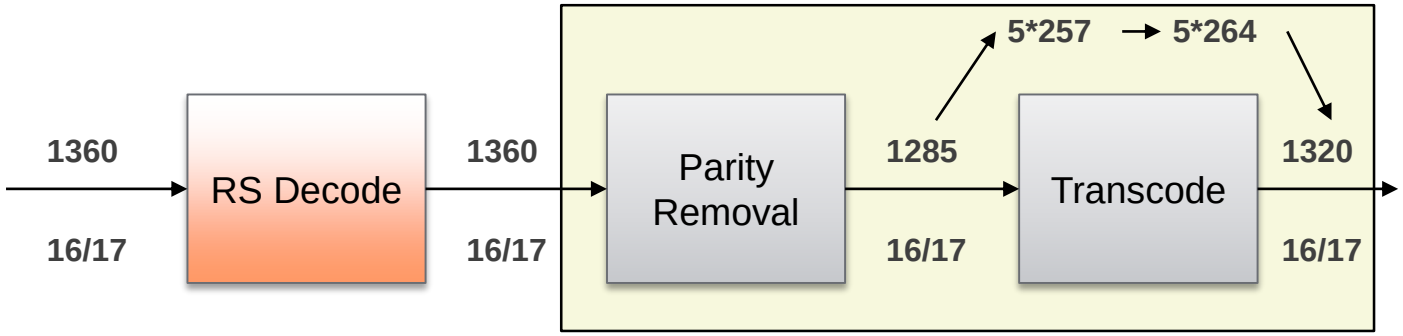
1x400G 332MHz Datapath

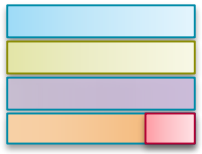
- Current FPGA appropriate bus widths and clock frequencies
- Uses free running local clock for most of the circuitry
  - Running off a local clock with periodic gaps easies design issues with unstable clocks
- Gearboxing from 1280b to 1360b is essentially free since this logic is used for alignment, re-ordering etc.



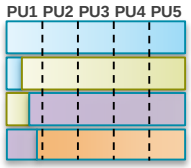
1x400G Transcode Gearboxing: 1360-bit Decoder

- Low complexity gearboxing for this option





1 RS Codeword
4 cycles of 1360 bits



4 cycles of 1285 bits

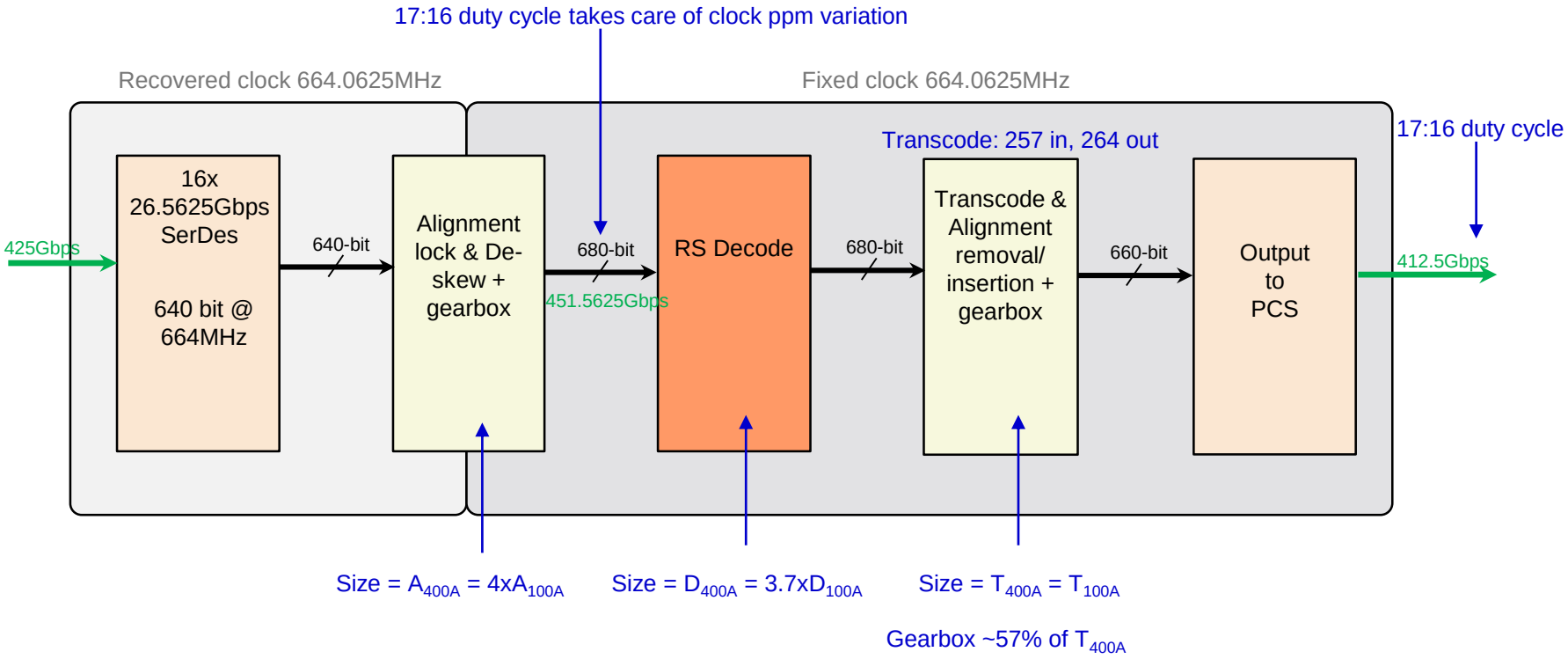
Buffer input mux is 4:1
Gearbox mux is 4:1
No output gearbox needed.

= parity bits

Simple gearbox + 5 Processing Units (PU), busy 100% of the time

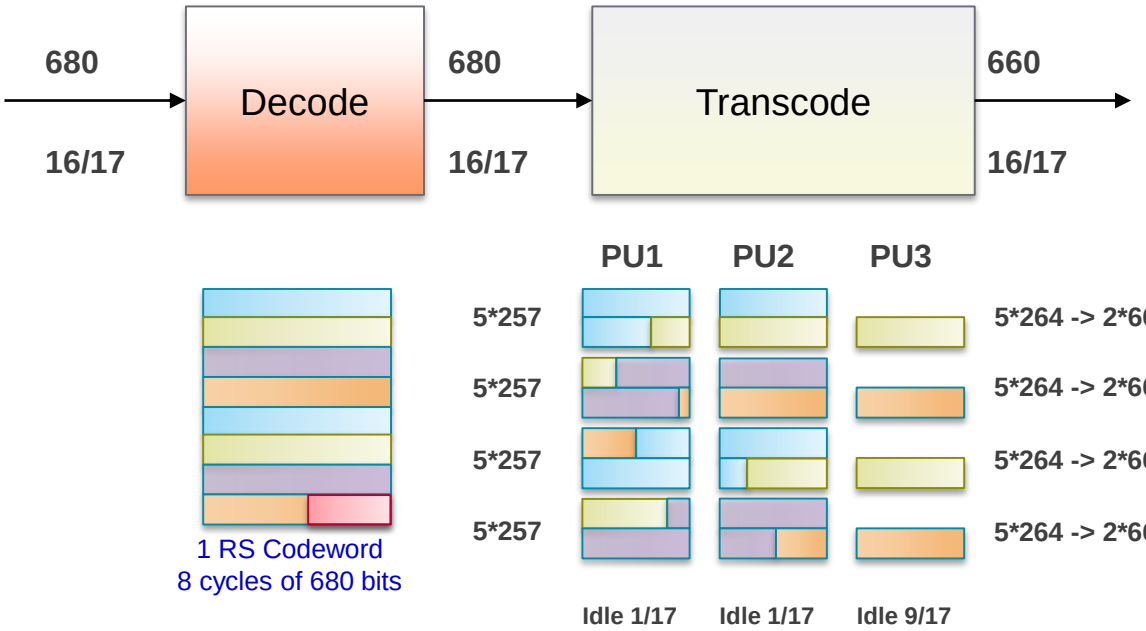
1x400G 664MHz Datapath

- Current ASIC and future FPGA appropriate bus widths and clock frequencies
- Uses free running local clock for most of the circuitry
  - Running off a local clock with periodic gaps easies design issues with unstable clocks
- Gearboxing from 640b to 680b is essentially free since this logic is used for alignment, re-ordering etc.



400G Transcode Gearboxing: 680-bit Decoder

- Medium complexity gearboxing for this option

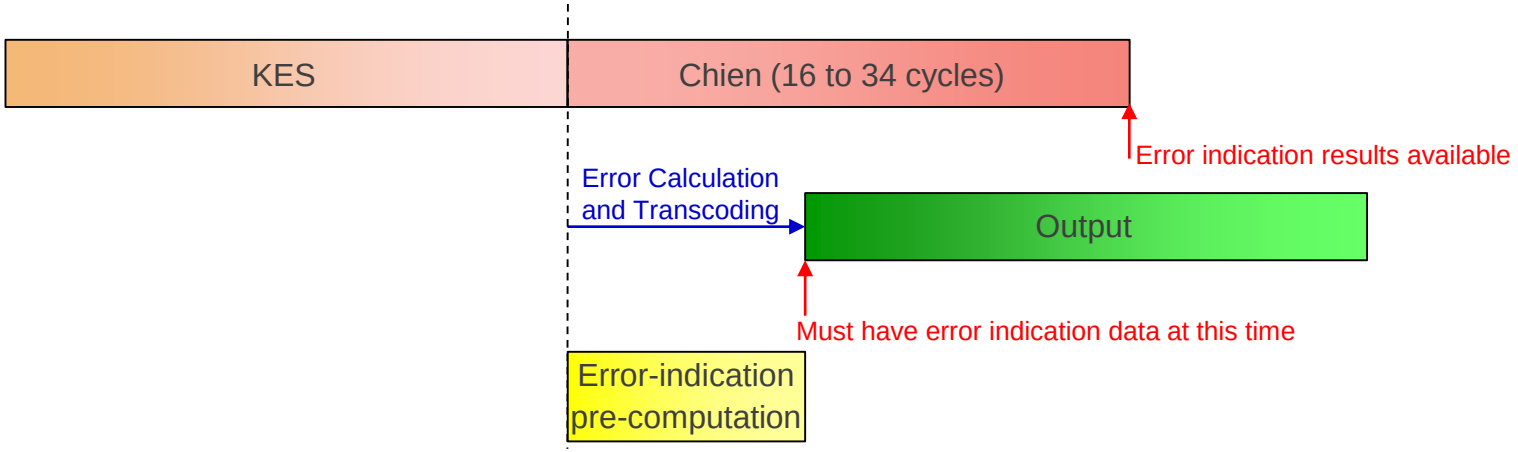


Gearbox + 3 Processing Units

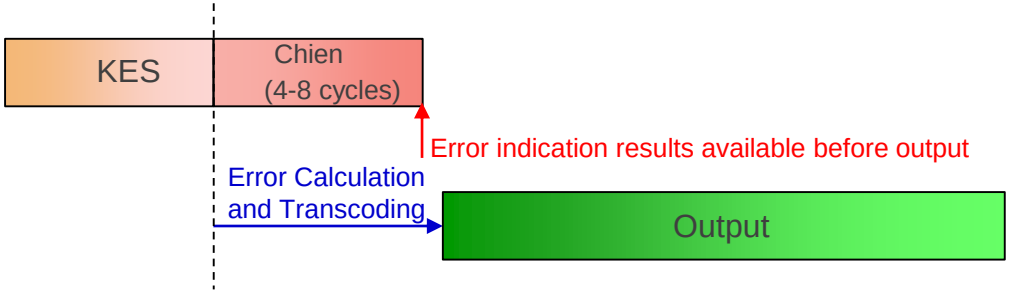
Buffer input mux is 8:1
PU1 & PU2 gearbox mux's are 8:1
PU3 gearbox mux is 4:1
Output gearbox needed.to convert from 5*264 to 2*660

Error Indication Implications

- 100G: needs additional logic to pre-compute error indication



- 400G: error indication results available in time



Size Comparison: 332MHz Clock

- **4x100G**
  - 100G RS Decoder, size = D_{100}*
  - 100G Alignment, lock and de-skew & gearboxes, size = A_{100} ~= $0.131D_{100}$
  - 100G Transcode, alignment removal & gearboxes, size = T_{100} ~= $0.094D_{100}$
  - 4x100G overall size = 4 * (D_{100} + A_{100} + T_{100}) ~= $4.9D_{100}$

- **1x400G**
  - 400G RS Decoder, size = D_{400} ~= $4D_{100}$
  - 400G Alignment, lock and de-skew & gearboxes, size = A_{400} ~= $4A_{100}$
  - 400G Transcode, alignment removal & gearboxes, size = T_{400} ~= $1.35T_{100}$
  - 400G overall size = D_{400} + A_{400} + T_{400} ~= $4.7D_{100}$

* Note: 100G Decoder would be larger if error indication had to be implemented. This would not affect 400G Decoder, so 100G solution would be even larger than 400G in reality.

Size Comparison: 664MHz Clock

- **4x100G**
  - 100G RS Decoder, size = D_{100A}*
  - 100G Alignment, lock and de-skew & gearboxes, size = A_{100A} ~= $0.187D_{100A}$
  - 100G Transcode, alignment removal & gearboxes, size = T_{100A} ~= $0.272D_{100A}$
  - 4x100G overall size = 4 * (D_{100A} + A_{100A} + T_{100A}) ~= $5.84D_{100A}$

- **1x400G**
  - 400G RS Decoder, size = D_{400A} ~= $3.68D_{100A}$
  - 400G Alignment, lock and de-skew & gearboxes, size = A_{400A} ~= $4A_{100A}$
  - 400G Transcode, alignment removal & gearboxes, size = T_{400A} ~= $0.94T_{100A}$
  - 400G overall size = D_{400A} + A_{400A} + T_{400A} ~= $4.68D_{100A}$

* Note: 100G Decoder would be larger if error indication had to be implemented. This would not affect 400G Decoder, so 100G solution would be even larger than 400G in reality.

Conclusion

- Both 4x100G and 1x400G architectures are implementable in both current ASIC and FPGA technology
- Gearboxing on either side of the decoder is not a concern, the logic is already there to do this function as part of the other required functions
- A 1x400G FEC architecture has a small size advantage