Generating Variable Transition Density Patterns

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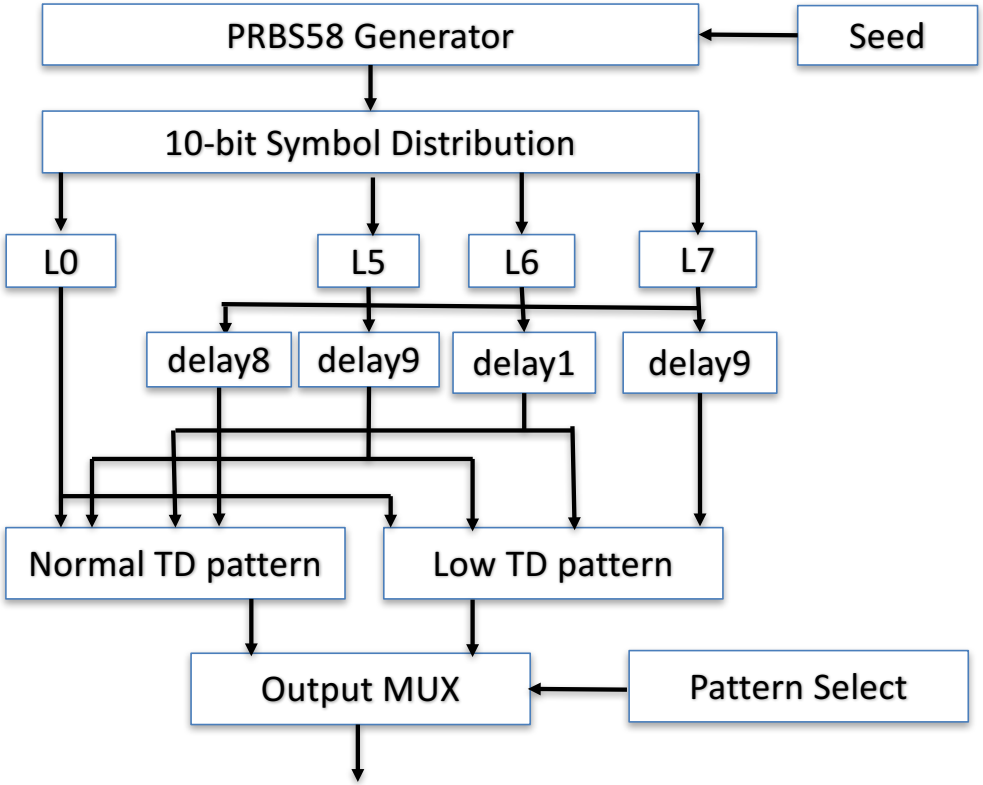
Background

- **It has been identified that a certain PCS when muxed with specific delay causes reduction in PAM4 transition density (TD) from 0.75 to ~0.683**
  - http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf
- **Follow on contribution showed that impact of reduction in transition density is reduction in CDR BW http://www.ieee802.org/3/bs/public/adhoc/logic/feb16_17/ghiasi_01_0217_logic.pdf**
  - Symmetrical transition through the signal average – nominal TD 25% pathological PCS sequence results in 28% reduction in TD
  - All transitions through signal average – nominal TD 50% immune to TD reduction
  - All transitions – nominal TD 75% pathological PCS sequence results in 9% reduction in TD
- **TD variation in this range can be tolerated by a good CDR design**
  - Most modern CDR tolerate TD reduction and the associated reduction in the CDR BW
- **This contribution investigate generation of lower TD test patterns to test CDR with to improve JTOL test coverage instead of forcing higher corner frequency (5.56 MHz) on all CDRs.**

How to Generate Low TD Test Patterns

- **Use the IEEE PRBS58 scrambler $G(x) = 1 + x^{39} + x^{58}$**
  - Suitable for protocol aware test and ASIC/FPGA
  - Cumbersome for optics/PMD testing
- **PRBSQ with lower TD**
  - Suitable for optics/PMD testing
  - Could be implemented in the BERT and SerDes, etc.
- **SSPRQ with variable TD**
  - For improve CDR JTOL coverage by having variable TD where CDR BW varies as result of TD
  - Could be implemented in BERT and SerDes, etc

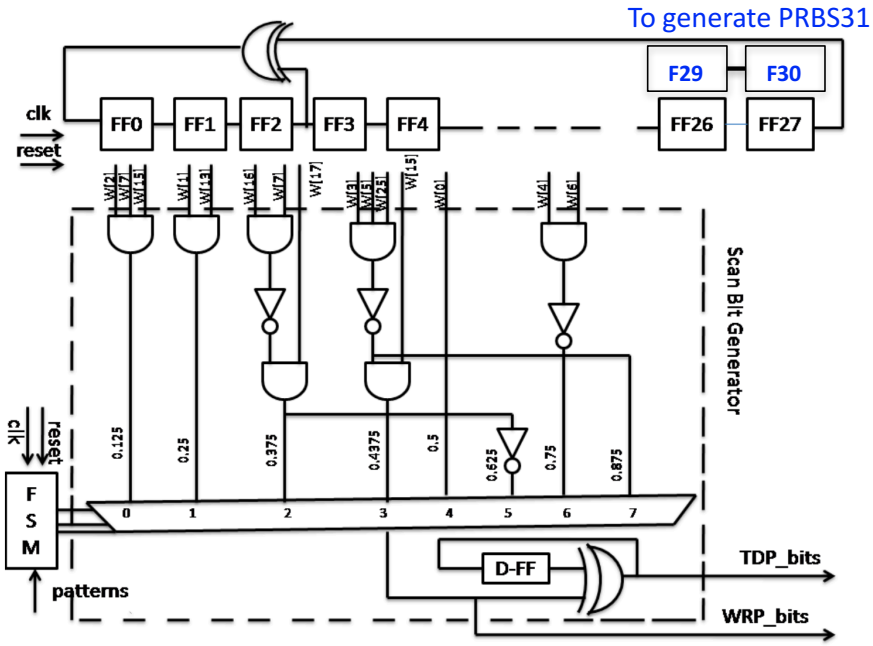
Generating Worst Clock Content Scrambled Pattern



- **Pattern Select toggles between normal and lower TD patters every certain bits**

How to Generate Specific TD PRBS31 Pattern

- **Simple combinatory out of the LFSR can generate variable weighted random, *px*, pattern**
  - The LFSR28 implementation generates pattern with *px* from 0.125 to 0.875 with step of 0.125
  - The basic approach can be extended to PRBS31 by adding 3 additional shift registers
  - For example combining two non-adjacent LFSR outputs generate *px*=0.25
  - $TD = p_0p_1 + p_1p_0 = 2p_1(1-p_1)$
    - Where $p_0 = (1-p_1)$.



Weighted Random and Transition Density Patterns For Scan-BIST
Farhana Rashid and Vishwani Agrawal
http://www.eng.auburn.edu/~agrawvd/TALKS/NATW12/natw_Rashid.pdf

How to Generate Specific TD PRBS31 Pattern

- **Worst case transition density TD due to clock content reported is ~0.683 (-8.9%)**
  - P=0.375 can generate TD of 0.703 (-6.3%) close to worst case TD report
  - We are investigating other combinatory implementations to get closer to worst case TD of ~0.683.

p	TD - NRZ	TD – PAM4
0.125	0.218	0.3281
0.25	0.375	0.5625
0.375	0.4688	0.703
0.4375	0.4922	0.738
0.5	0.5	0.75
0.625	0.4688	0.7031
0.75	0.375	0.5625
0.875	0.2188	0.3281

How to Generate Variable TD SSPRQ

- **SSPRQ pattern is a repeating 216-1 PAM4 symbol sequence constructed out of 3 sections of PRBS31 as shown in table 120-2 sequence A**
  - Sequence B is two repetition of sequence A with 1st and last bit removed creating 65534 bit sequence

Table 120–2—SSPRQ bit sequence A

Pattern	Seed	Length
PRBS31	0x00000002	10924 bits
	0x34013FF7	10922 bits
	0x0CCCCCCC	10922 bits

- **To test CDR loop response it is best to transmit normal TD pattern at least for duration of CDR loop response then switch to low TD pattern**
  - With CDR BW=4 MHz (0.25 μs) each pattern duration should be about the CDR loop response
  - Transmission duration of sequence A 32767 bits @53.1 GBd = 0.31 μs
- **Bit sequence B with length of 65534 per definition of 120.5.11.2.3 can be formed by cascading sequence having PAM4 TD of 0.75 then followed by 2nd sequence having PAM4 TD of 0.703 PAM4 creating variable TD data pattern.**

Summary

- **Reduction in TD (transition density) will reduce the nominal CDR BW**
- **TD of pathological lanes are 9% to 28% lower than normal, and can be tolerated by a well designed CDR.**
  - Although the maximum CDR BW may be limited by latency in CDR loop, CDR BW can be adjusted
- **Instead of testing all CDRs with higher JTOEL corner a better approach is to test the CDR with worst case clock content data pattern**
- **Worst clock content can be generated**
  - With scrambled X^58 data
  - With PRBS31Q with lower TD
  - SSPRQ pattern where one section is replaced with PRBS31 with lower TD creating variable TD data pattern
- **The overall clock content impact on the CDR is minor but it is best practice to define a data pattern to test for worst case TD**
- **Need to investigate and get feedback on the complexity of the pattern checker.**