Impact of Clock Content on the CDR with Propose Resolution

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IEEE 802.3bs Logic Adhoc

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List of supporters

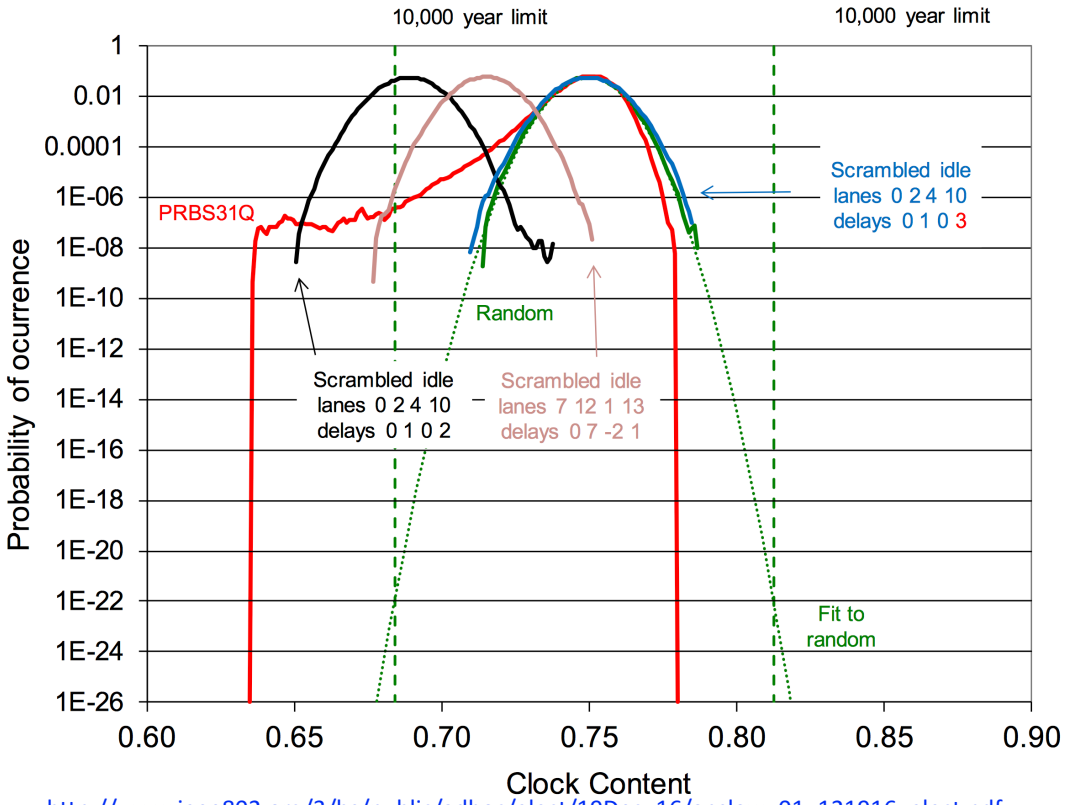
- **Eric Baden – Broadcom**
- **Rob Stone - Broadcom**

Background

- **In support of comments 92 and 93.**
- **It has been identified that a certain PCS when muxed with specific delay causes reduction in PAM4 transition density (TD) from 0.75 to ~0.683**
  - http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf
- **Follow on contribution showed that impact of reduction in transition density is reduction in CDR BW http://www.ieee802.org/3/bs/public/adhoc/logic/feb16_17/ghiasi_01_0217_logic.pdf**
  - Symmetrical transition through the signal average – nominal TD 25% pathological PCS sequence results in 28% reduction in TD
  - All transitions through signal average – nominal TD 50% immune to TD reduction
  - All transitions – nominal TD 75% pathological PCS sequence results in 9% reduction in TD
- **TD variation in this range can be tolerated by a good CDR design**
  - Most modern CDR tolerate TD reduction and the associated reduction in the CDR BW
  - Understanding of the subject is important before attempting to make substantive change to the draft
- **This contribution investigate feasibility of using existing SSPRQ as well as defining new test patterns to improve the CDR JTOL test coverage by protecting against worst case clock content.**

The Extent of Clock Content Issue for All Transitions

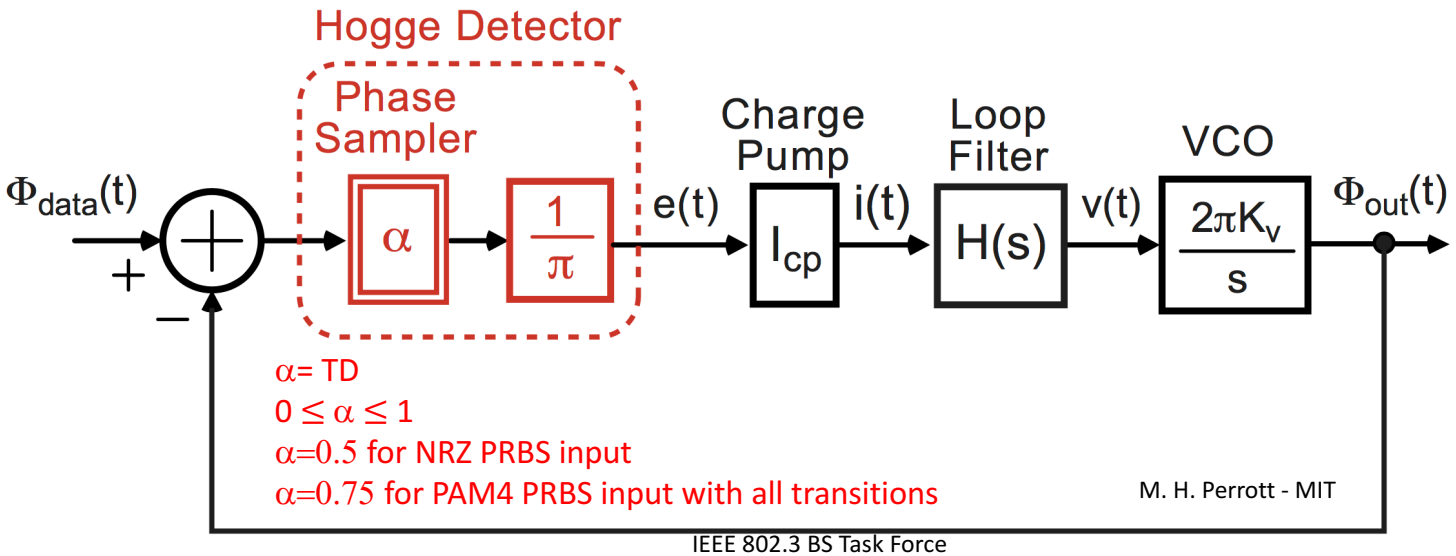
- **Lets assume given CDR operates with all transitions and the nominal CDR BW=4MHz**
- **High probability occurrence determine CDR BW with low probability occurrences washed out**
  - PRBS31Q with peak TD=0.75 and large left shoulder may result in negligible reduction in CDR BW from 4 MHz
  - Scrambled idle (blue) and random data will result in CDR BW of 4 MHz
  - Scrambled idle (pink) with TD=0.72 results in CDR=3.84 MHz
  - Scrambled idle (black) with TD=0.683 results in CDR BW=3.64 MHz
- **Given TD peak the CDR BW reduction is pretty much determined proportionally by TD shift.**



http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf

Basic Operation of the CDR

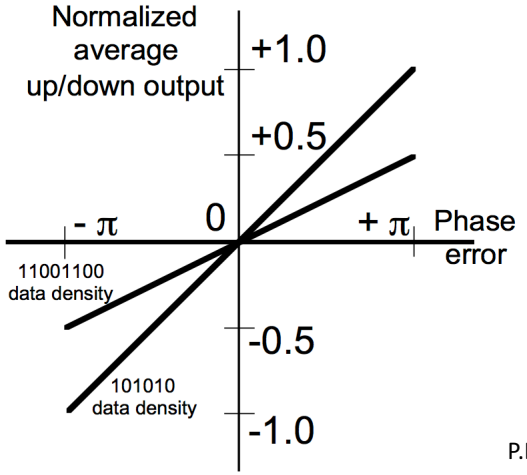
- **Key element of CDR are the phase detector, charge pump, loop filter and VCO**
  - Common implementation of phase detector is based on Hogge Detector where TD affects the loop gain and loop BW
  - $CDR\ BW = Nominal\ loop\ BW \times TD$
- A CDR designed for 802.3bs applications has a BW of 4 MHz assuming nominal PAM4 TD.



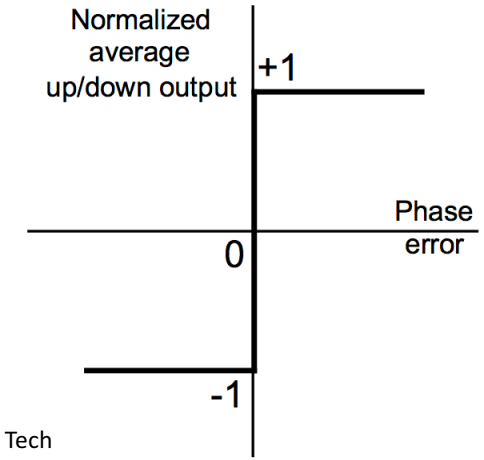
Transfer Characteristics of the Hogge Phase Detector

- **Example of linear and binary phase detector**
  - Linear phase detector response
    - Pattern 11001100 with TD=0.5 has gain of 0.5
    - Pattern 10101010 with TD=1.0 has gain of 1.0
- **A sophisticated CDR may have TD detector and accordingly adjust the loop gain to maintain target loop BW**
- **8B10B coding run length are limited to 5 bit but TD varies drastically or from 0.3 to 1.0!**

Linear Phase Detector



Binary Phase Detector

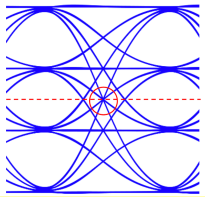


P.E. Allen-G. Tech

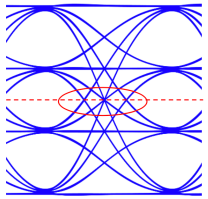
PAM4 CDR Implementation

- **PAM4 CDR architecture is very similar to NRZ with addition of PAM4 to Binary convertor**

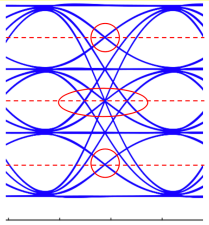
Symmetrical through average CDR



All transitions through average CDR



All transitions CDR



PAM4 to Binary Convertor

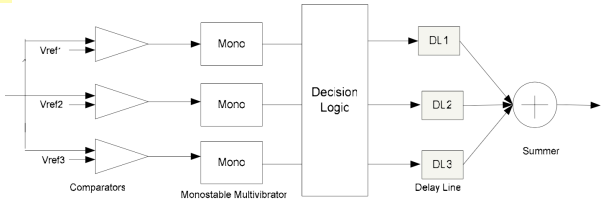
Simple PAM4 to Binary Convertor operating with 25% TD

PCS Pattern may Reduce TD to 0.18 Nominal CDR BW Reduces from 4 MHz to 2.88 MHz!

Simple PAM4 to Binary Convertor operating with 50% TD

PCS Pattern doesn't Change TD and CDR BW is not effected!

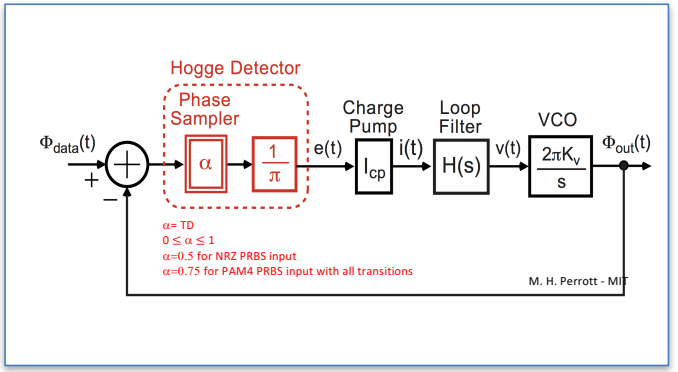
More robust implementation sampling all 3 eyes operating with 75% TD



Kim, Proceeding IDEAS 2005

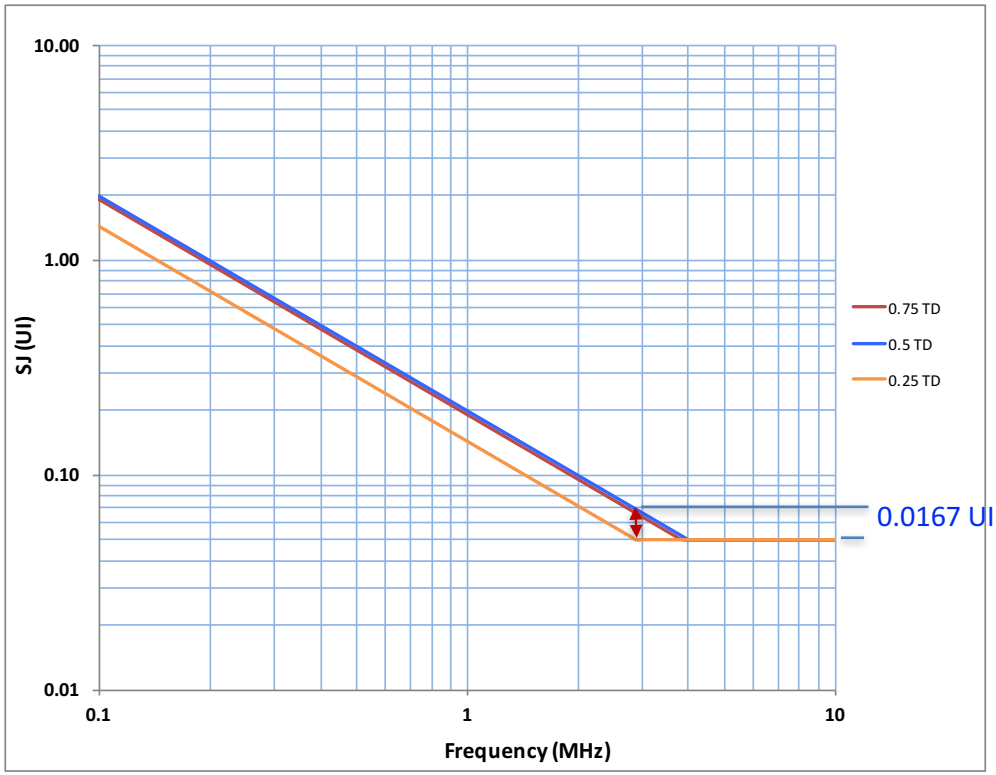
PCS Pattern may Reduce TD to 0.683 Nominal CDR BW Reduces from 4 MHz to 3.64 MHz!

Generic CDR



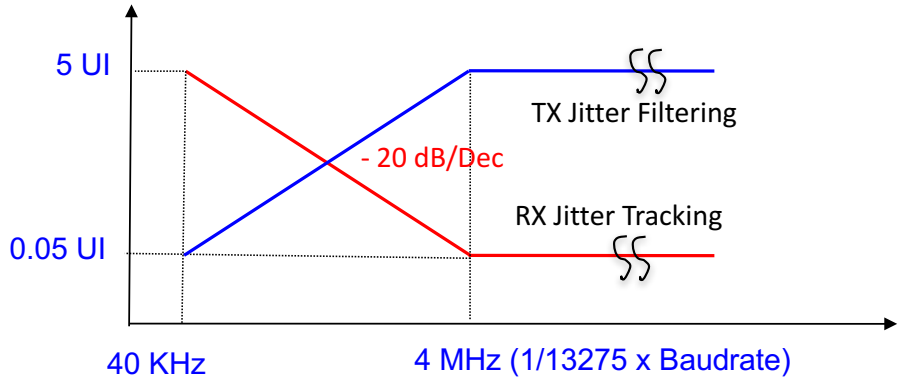
Penalty as Result of Clock Content on Jitter Tolerance

- **The three type of CDR**
  - A CDR operating with symmetrical transition through average corner frequency reduced to 2.88 MHz
  - A CDR operating with transition through average corner frequency remain 4 MHz
  - A CDR operating with all transition corner frequency reduced to 3.84 MHz
- **The worst case penalty as result of clock content for a CDR operating symmetrical transition through average is only 0.0167 UI!**
  - For CDR operating with all transitions is even less 0.0021 UI!



Could Existing JTOL Test Protect Against Clock Content?

- **Clock content issue as result of pathological PCS lane mux and delay has the effect of reducing CDR BW due to low transition density**
  - Yes it can, if the CDR is tested with a data pattern that has similar effect reducing CDR BW
  - Initial option investigated was to generate weighted PRBS with lower TD as a JTOL test
  - But if an existing data pattern can provide the necessary protection against clock content issue it would preferable at this point in project.



40 KHz

Testing CDR with Stress Pattern to Protect Against Worse Case Clock Content

- **SSPRQ pattern is a repeating 216-1 PAM4 symbol sequence constructed out of 3 sections of PRBS31 as shown in table 120-2 sequence A**
  - SSPRQ has variable TD from 0.65-0.74 and already more stressful than PRBS31 for the CDR
  - Sequence B is two repetition of sequence A with 1st and last bit removed creating 65534 bit sequence

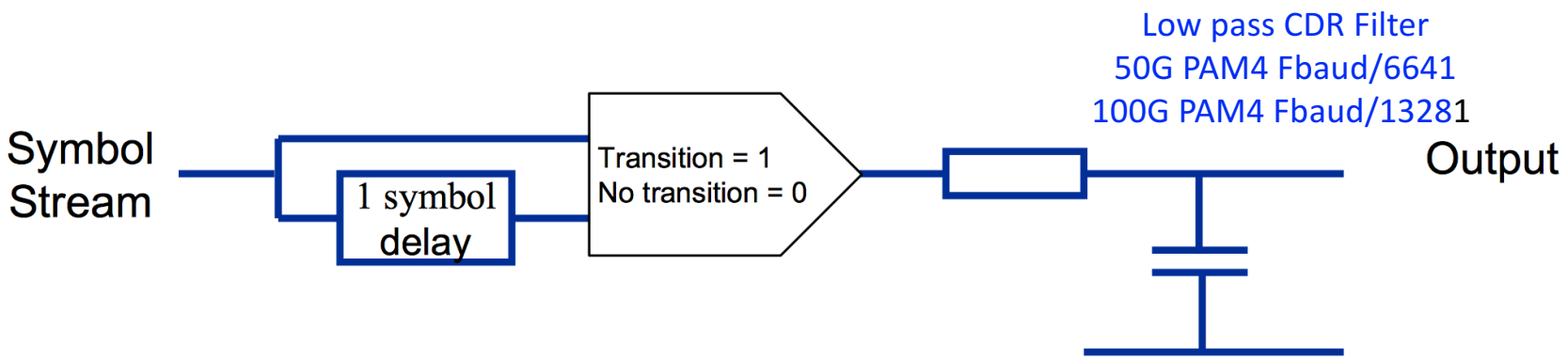
Table 120–2—SSPRQ bit sequence A

Pattern	Seed	Length
PRBS31	0x00000002	10924 bits
	0x34013FF7	10922 bits
	0x0CCCCCCC	10922 bits

- **Optional SSPRQ2 was created using standard PRBS31 for sequence A but using weighted PRBS31 having p1=0.328 for sequence B**
  - SSPRQ2 adds dual bell shape response to the SSPRQ
- **Given SSPRQ stresses the CDR more than the worst case clock content reported then it isnot necessary to use SSPRQ2!**

How Clock Content is Evaluated?

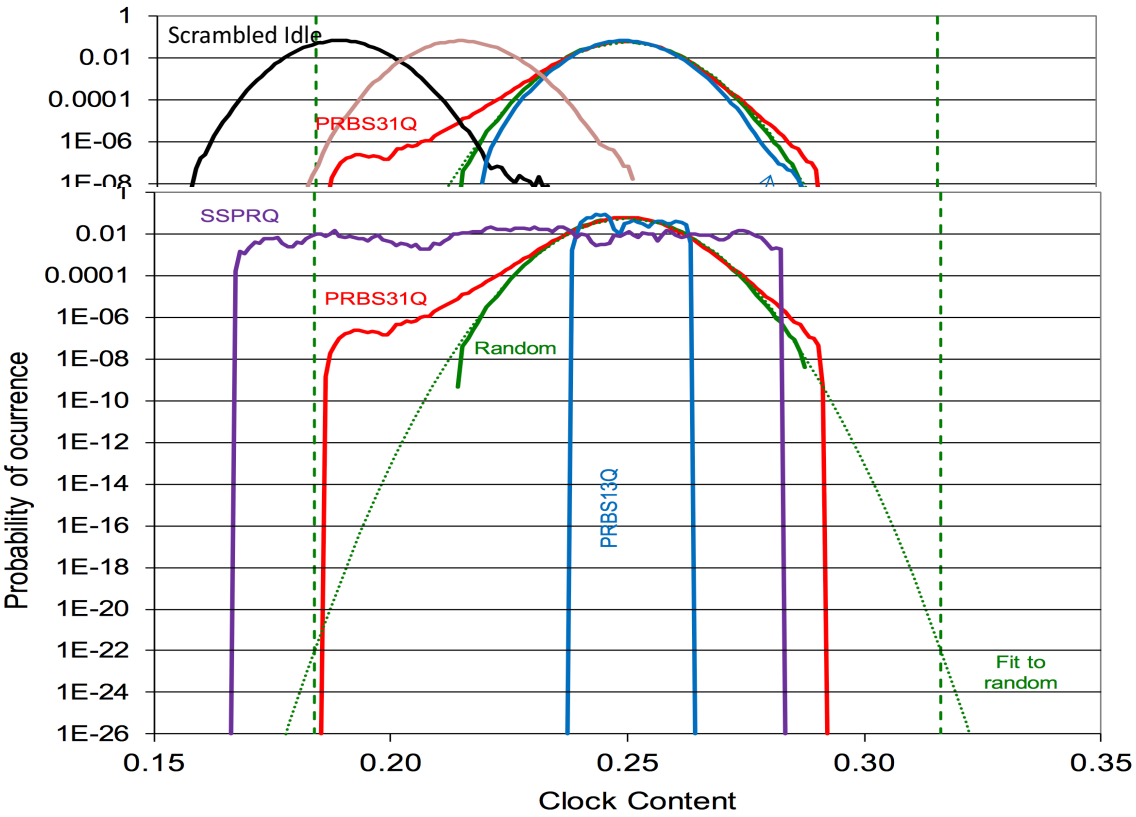
- **Data pattern transitions are filtered with a 4 MHz low pass filter**
  - The 4 MHz 1st order low pass filter represent CDR tracking to the data
  - See http://www.ieee802.org/3/bs/public/adhoc/logic/oct27_16/anslow_02a_1016_logic.pdf.



Comparing Worst Case Clock Content to SSPRQ

- **For symmetrical transition through average**
- **Existing SSPRQ test pattern for all transitions is actually much more stressful than worst case clock content scrambled idle (black)!**
  - TD data include a 4 MHz low pass filtered so the CDR loop BW will adjust proportionally to the reduction in the TD
  - For a bell shape TD the CDR stays at the center of the bell, scrambled idle(black) will result in 2.88 MHz BW
  - But for SSPRQ at ~0.01 probability of occurrence varying from 0.165-0.28 results in a CDR BW to drop to as low as 2.64 MHz, which is more stressful than scrambled idle (black) on the top graph!

http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf



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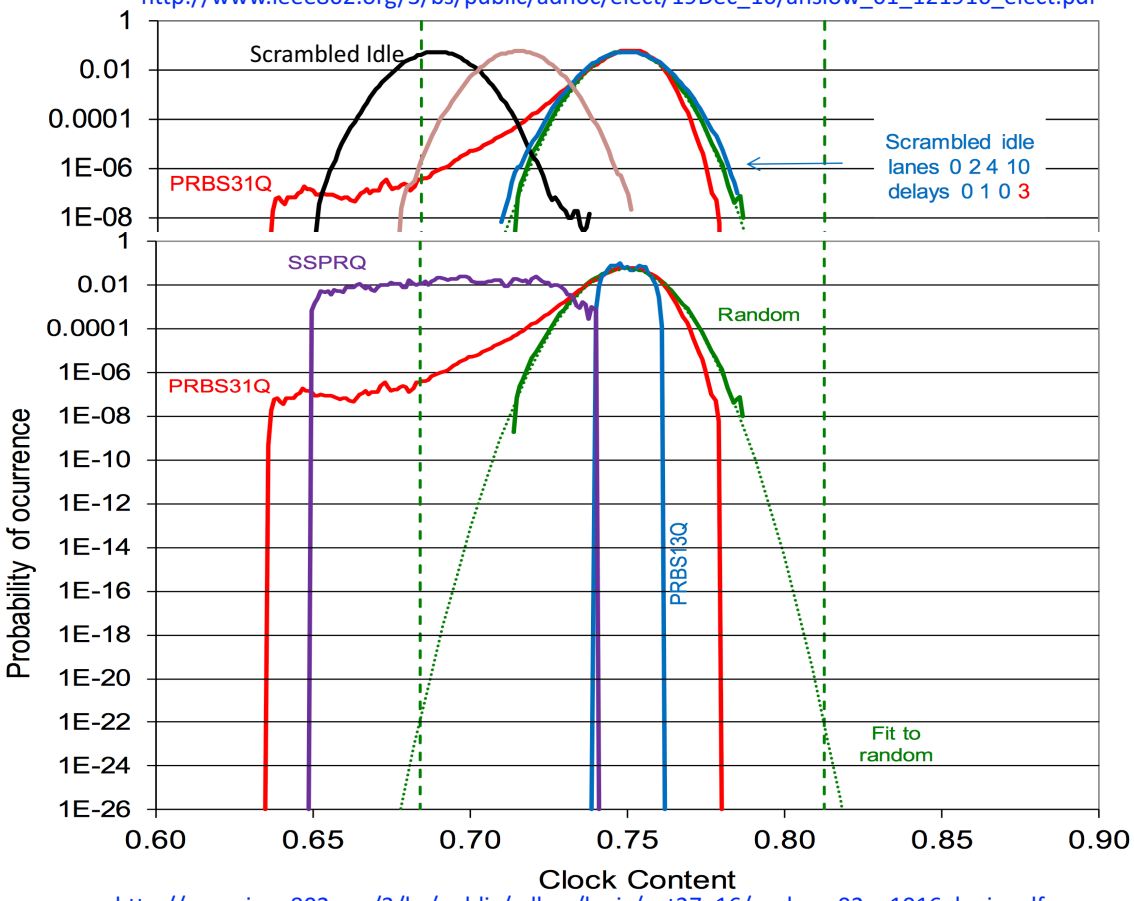
Comparing Worst Case Clock Content to SSPRQ

- **For all transitions**
- **Existing SSPRQ test pattern for all transitions is actually more stressful than worst case clock content scrambled idle (black)!**
  - TD data include a 4 MHz low pass filtered so the CDR loop BW will adjust proportionally to the reduction in the TD
  - For a bell shape TD the CDR stays at the center of the bell, scrambled idle(black) will result in 3.84 MHz BW
  - But for SSPRQ at ~0.01 probability of occurrence varying from 0.65-0.74 results in the CDR BW to drop to as low as 3.47 MHz, which is more stressful than scrambled idle (black)!

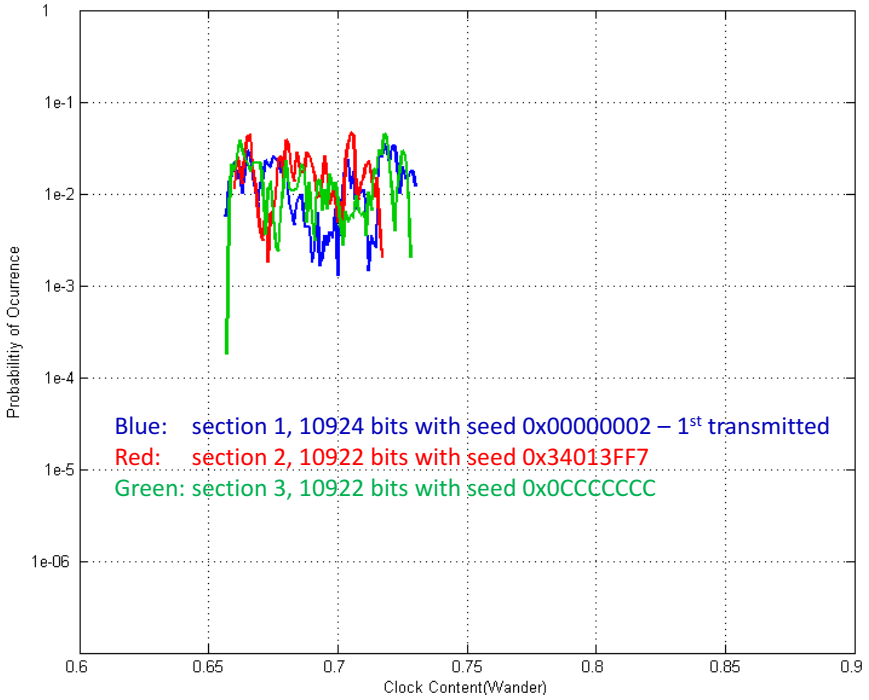
http://www.ieee802.org/3/bs/public/adhoc/elect/19Dec_16/anslow_01_121916_elect.pdf

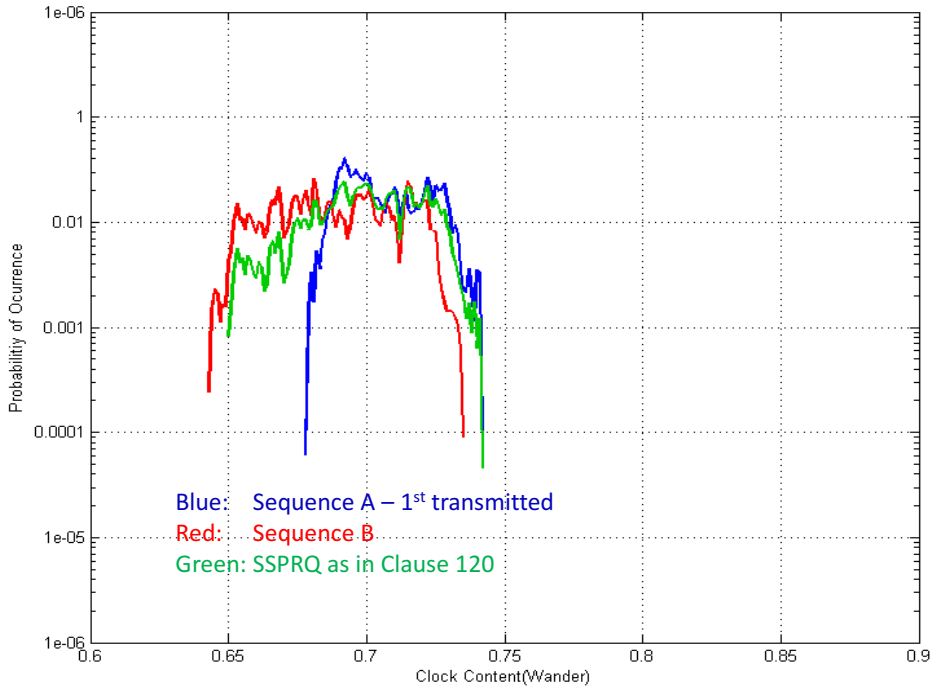


http://www.ieee802.org/3/bs/public/adhoc/logic/oct27_16/anslow_02a_1016_logic.pdf

Lets Look at SSPRQ Further

- **Looking at the SSPRQ TD time evolution for each of the 3 seeds and sequence A and B**
  - SSPRQ TD pattern exercises CDR over greater range than the reported clock content issue!





How to Protect Against Lower TD Data Pattern

- **CDR JTOL due to reduction in TD reduces CDR BW and can be protected in several ways:**
  - Reduce TX golden PLL corner frequency to ~2.88 MHz and keep the 4 MHz CDR BW to allow CDR implementation based on 25%, 50%, or 75% TD
  - Keep TX golden PLL corner frequency at 4 MHz and increase the CDR BW to ~5.56 MHz to allow CDR implementation based on 25%, 50%, or 75% TD
  - Test the DUT with a test pattern having variable TD forcing the CDR operate with nominal and low BW
- **The right approach without penalizing all transmitters or receivers is to test with a representative test pattern**
  - Given SSPRQ has the necessary property exercising the CDR linearly through the full range, expected to be more stressful and is our preferred solution
  - We have also created SSPRQ2 with two bell-shaped response, SSPRQ2 if anything it would be less stressful than SSPRQ because the CDR will toggle between two point
- **Existing SSPRQ can guard against potential CDR systematic weakness due to possible pathological clock content.**

Text Update to CL 124 in Support of Worst Case Clock Content (Preferred Option)

- **Add SSPRQ pattern 6 to the stress receiver sensitivity test - no other change!**

Table 124–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Table 124–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 400GBASE-R signal	124.8.2
Side mode suppression ratio	3, 5, 6 or valid 400GBASE-R signal	—
Average optical power	3, 5, 6 or valid 400GBASE-R signal	124.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	124.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	124.8.5
Extinction ratio	4 or 6	124.8.6
$RIN_{21.4}OMA$	Square wave	124.8.7
Stressed receiver conformance test signal calibration	6	124.8.9
Stressed receiver sensitivity	3 or 5 and 6*	124.8.9

* Pattern 6 is to test for CDR tracking.

Summary

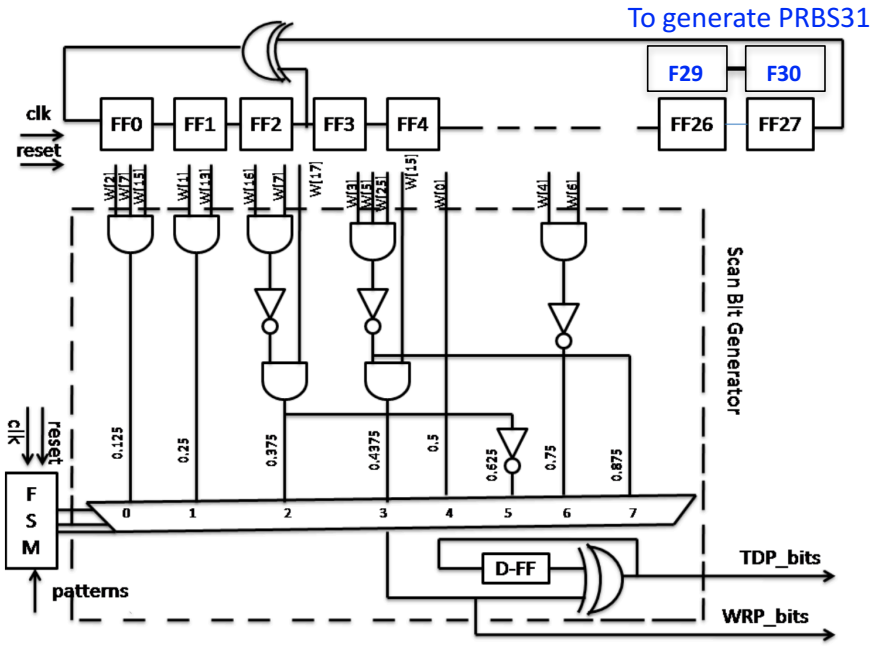
- **Worst case pathological clock content indicate:**
  - A CDR operating with all transition TD reduced by 9% - CDR BW drop by 9%
  - A CDR operating with all transitions through average not impacted – CDR BW not impacted
  - A CDR operating with only symmetrical transitions TD reduced by 28% - CDR BW dropped by 28%
- **Worst case clock content will reduce the nominal CDR BW but a well design CDR can tolerate reduction in CDR tracking BW**
- **Instead of testing all CDRs with higher JTOL corner a better approach is to test the CDR with a test pattern having similar or greater TD range**
- **The overall clock content impact on the CDR is minor with just 0.0167 UI for a CDR operating with symmetrical transitions through average and just 0.0021 UI for a CDR operating with all transitions**
  - The impact of TD is negligible but best practice is to test the CDR with worst case TD data pattern
- **With SSPRQ transition density range exceeds worst case clock content reported, then existing SSPRQ pattern can provide necessary test to protect against any CDR systematic weakness**
- **Given the CDR need to operate with SSPRQ test pattern the burden of additional test is negligible**
- **So we are in luck - no need to make substantive change to the draft or add new test pattern given how stressful a pattern is SSPRQ (SSPRQ2 included in the back up material but is not necessary)!**

Back up Material

How to Generate SSPRQ2

How to Generate Specific TD PRBS31 Pattern

- **Simple combinatory out of the LFSR can generate variable weighted random, *px*, pattern**
  - The LFSR28 implementation generates pattern with *px* from 0.125 to 0.875 with step of 0.125
  - The basic approach can be extended to PRBS31 by adding 3 additional shift registers
  - For example combining two non-adjacent LFSR outputs generate *p*=0.25
  - $TD = p_0p_1 + p_1p_0 = 2p_1(1-p_1)$
    - Where $p_0 = (1-p_1)$.



Weighted Random and Transition Density Patterns For Scan-BIST
Farhana Rashid and Vishwani Agrawal
http://www.eng.auburn.edu/~agrawvd/TALKS/NATW12/natw_Rashid.pdf

How to Generate Specific TD PRBS31 Pattern

- **Worst case transition density TD due to clock content reported is ~0.683 (-8.9%)**
  - P=0.328 can generate TD of 0.661 (-11.9%) slightly worse that worst case clock content
  - P=0.328 is created by ANDing two 0.625 outputs
  - SSPRQ2 is generated similar to SSPRQ see next page and accompanying word document.

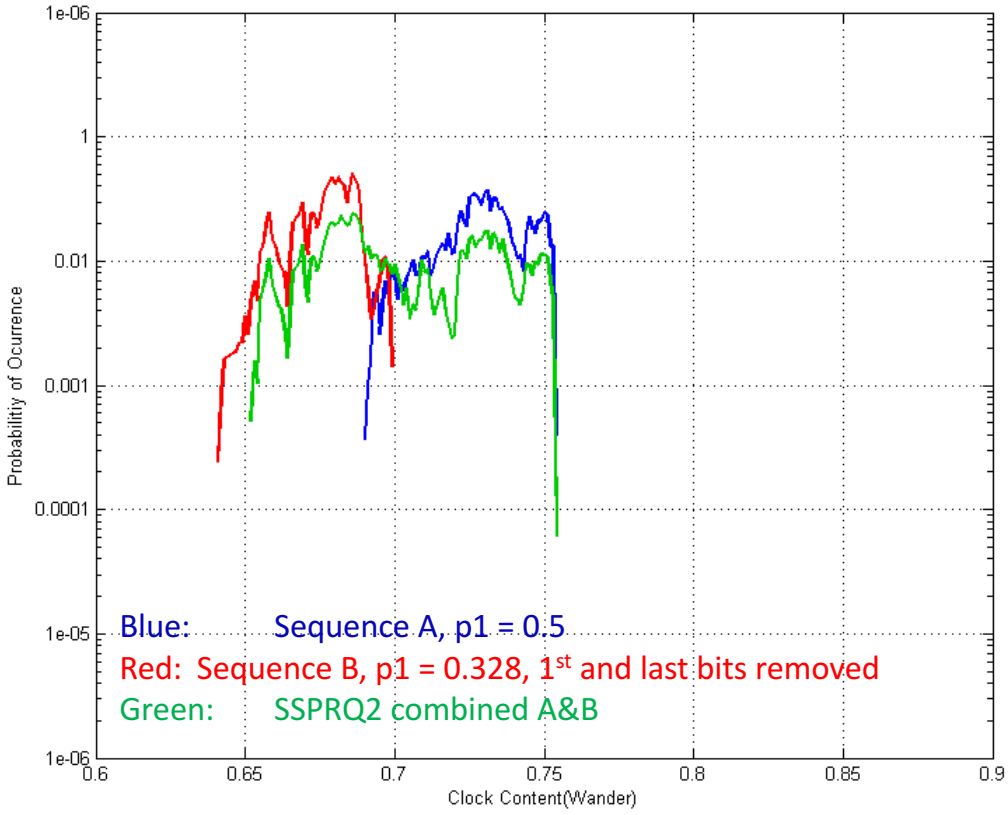
p	TD - NRZ	TD – PAM4
0.125	0.218	0.3281
0.25	0.375	0.5625
0.328	0.441	0.661
0.375	0.4688	0.703
0.4375	0.4922	0.738
0.5	0.5	0.75
0.625	0.4688	0.7031
0.75	0.375	0.5625
0.875	0.2188	0.3281

SSPRQ2 Clock Content

- **TD response for all transitions**
- **SSPRQ2 constructed as following**
  - Sequence A has three sections: A1, A2, A3
  - Sequence B has three sections: B1, B2, B3

Section	Seed	Length	WPRBS31 P1
A1	0x00000002	10924	0.5
A2	0x34013FF7	10922	0.5
A3	0x0CCCCCCC	10922	0.5
B1	0x00000002	10924	0.328
B2	0x34013FF7	10922	0.328
B3	0x0CCCCCCC	10922	0.328

- **The SSPRQ2 is then composed as:**
- **32768/2 PAM4 symbols of Sequence A**
- **32768/2 inverted PAM4 symbols of Sequence A.**
- **32768/2 PAM4 symbols of Sequence B**
- **32768/2 inverted PAM4 symbols of Sequence B.**



Text Update to CL 124 in Support of Worst Case Clock Content (Back up Option)

- **Add SSPRQ2 pattern 7 to the stress receiver sensitivity test – see backup and accompanying word document how to generate SSPRQ2.**

Table 124–9—Test patterns

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7	SSPRQ2	120.5.11.2.3

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