FEC Core Area Comparison and Model

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Overview

- Motivation
- Caveats
- Results
- Background
- Next Steps

Motivation

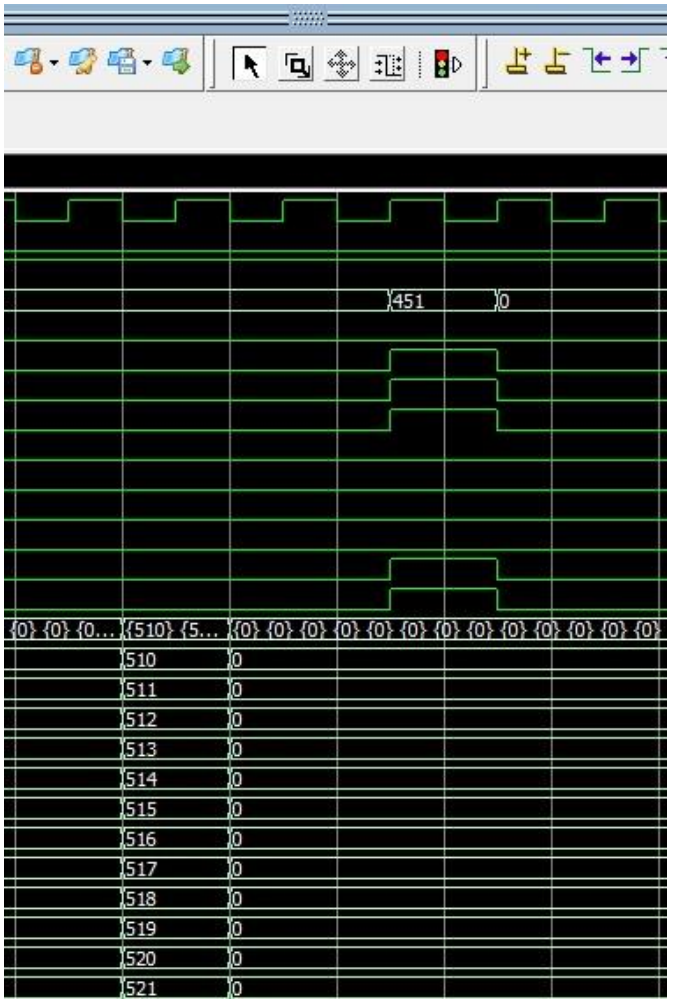
- **Reed Solomon used in 100GE, likely to find use in 400GE**
- **This presentation is to give confidence that we have not reached end point in direct implementation of Reed Solomon**
- **Show that published algorithms, current commercial devices are enough to deliver Reed Solomon for the forseeable future**
  - Multi-Tbps monolithic performance

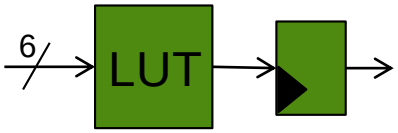
Caveats

- **This presentation does not suggest that Reed Solomon is the best FEC for future standards**
  - Only that it can scale to much higher speeds easily
- **Monolithic FEC may not be the best approach**
  - Monolithic FECs required for multi-Tbps aggregation
  - Alternate approach may distribute FECs across multiple links

Results - Encoder

- **KR4 RS (528,514,7)**
- **Logic only implementation**
  - FPGA 4LUT/6LUT independent
  - ASIC direct synthesis
- **Relatively area efficient**
  - 40K 6LUT
- **High performance**
  - 2.5 Tbps
    - 475MHz @ 5280 bits
  - Performance scaling possible
    - Area/performance tradeoff
    - Unlikely to be linear
- **Very low latency**
  - 3 clock cycles (6ns)





FPGA basic building block is 6 input look up table + register

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FPGA Technology Scaling

- **40nm FPGA – 2009 production**
  - 100K 6LUT (mid range) – 250K 6 LUT (high end)
  - 2.5 Tbps @ 40K 6LUT
    - Normalized 100 Gbps = 1.6K 6LUT
    - Normalized 400 Gbps = 6.4K 6LUT
- **28nm FPGA – 2012 production**
  - 200K 6LUT – 400K 6LUT
- **20nm FPGA – 2015 production**
  - 200K 6 LUT – 500K 6LUT
- **FinFET FPGA – 2017 production**
  - 500K 6LUT – 1M 6LUT

N.B. handwaving numbers – to show practicality of implementing future performance in currently available or planned devices

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Cauchy Matrix Based Encoding

- **Common Encoding:**
  - $\boldsymbol{p(x) + x^{(n-k)} m(x) = c(x)}$
  - $\boldsymbol{p(x)}$ is the reminder of the division of $\boldsymbol{x^{(n-k)} m(x)}$ by $\boldsymbol{g(x)}$
  - Finding $\boldsymbol{p(x)}$ requires a division circuit (very difficult to parallelize!)

- **Matrix based Encoding**
  - RS generator matrix has a Vandermond structure e.g $\mathbf{G} = \begin{bmatrix} \alpha^{254} & \alpha^{253} & \cdots & 1 \\ \alpha^{2.254} & \alpha^{2.253} & & \vdots \\ \vdots & \vdots & & \vdots \\ \alpha^{239.254} & \alpha^{239.253} & \cdots & 1 \end{bmatrix}$
  - It can be put in systematic form as: $\widetilde{\mathbf{G}} = \mathbf{V}^{-1}\mathbf{G} = [\mathbf{I} \quad \mathbf{P}]$
  - Encoding is performed by direct multiplication $\mathbf{c} = \mathbf{m}.\widetilde{\mathbf{G}}$

- **Seroussi encoder [1]**
  - Systematic generator matrix indices are: $p_{ij} = \frac{\alpha^{i-k-j} \prod(\alpha^{n-1-k-j} - \alpha^{n-1-t})}{\alpha^{n-i-1} + \alpha^{n-k-j-1} \prod_{t \neq i}(\alpha^{n-1-i} - \alpha^{n-1-t})}$
  - With a *relatively* simple recurrence relation between p_{ij} and p_{i+1j} leading to a possible systolic architecture

[1] G.Seroussi, IEEE Trans. on Inf. Theory, Vol.137, no.4,1991

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Next Steps

- Other encoder design examples (KP4)
- Multi-Tbps Decoder

Conclusions

- **Reed Solomon is scalable to multi-Tbps applications**
  - No new FPGA technology required
    - Next generation FPGA technology will be even faster, more cost effective
  - Will work in any technology (such as ASIC)
- **Effective – low area/performance ratio**
- **Low latency**

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Thank You