IEEE P802.3bs 400 Gb/s Ethernet Task Force Logic Ad Hoc

Teleconference October 23rd, 2015

Minutes taken by Mark Gustlin, Xilinx
The meeting started at 8:01 am Pacific chaired by Mark Gustlin, the attendee list was taken from the WebEx attendee list.

Documentation for the call can be found at the Ad Hoc web page:
http://www.ieee802.org/3/bs/public/adhoc/logic/index.shtml

Mark showed the patent link and asked if anyone had any questions, no one responded.

Presentation #1
Title: Toward convergence of FEC interleaving schemes for 400GE –Zhongfeng Wang
See: wangz_01_1015_logic.pdf

Presentation #2
Title: FEC codeword filling performance –Pete Anslow
See: anslow_01_1015_logic.pdf

Attendees (taken from webex, please let me know if you have a correction or addition):
Mark Gustlin, Xilinx
Paul Mooney, Spirent
Andre Szczepanek, Inphi
Eric Fortin, ALU
Jeff Slavick, Avago Technologies
Rick Rabinovich, Alcatel-Lucent
Jerry Pepper, Ixia
Tongtong Wang, Huawei
Derek Cassidy, BT
Eric Baden, Broadcom
Dan Lambalot, Bayside Design
Zhongfeng Wang, Broadcom
Peter Stassar, Huawei
Martin White, Cavium
Mike Dudek, Qlogic
Paul Reepschlager, Lumentum
B. Smith, Inphi
Tom Palkert, Xilinx, Luxtera,
Molex
David Malicoat, HP
John Ewen, Global Foundries
Bill Wilkie, Xilinx

Piers Dawe, Mellanox
Kenneth Jackson, Sumitomo
Pete Anslow, Ciena
Daniel Koehler, MorethanIP
Phil Sun, Marvell
Ali Ghiasi, Independent
Gary Nicholl, Cisco
Kapil Shrikhande, Dell
Xinyuan Wang, Huawei
Geoffrey Chacon, HP
Mark Gravel, HP
JC Calderon, Inphi