Clear Remaining Issues for 400GE FEC

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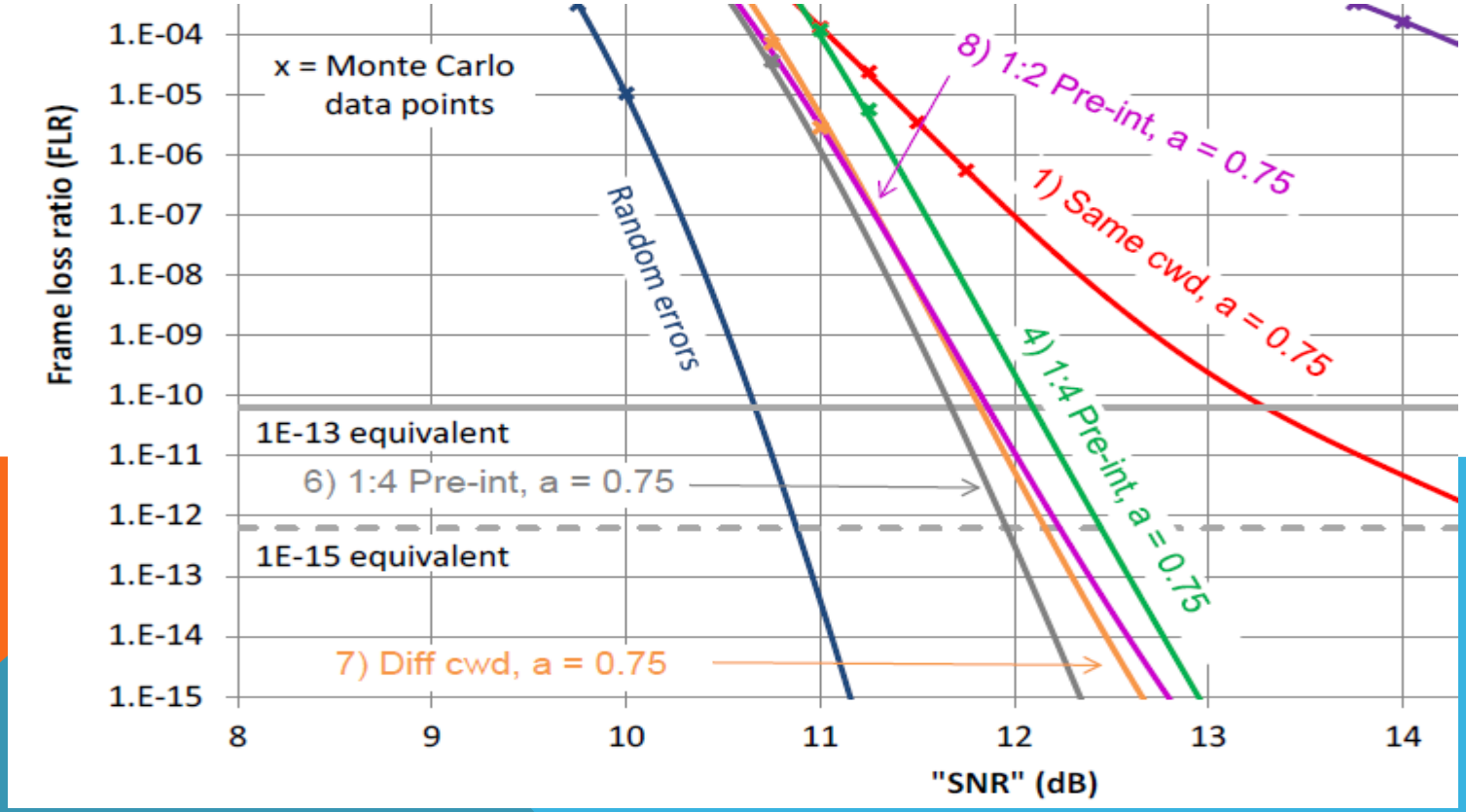
INTRODUCTION

- **Given 2-way interleaved RS coding scheme is accepted as 400GE FEC baseline.**
- **This presentation discuss some details of code-word interleaving.**

- **It can be found that differences between various interleaving options are small.**
- **However, without back compatibility concern in our case, we should pick the one that is better than all others.**

PACK RATE LOSS VS. SNR LOSS

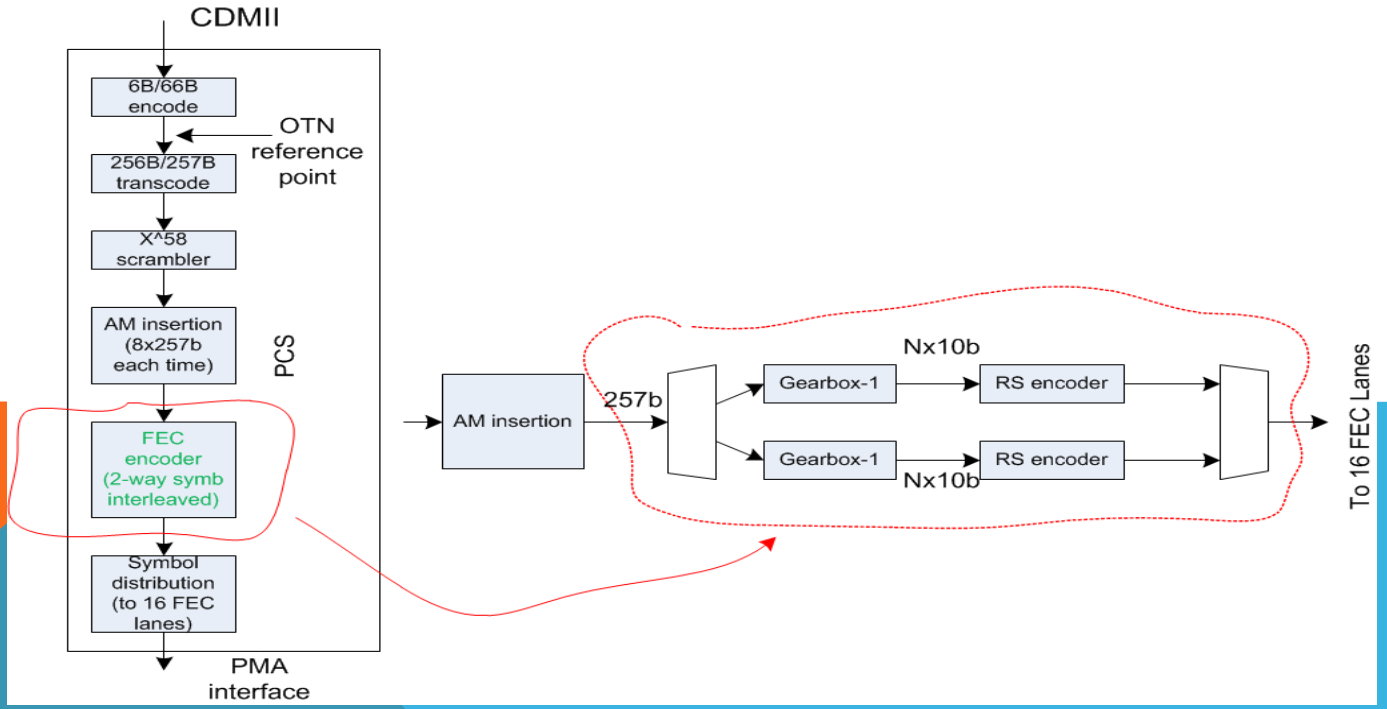
- **Comparing 2 sequential codewords vs. 2 interleaved codewords to be interleaved, the difference between Pack Rate Loss (PRL) is less than 2x:**
  - One Ethernet packet may cover 2 RS codes
  - Error correlation may lead to both RS codes un-decodable
- **From following figure, 1.7x PRL ~= 0.05dB SNR loss**
- **Interleaving 2 sequential codewords is not a good tradeoff due to increased latency and complexity.**



CASE-I: INTERLEAVING WITH 257B GRANULARITY

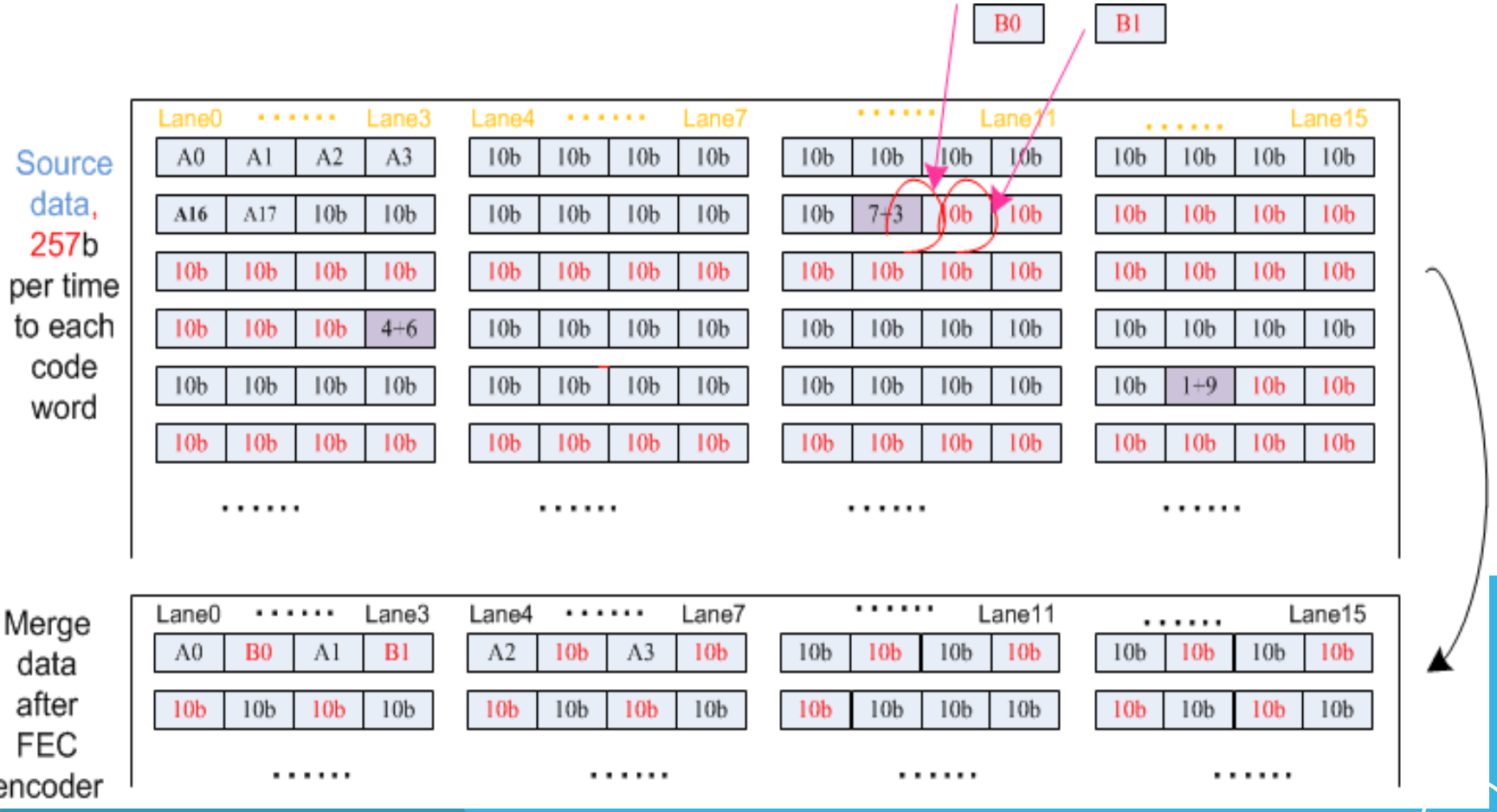
- Spec description: the output of AM insertion module will be distributed to 2 RS code words 257 bits per time and the encoded data from 2 code words will be sent out in the check board fashion with 10b granularity. The 8x257b AM data patterns is the pre-permuted form of that shown in gustin_xxx_yy.pdf on page zz. It is also shown …..

- Analyses: pre-permuted AM patterns are really random, hard to remember, easy to cause RTL coding error. Input data (payload) order is changed.



CASE-I: 257B GRANULARITY (CONT'D)

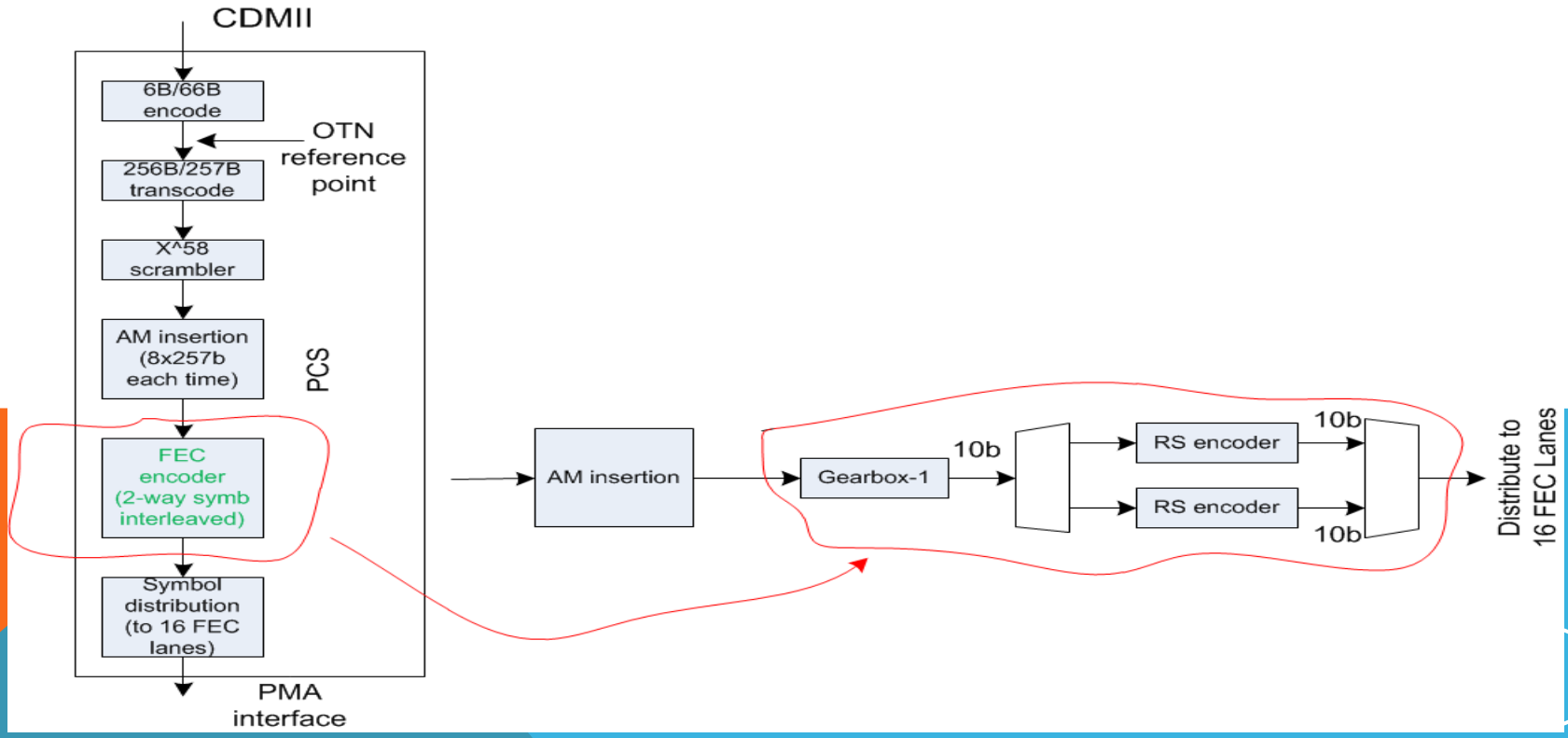
- Source data are permuted at output of Tx.
- AM data patterns need pre-permuted.



CASE-II: INTERLEAVING WITH 10B GRANULARITY

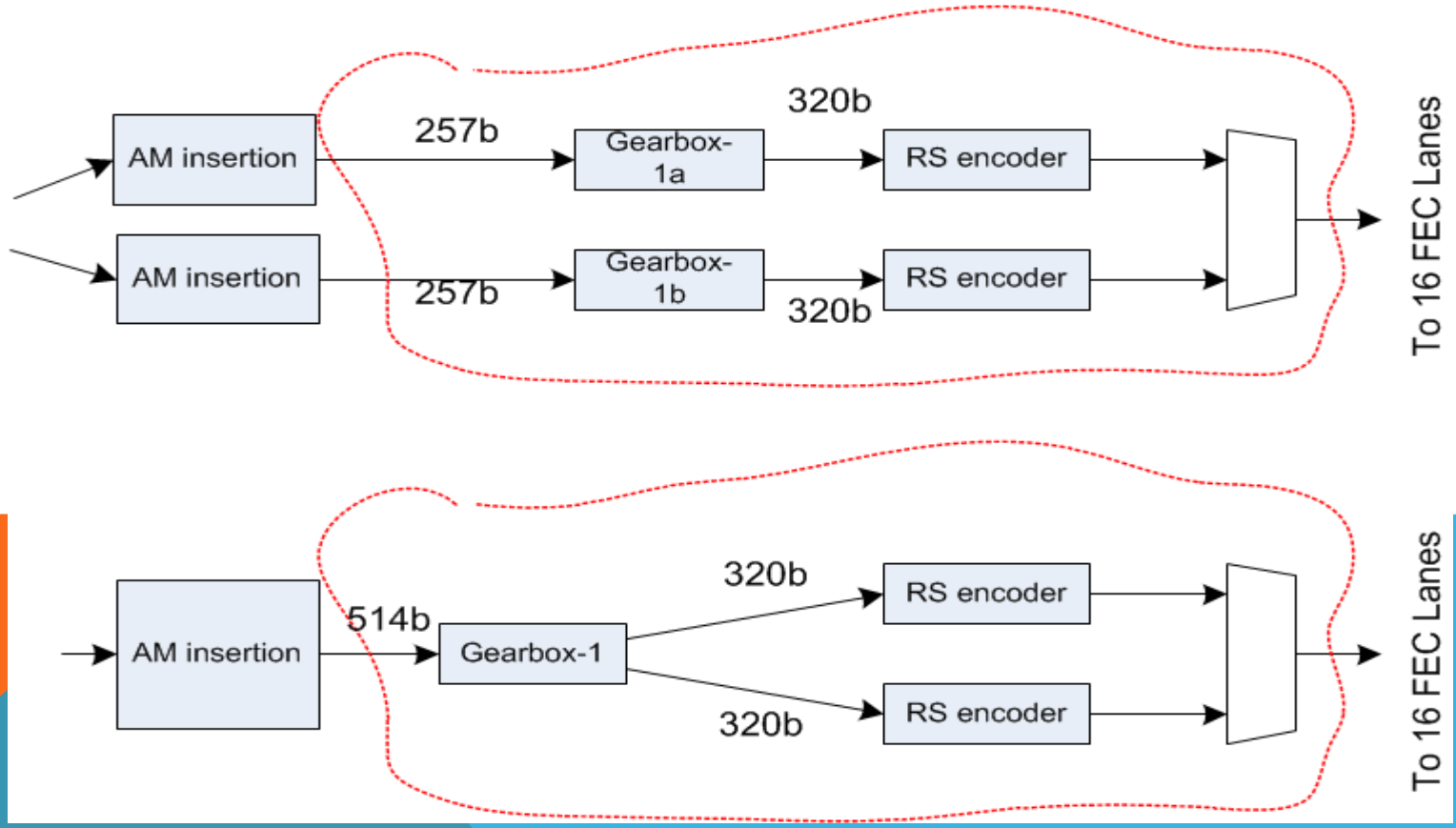
- Spec description: the output of AM insertion module will be distributed to 2 RS code words in the check board fashion and the encoded data will be sent out in the same interleaved fashion. The 8x257b AM data patterns is shown in gustin_xxx_yy.pdf on page zz.

- Advantages: simple AM patterns, simple spec description, input data order are maintained, no need to change current data flow (left figure). Low complexity.



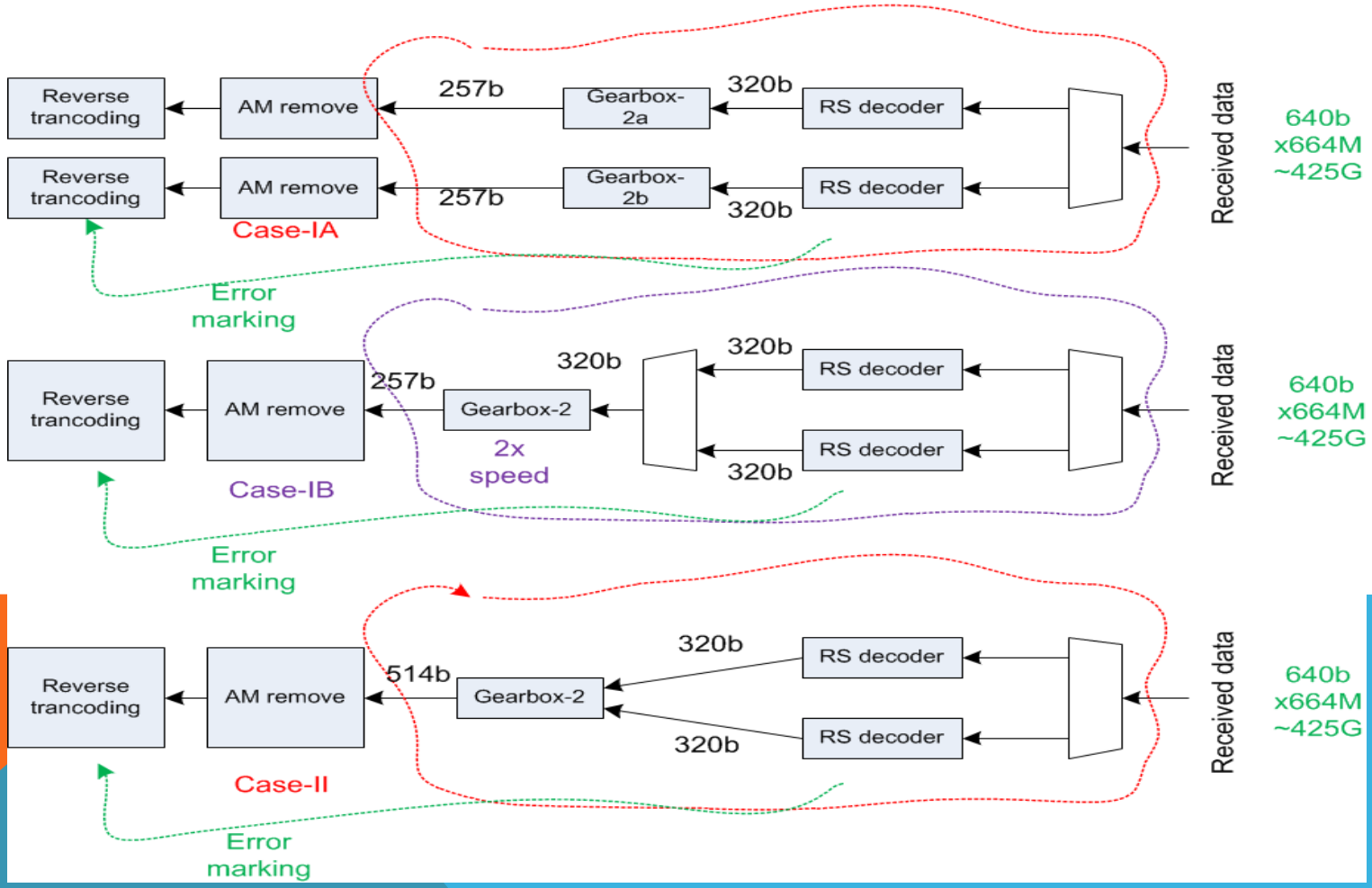
CLOSER VIEW AT 257B VS 10B INTERLEAVING

- Following figure shows a typical HW implementation for 2 different cases.
- The gearbox repetition period is 20 in case-I (2 gearboxes of 257b to 320b) while it is 10 in case-II (1 gearbox to convert 514b to 640b). Thus it is less complex in case-II.



ERROR MARKING IN DIFFERENT CASES

- Following figures show Rx Signal Flow for different cases. They didn't specify any specific HW implementation.



COMPARE 257B INTERLEAVING WITH 10B INTERLEAVING

1) Same system performance
2) Output data is out of order, not too bad, is that good?
3) AM patterns need pre-permuted, cause unnecessary RTL coding and verification issues –- even if it is a small problem
4) Error marking: same process after RS decoding
5) Slightly larger complexity in gearbox
6) Slightly more complex spec description

FINAL REMARK

- From previous detailed analyses, we can conclude that 10b interleaving is the best solution (there's no tradeoff, slightly better is better) among all possible options EVEN if the other options are also feasible.
- The above conclusion didn't consider multi-mode (e.g., 40G, 100G, 400G, et al) implementation in one chip.