IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Logic Ad Hoc

Teleconference October 27th, 2016

Minutes taken by Mark Gustlin, Xilinx
The meeting started at 8:02 am Pacific chaired by Mark Gustlin, the attendee list was taken from the WebEx attendee list.

Documentation for the call can be found at the Ad Hoc web page:
http://www.ieee802.org/3/bs/public/adhoc/logic/index.shtml

Mark showed the patent link and asked if anyone had any questions, no one responded.

Presentation #1
200GbE alignment marker characteristics - Pete Anslow, Ciena

Presentation #2
SSPR generation - Pete Anslow, Ciena

Presentation #3
Autocorrelation of PRBS13Q – Yasuo Hidaka, Fujitsu

Attendees (taken from webex, please let me know if you have a correction or addition):

Mark Gustlin, Xilinx
Yasuo Hidaka, Fujitsu
Tom McDermott, Fujitsu
Pete Anslow, Ciena
Ryan Wong, Broadcom
Paul Mooney, Spirent
David Malicoat, HPE
Flavio Marques, Furukawa
Ben Jones, Xilinx
Gary Nicholl, Cisco
Mark Kimber, Semtech
Adrian Butter, Global Foundries
Rick Rabinovich, Ixia
Slobodan Milijevic, Microsemi
Mike Dudek, Cavium
Phil Sun, Credo Semiconductor
John Dillard, Microsemi
Matt Brown, Applied Micro
Raymond Nering, Cisco
Kumaran Krishnasamy, Broadcom

James Fife, Etopus
Oded Wertheim, Mellanox
Mike Li, Intel
Steve Gorshe, Microsemi
Rick Pimpinella, Panduit
Hong Lim, Cisco
Martin White, Cavium