Updated Considerations on 400Gb/s Ethernet SMF PMDs

Peter Stassar

SMF Ad Hoc, 30 September 2014

HUAWEI TECHNOLOGIES CO., LTD.

HUAWEI

Contents

Introduction

- Over past 400GE Study Group and P802.3bs meetings a lot of material has been presented (considerations, simulations and test results)

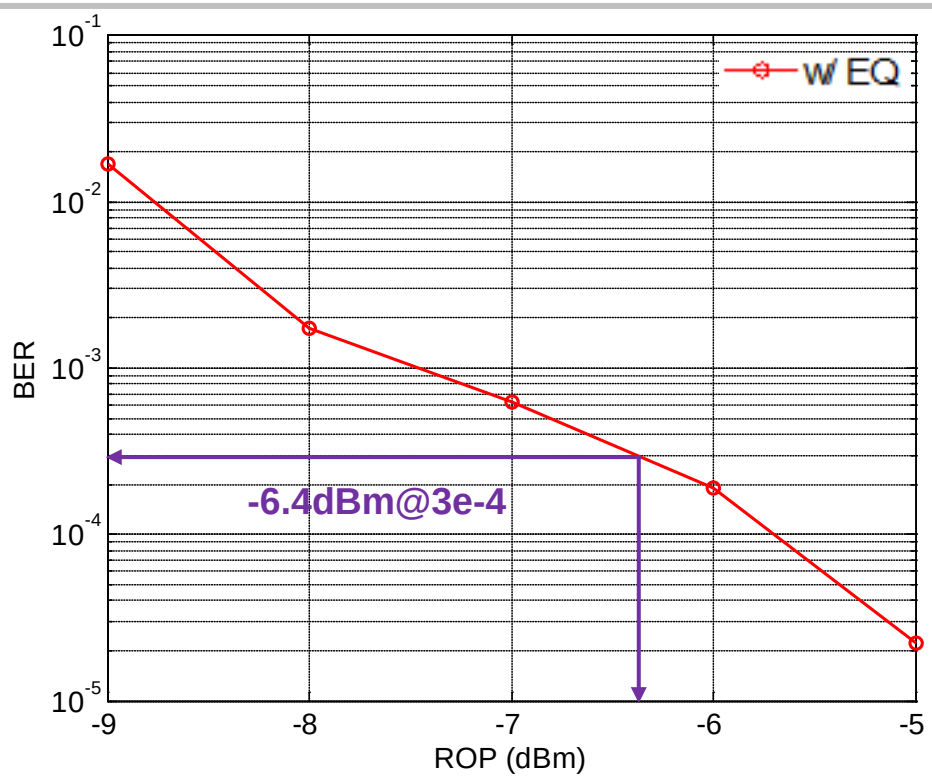
- Many people have expressed their preference for 100G serial solutions at the Ottawa meeting in September, but many others stated that 50G serial solutions would be a more robust approach

- What can we learn from this material?

- What additional material will be necessary?

Recap of “stassar_3bs_01_0714”, San Diego, July 2014

“Updated Considerations on a 4x112Gb/s PAM4 Configuration for the 2km SMF PMD”



Average power
After demux
PRBS 2^{15}-1
KP4 FEC

- An ROP (average) of -6.4dBm @ 3e-4 (after demux) has been achieved with equalization.
- In stassar_3bs_01_0714 a mux/demux loss of 1.5 dB (each) was assumed, however following Cole’s suggestion of 2 dB loss, PAM4 modulation penalty of 5 dB and perfect extinction ratio, this measured value translates in OMA(01-00) sensitivity of -6.4dBm @ 3e-4 (demux input)

Possible loss budgets (Black & White analysis) from stassar_3bs_01_0714

	HW test	Manufacturing specification 1	Manufacturing specification 2	Unit
Tx OMA (01-00) min Tested	-0.8	–	–	dBm
Tx OMA (01-00) min Specification Value	–	-1	-6	dBm
TDP	1	1	1	dB
Tx OMA (01-00) – TDP min	-1.8	-2	-7	dBm
Channel insertion loss Specification Value	–	4	4	dB
Rx ROP OMA (01-00) with KP4 FEC Specification Value	–	-6	-11	dBm
Rx ROP OMA (01-00) with KP4 FEC Tested	-6.7	-6.9	-12	dBm
Available channel loss	**4.9**	–	–	dB

Remarks on previous Slide 5

- It was the intent of “stassar_3bs_01_0714”, that actually neither of the two draft manufacturing specifications are realistic.
- During Ottawa meeting it appeared that many had interpreted these as realistic proposals
- Therefore in this presentation we propose one realistic budget, based upon following assumptions:
  - Mux & Demux loss of 2 dB (each), PAM4 modulation Penalty of 5 dB and perfect extinction ratio.
  - “Realistic” Tx average power of -1.5 dBm (before mux, according to Cole), leading to OMA (01-00) min of -5.5 dBm (after mux)
  - Realistic Receiver sensitivity in OMA (01-00) max of -6 dBm (before demux), which is close to tested value of -6.4 dBm (@ PRBS 2^{15}-1)

Realistic loss budget (Black & White analysis) for 4x100G PAM4 configuration

	Realistic specification for 2km duplex SMF	Realistic specification for 500m PSM4 SMF	Unit
Tx OMA (01-00) min Specification Value	-5.5	-3.5	dBm
TDP	1	1	dB
Tx OMA (01-00) – TDP min	-6.5	-4.5	dBm
Wanted channel insertion loss, specification Value	4	4	dB
Rx ROP OMA (01-00) with KP4 FEC Specification Value	-6	-8	dBm
Available channel loss	-0.5	3.5	dB

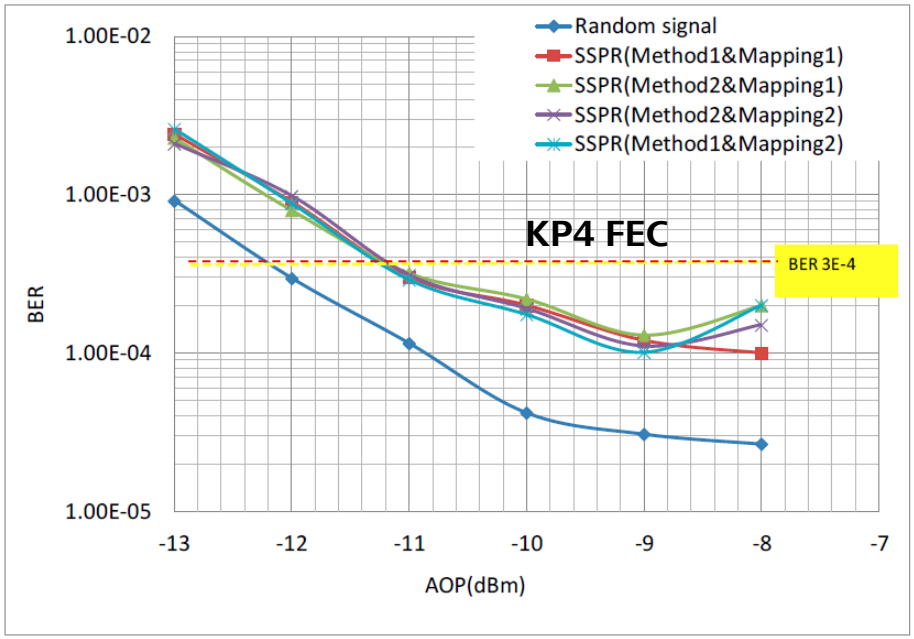
For 2km duplex SMF the "gap" in this budget seems too big to be bridged. If reconfirmed then 4x100G PAM4 may only be useable for 500m PSM4.

Is PAM4 a showstopper?

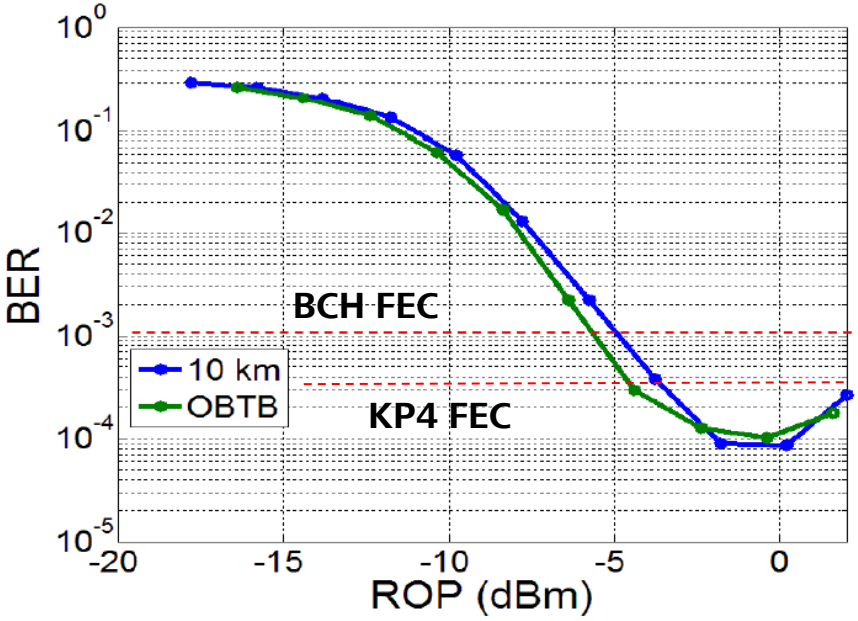
- **During both San Diego (July 2014) and Ottawa (September 2014) many presentations with test results showing BER curves have been given:**
  - *8*50G PAM4:*
    - xu_3bs_01_0714, San Diego, July 2014
  - *8*50G NRZ:*
    - wen_3bs_01_0914, Ottawa, September 2014
  - *4*100G PAM4:*
    - way_3bs_01a_0914, Ottawa, September 2014
    - hirai_3bs_01_0914
    - mazzini_3bs_01_0914
  - *4*100G DMT:*
    - Many presentations (not addressed in this presentation)

Is PAM4 a showstopper? continued

The common denominator of ***ALL*** PAM4 BER curves is a BER-floor in the range of 10^{-4} to 10^{-6}, even when many presentations are performed for a too short PRBS 2^{15}-1.



xu_3bs_01_0714

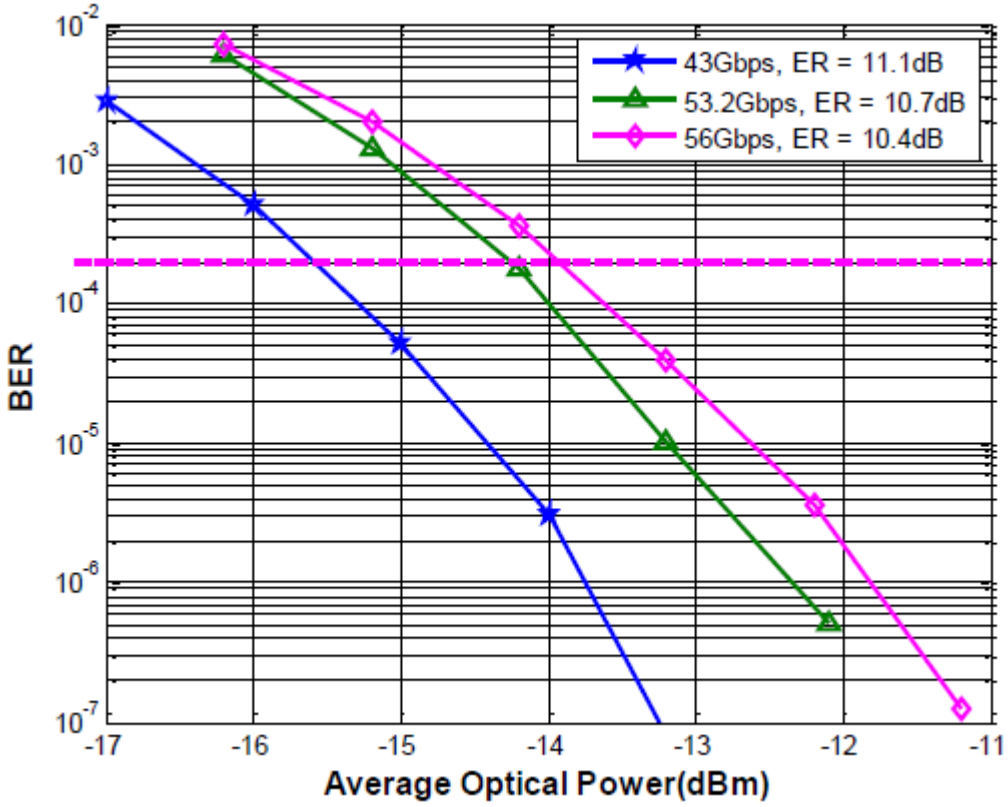


way_3bs_01a_0914

A BER floor that close to the FEC operation point, even under “ideal” laboratory conditions, will certainly lead to unstable performance in the field under practical field conditions

Is PAM4 a showstopper? Continued 2

The BER curves shown in wen_3bs_01_0914 were “nice” waterfall curves with no sign of a BER floor close to the operation point, as we would want to see. Slide 8 of wen_3bs_01_0914 says PRBS31.



PRBS31

wen_3bs_01_0914

Is PAM4 a showstopper? Continued 3

- Can we now conclude that PAM4 is not usable?
- *NO!!!*
- BUT……, it will be critical to identify the reason for these BER-floors and, when identified, show experimental results where the BER-floor is sufficiently below the operation point.
- Questions:
  - Redo both NRZ and PAM4 experiments for SSPR pattern (PRBS 2^{15}-1 is too short) in b2b configuration (to exclude dispersion effects)
  - Is there a difference between 25Gb/s, 50Gb/s and 100Gb/s PAM4?
- Preliminary assessment of PAM4 at Huawei:
  - It seems that the SNR at the receiver is NOT the limiting factor
  - It may be pure ISI from the Tx eye, which cannot be addressed by TDP

Some literature references

- [1] Fotini Karinou, Roberto Rodes, Kamau Prince, Ioannis Roudas and Idelfonso Tafur Monroy, "*IM/DD vs. 4-PAM Using a 1550-nm VCSEL over Short-Range SMF/MMF Links for Optical Interconnects*", OW4A.2 OFC/NFOEC 2013:
  - Even in this experiment @10Gb/s a BER-floor is present for PAM4 and not for NRZ. This may be caused by using a VCSEL as a transmitter.
- [2] Krzysztof Szczerba, PetterWestbergh, Johan Gustavsson, Asa Haglund, Johnny Karout, Magnus Karlsson, Peter Andrekson, Erik Agrell and Anders Larsson, "*30 Gbps 4-PAM transmission over 200m of MMF using an 850 nm VCSEL*", ECOC2011:
  - In this experiment (using PRBS7!) no error floor is seen even for operation on OM3 MMF.

Suggestions for follow-up

- Agree on a common test environment with SSPR pattern
- Agree on working assumptions for mux & demux loss as proposed by Chris Cole:
  - 1 dB for 1:2, 2 dB for 1:4 and 3 dB for 1:8 mux/demux (each)
- Identify a working assumption for reasonable transmitter output power
- Identify a maximum level for a BER-floor under SSPR pattern testing
- Do we agree that we shouldn't want to see a BER floor in our experiments?
- What is a reasonable FEC (coding gain versus complexity and power consumption) to be used? KP4? Noting that with BCH FEC there may be issues with power/hardware complexity/latency in the client interface.
- Can we sufficiently minimize ISI with PAM4 transmitters or will it require exotic technology?
- What can we gain with FEC, FFE and DSP technologies? And can we afford it?

Q & A

Thank you