# **SMF PMD Modulation Observations**

400 Gb/s Ethernet Task Force SMF Ad Hoc Conference Call 24 February 2015 Chris Cole



### Shannon-Hartley Theorem

- $C = B \log_2 (1 + S/N)$ 
  - $C \triangleq Channel capacity$
  - $B \triangleq Bandwidth$
  - $S \triangleq Signal Power$
  - $N \triangleq Noise Power$

Guidance to increase C:

- If B limited, increase S/N to support higher order modulation (HOM)
- If S/N limited, increase B to support higher Baud rate

# Cu & SMF Client Channel Comparison

#### Data points 0 SMF 2km link insertion loss (electrical) -10 Loss [dB] -20 -30 Cu chip-to-chip max insertion loss -40 5 10 15 25 20 30 0 Frequency (B) [GHz]

#### Observations

- Cu channel is bandwidth (B) limited
- SMF client channel is not bandwidth (B) limited

# Cu & SMF Client Optics TRX S/N Comparison

- Data points
  - Cu SerDes S/N (BTB) = ~50dB (no FEC)
  - SMF DML TX, PIN RX client optics S/N (BTB) = ~16dB (electrical, no FEC)
- Observations
  - Cu TRX is not S/N limited
  - SMF client optics TRX is S/N limited

#### **Results Summary**

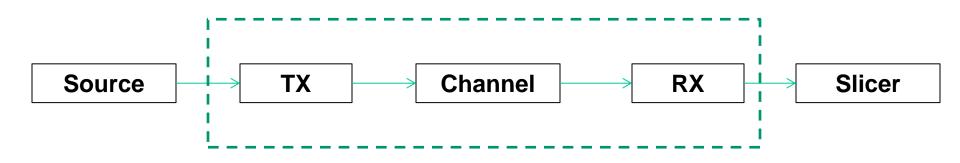
- To increase C:
  - If B limited, increase S/N to support higher order modulation (HOM)
  - If S/N limited, increase B to support higher Baud rate
- Observations:

	Channel	Limitation		Modulation
		Channel B	TRX S/N	Guidance
	Cu	Yes	No	НОМ
	SMF Client	No	Yes	NRZ
24 February 2015 5			Finisa	

# Fiber Bandwidth Limited Channel Examples

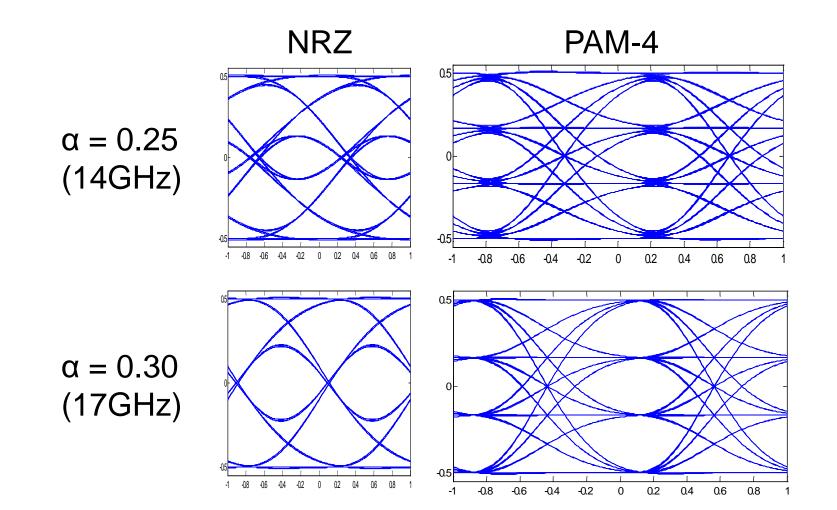
- SMF DWDM Transport
  - B = 50GHz
  - 100G/λ modulation: DP-QPSK
- MMF client
  - B = ~2GHz/km (OM3)
  - B (100m) = ~20GHz
  - ~2x for OM4
  - Very different from SMF client channel
  - 50G/λ modulation: PAM-4 is a good candidate (although NRZ has been demonstrated)
- Common modulation format across all channel types at 50G and higher per lane bit rate is not optimal

#### Ideal SMF Client System Model



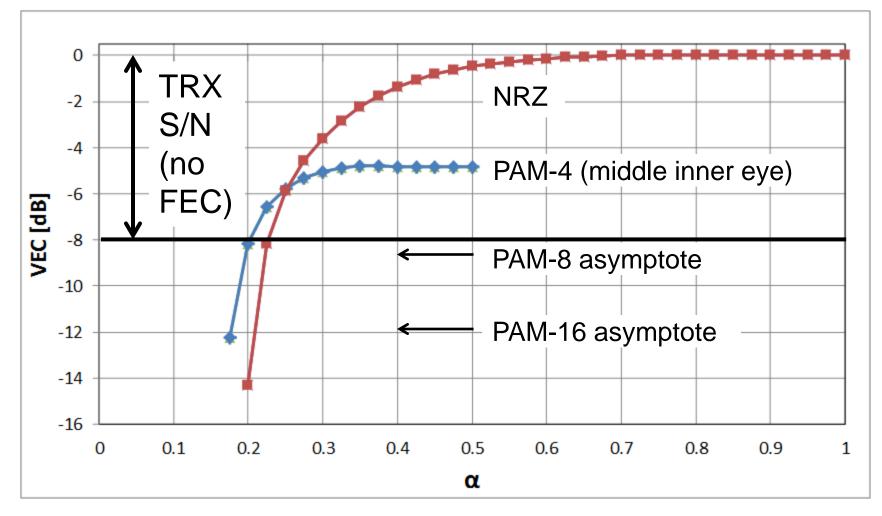
- SMF Client channel assumed ideal
- TX \* Channel \* RX modelled as 4<sup>th</sup> order BT filter
- $B = \alpha$  bit-rate
- Ex. bit rate = 56G
  - $\alpha = 0.25 \rightarrow B = 14GHz$
  - $\alpha = 0.30 \rightarrow B = 17GHz$

#### Slicer Input Eyes of Ideal SMF Client System



24 February 2015

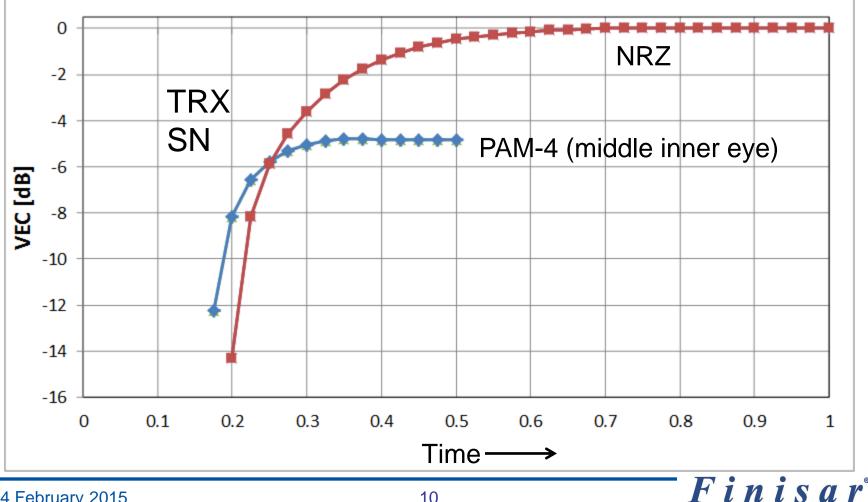
#### Vertical Eye Closure at Slicer Input



Noise penalty offsets VEC by ~1dB depending on B<sub>NRZ</sub>/B<sub>PAM-4</sub> Finisar

# VEC & Component Bandwidth

VEC improves with component bandwidth which improves over time, so Time can equivalently be the x-axis variable



### Component Bandwidth Observations

- "Serial wins over time" example statements:
  - "The general consensus (including CWDM advocates) is that serial will be cost effective in long term." (p.14) Matt Traverso, et. al, "40GbE 10km SMF Objective: Serial", IEEE 802.3ba Task Force, July 14-17, 2008
  - "All optical technologies have matured (are maturing) over time to the lowest size, cost, power" (p.2)
    Gary Nicholl, "100Gb/s Single Lambda Optics –Why ?", OIDA 100GbE per Lambda for Data Center Workshop, June 12-13 2014
- "Serial wins over time" is equivalent to stating that component bandwidth increases over time
- All of the arguments and evidence, including SMF PMD examples used in support of "Serial wins over time", apply equally to: "NRZ wins over time"

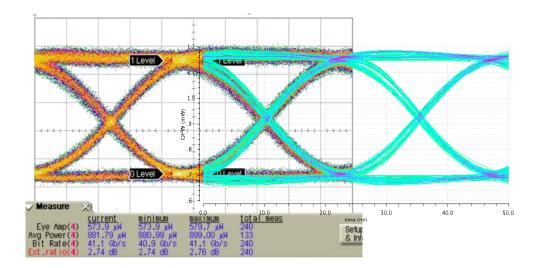
# Component Bandwidth Timing Questions

- Example component bandwidth timing question:
  - "The discussion is not if 100Gb/s single lambda is compelling but when ... is it technically feasible ?" (p.4) Gary Nicholl, "100Gb/s Single Lambda Optics –Why ?", OIDA 100GbE per Lambda for Data Center Workshop, June 12-13 2014
- 50G/λ SMF Q&A
  - Q: When is 50Gb/s single lambda NRZ technically and economically feasible?
  - A: Now; see following pages (Although it was not in 2000 and 2008)
- 100G/λ SMF Q&A
  - Q: When is 100Gb/s single lambda NRZ technically and economically feasible?

Finisar

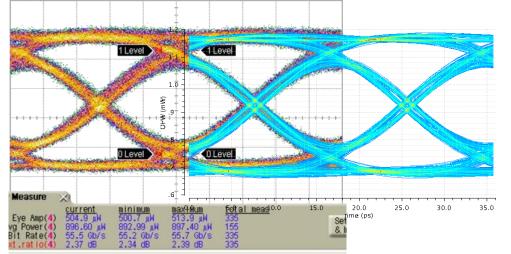
• A: Not now, but likely >2020

# 50G NRZ SiP PIC TX Data Example



40Gb/s, PRBS9 TX optical eye diagram at π/2 bias:

- Measurement data,
- Simulation



56Gb/s, PRBS9 TX optical eye diagram at  $\pi/2$  bias:

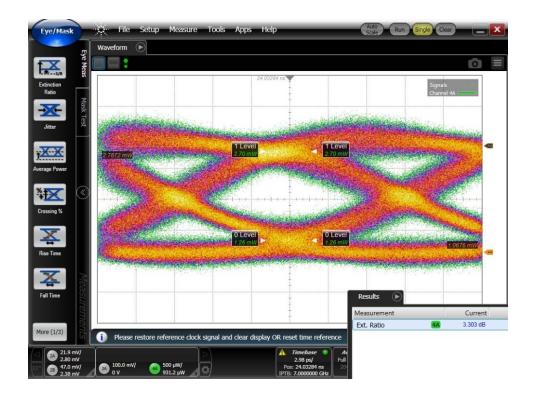
Measurement data,

Finisar

Simulation

Finisar 2x50G hybrid SiP PIC fabricated at ST Microelectronics

24 February 2015



56Gb/s, PRBS15 TX, 65mA bias, 50°C Finisar DML chip

Finisar

- Detailed results submitted for publication as OFC-2015 post-deadline paper
- 50G NRZ EML data presented by K. Kojima, et. al.

24 February 2015

### Discussion

- For SMF client interfaces, NRZ is the preferred choice unless it's not feasible
- Over time, NRZ optics margins improve and cost drops
- HOM, like PAM-4, permanently locks in S/N penalty which never goes away, even as components improve
- Multiple factors not in this presentation include:
  - Dispersion Penalty
  - MPI
  - other
- Data to be presented includes:
  - TX power
  - RX sens.
  - TDP, including Dispersion
  - other

#### SMF PMD Modulation Observations

# Thank you

