802.3bs: Proposal for PAM4 PMDs link budgets harmonization

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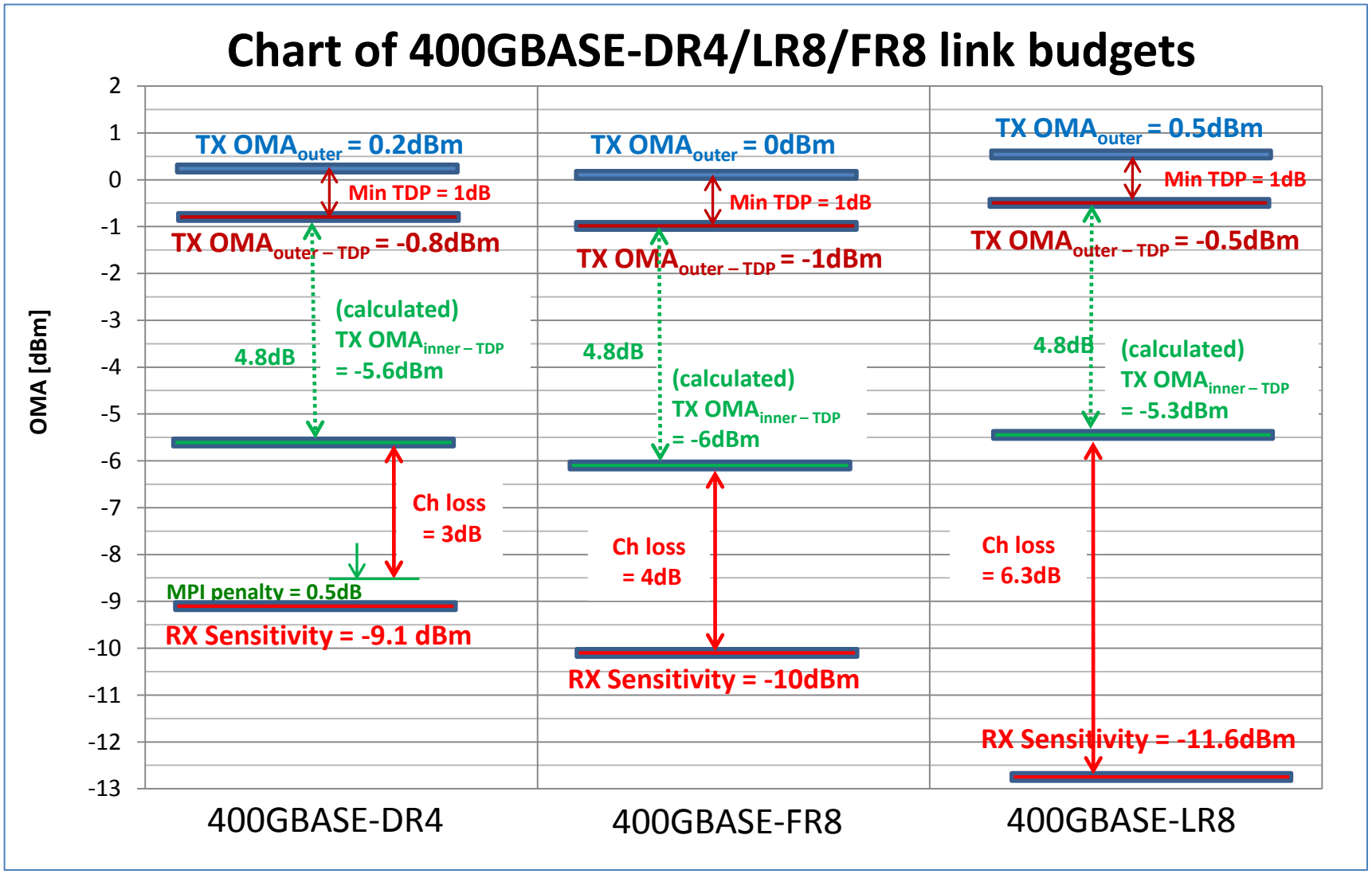
Background

Following last plenary presentation, this contribution propose an harmonization over the three SMF (PAM4) PMD types (400GBASE-FR8/LR8 and 400GBASE-DR4) trying to:

- Define same assumptions on link power budget and penalties.

- Re-cap latest discussions and contributions about MPI.
  - Open discussion about target TX/RX reflectance and connectors RL.
  - Propose MPI penalty to be considered.

PAM4 PMDs: snapshot of (Draft 1.1) 400GBASE-DR4/LR8/FR8 budgets.



PAM4 PMDs: transmit/link characteristics

Table 122–6—400GBASE-DR4 transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Lane wavelength (range)	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	dB
Average launch power, each lane (max)	4	dBm
Average launch power, each lane[a] (min)	–1.9	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	0.2	dBm
Launch power in OMA_{outer} minus TDP, each lane (min)	–0.8	dBm
Transmitter and dispersion penalty (TDP), each lane (max)	2.5	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio, each lane (min)	5	dB
$RIN_{xx}OMA$ (max)	–142	dB/Hz
Optical return loss tolerance (max)	TBD	dB
Transmitter reflectance[c] (max)	–20	dB
Transmitter eye mask definition	TBD	

[a]Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDP < 1 dB, the OMA_{outer} (min) and OMA_{inner}(min) must exceed these values.
[c]Transmitter reflectance is defined looking into the transmitter.

Table 122–8—400GBASE-DR4 illustrative link power budget

Parameter	Value	Unit
Power budget (for max TDP)	6	dB
Operating distance	500	m
Channel insertion loss[a]	3	dB
Maximum discrete reflectance	–35	dB
Allocation for penalties[b] (for max TDP)	3	dB
Additional insertion loss allowed	0	dB

[a]The channel insertion loss is calculated using the maximum distance specified in Table 122–5 and cabled optical fiber attenuation of 0.5 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 122.11.2.1.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

Table 123–7—400GBASE-FR8 and 400GBASE-LR8 transmit characteristics

Description	400GBASE-FR8	400GBASE-LR8	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		—
Lane wavelengths (range)	1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Total average launch power (max)	13.2		dBm
Average launch power, each lane (max)	4.2		dBm
Average launch power, each lane[a] (min)	–3	–2.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	5.5	5.7	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	0	0.5	dBm
Difference in launch power between any two lanes (OMA_{outer}) (max)	TBD	TBD	dB
Launch power in OMA_{outer} minus TDP, each lane (min)	–1	–0.5	dBm
Transmitter and dispersion penalty (TDP), each lane (max)	2.2	2.4	dB
Average launch power of OFF transmitter, each lane (max)	–30		dBm
Extinction ratio (min)	4.5		dB
$RIN_{xx}OMA$ (max)	TBD		dB/Hz
Optical return loss tolerance (max)	TBD		dB
Transmitter reflectance[c] (max)	TBD		dB
Transmitter eye mask definition	TBD		

[a]Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDP < 1 dB, the OMA_{outer} (min) must exceed this value.
[c]Transmitter reflectance is defined looking into the transmitter.

Table 123–9—400GBASE-FR8 and 400GBASE-LR8 illustrative link power budgets

Parameter	400GBASE-FR8	400GBASE-LR8	Unit
Power budget (for maximum TDP)	6.2	8.7	dB
Operating distance	2	10	km
Channel insertion loss	4[a]	6.3	dB
Maximum discrete reflectance	TBD	TBD	dB
Allocation for penalties[b] (for maximum TDP)	2.2	2.4	dB
Additional insertion loss allowed,	0	0	dB

[a]The channel insertion loss is calculated using TBD plus an allocation for connection and splice loss given in 123.11.2.1.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

An additional 0.5dB MPI penalty, on top of max TDP of 2.5dB is considered into 400GBASE-DR4 link (see welch_3bs_01a_0715), while MPI penalty is part of TDP in the 400GBASE-FR8/LR8 budgets (cole_3bs_01a_071, slide 8). Consequently penalties are not aligned, as well as power budget calculation.

PAM4 PMDs: receiver characteristics

Table 122–7—400GBASE-DR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Lane wavelengths (range)	1304.5 to 1317.5	nm
Damage threshold[a], each lane (min)	6.5	dBm
Average receive power, each lane (max)	4	dBm
Average receive power, each lane[b] (min)	–4.9	dBm
Receive power, each lane (OMA_{outer}) (max)	4.2	dBm
Receiver reflectance (max)	–26	dB
Receiver sensitivity (OMA_{inner}), each lane[c] (max)	–9.1	dBm
Stressed receiver sensitivity (OMA_{inner}), each lane[d] (max)	TBD	dBm
Conditions of stressed receiver sensitivity test:		
Condition 1[e]	TBD	
Condition 2[e]	TBD	

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA_{inner}), each lane (max) is informative.
[d]Measured with conformance test signal at TP3 (see 122.8.10) for the BER specified in 122.1.1.
[e]Condition 1 and condition 2 are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Was -9.25dBm into Draft 1.0

Table 123–8—400GBASE-FR8 and 400GBASE-LR8 receive characteristics

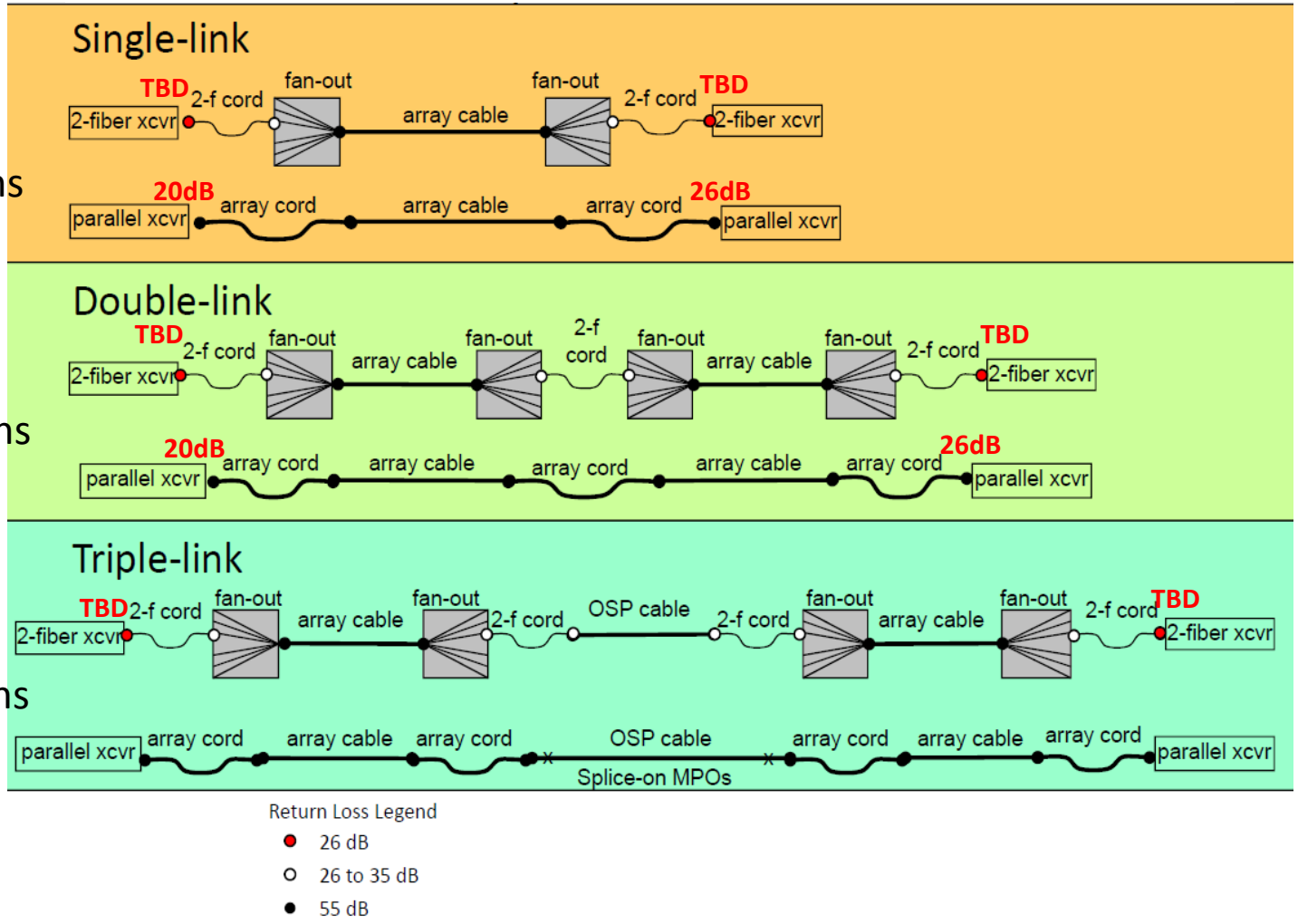
Description	400GBASE-FR8	400GBASE-LR8	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		—
Lane wavelengths (range)	1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19		nm
Damage threshold[a], each lane	5.2		dBm
Average receive power, each lane (max)	4.2		dBm
Average receive power, each lane[b] (min)	–7	–8.8	dBm
Receive power, each lane (OMA_{outer}) (max)	5.7		dBm
Difference in receive power between any two lanes (OMA_{outer}) (max)	TBD	TBD	dB
Receiver reflectance (max)	TBD		dB
Receiver sensitivity (OMA_{inner}), each lane[c] (max)	–9.8	–11.6	dBm
Stressed receiver sensitivity (OMA_{inner}), each lane[d] (max)	TBD	TBD	dBm
Conditions of stressed receiver sensitivity test			
Condition 1[e]	TBD	TBD	
Condition 2[e]	TBD	TBD	

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA_{inner}), each lane (max) is informative.
[d]Measured with conformance test signal at TP3 (see 123.8.10) for the BER specified in 123.1.1.
[e]Condition 1 and condition 2 are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

400GBASE-DR4 Min TDP (1dB, was 0.8dB) and margin reduction (0dB, was 0.15dB) resulted in a further increase on TX OMA outer (was 0dBm) and RX sensititivity (was -9.25 dBm).
Opposite direction w/respect our intent to reduce TX OMA (traverso_3bs_01a_1115), neither there was agreement to relax sensititivity.

MPI penalty – common channel implemetation and hypothesis

Reference SM channel from Paul Kolesar, December 2014.



Four connections — FR8/LR8, DR4

Six connections — FR8/LR8, DR4

Eight connections — LR8, n/a

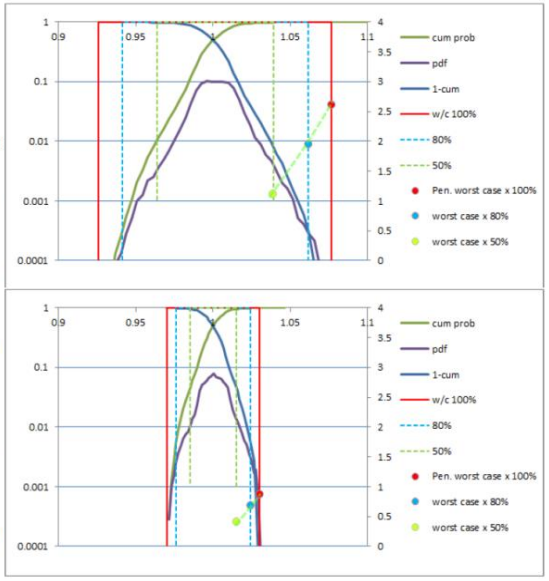
400GBASE-DR4 links should be implemented with 8° Angle Polish MTP connectors: ≥55dB return loss. Current 400GBASE-DR4 TX reflectance should be really improved from 20dB, considering what is achievable from different implementation technologies perspectives.

MPI penalty – latest contributions

1.8dB penalty (ref. **J.King, Dec 2014**) w/probability 99.9%

MPI-PAM4

- Monte Carlo spreadsheet model
- Six 26 dB RL connections (top)
  - At 0.1% probability, the MPI penalty is ~1.8dB, (equivalent to the penalty associated with ~70% of the worst case coherent sum of all the double reflected fields)
- Four 26 dB RL connections (bottom)
  - At 0.1% probability, the MPI penalty is ~0.9dB, (equivalent to the penalty associated with ~100% of the worst case coherent sum of all the double reflected fields)
- 0.1% ~ 9 hours/year

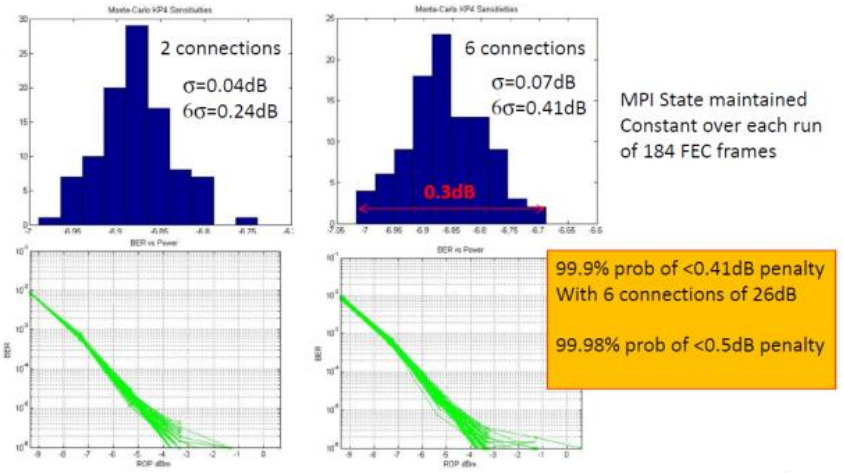


(ref. **A.Tipper, Dec 2014**)

6 connections: **0.41dB penalty** w/probability 99.9%

2 connections: **0.24dB penalty** w/probability 99.9%

(100 runs / simulation, 26dB reflectors)



MPI State maintained Constant over each run of 184 FEC frames

99.9% prob of <0.41dB penalty With 6 connections of 26dB

99.98% prob of <0.5dB penalty

Deterministic upper bound assumptions (see bhatt_01_0512):
- fiber attenuaton and connector losses are 0
- all interfering optical signals are perfectly aligned in polarization.

Statistical upper bound assumption (see farhood_01_1112):
- takes into account the fact that MPI impact varies as a function of received symbol power
- takes into account statistical distribution of the interfering signals

Reference: bhatt 31-Oct-2014 and further analysis run yesterday.

MPI Penalty Estimates	Tx Reflectance, dB	Rx Reflectance, dB	Connector Discrete Reflectance each, dB (4 connections)	MPI Penalty, dB, Deterministic Upper Bound	MPI Penalty, dB, Statistical Upper Bound
Case A	**26**	**26**	**26**	**1.95**	**1.42**
Case B	20	20	26	4.28	2.85
Case C	**26**	**26**	**35**	**0.51**	**0.39**
Case D	35	35	35	0.20	0.16
Case E	**26**	**26**	**55**	**0.14**	**0.11**
Case F	26	26	45	0.21	0.16
Case G	**20**	**26**	**55**	**0.26**	**0.20**
Case H	20	26	45	0.37	0.28

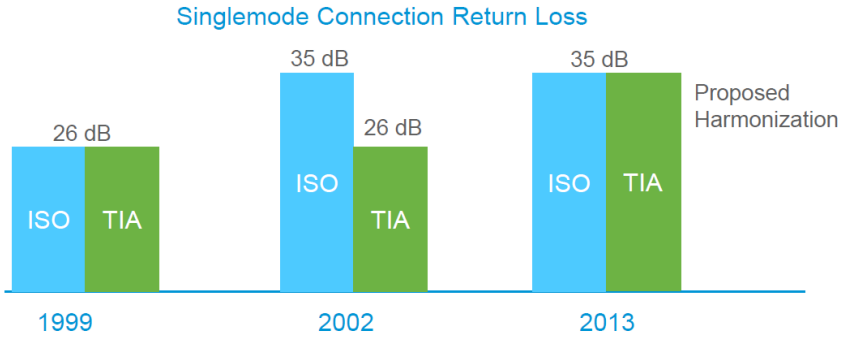
Double link cases (six connections)

- To stay safe, we propose to consider deterministic upper bound analysis for MPI.
- Triple-link analysis, applicable to LR8, has to be run.

MPI penalty – further works and proposal.

Singlemode Connection RL: Prevailing Standards

- In IEEE optical link specs, we can choose an appropriate value of connection return loss. For optical cable and connectors, we generally point to prevailing major international standards.
- The two relevant standards bodies are TIA-568 (for USA) and ISO/IEC 11801 (for all countries). They are largely equivalent, but this presentation points out one spec on which harmonization has become necessary:



A.4.3 Return loss

Test procedure: TIA-455-107 or TIA-455-8

Sample size: 24 devices (i.e., pairs of mated connectors)

Details:

- Deviations: none
- Requirement: 20 dB minimum for multimode fiber, 35 dB minimum for single-mode fiber, 55 dB minimum for single-mode broadband analog video (CATV) applications.

Can 400GBASE-FR8/LR8 already refer to normalized connector's return loss (see bhatt_400_01a_0713 and Liason letter to TIA Subcommittee) ?

TIA TR-42.11, is processing the 6th ballot of ANSI/TIA-568.3-D which contains the revised return loss specification for SM connections of >= 35 dB. Will follow publication approval at the upcoming meeting (end January 2016).

Assuming 35 dB return loss for LC and 55dB for MPO connectors, 26 dB reflectance for Rx and Tx would give a manageable worst case MPI penalty to take into account:

400GBASE-DR4 ≈ 0.15 dB

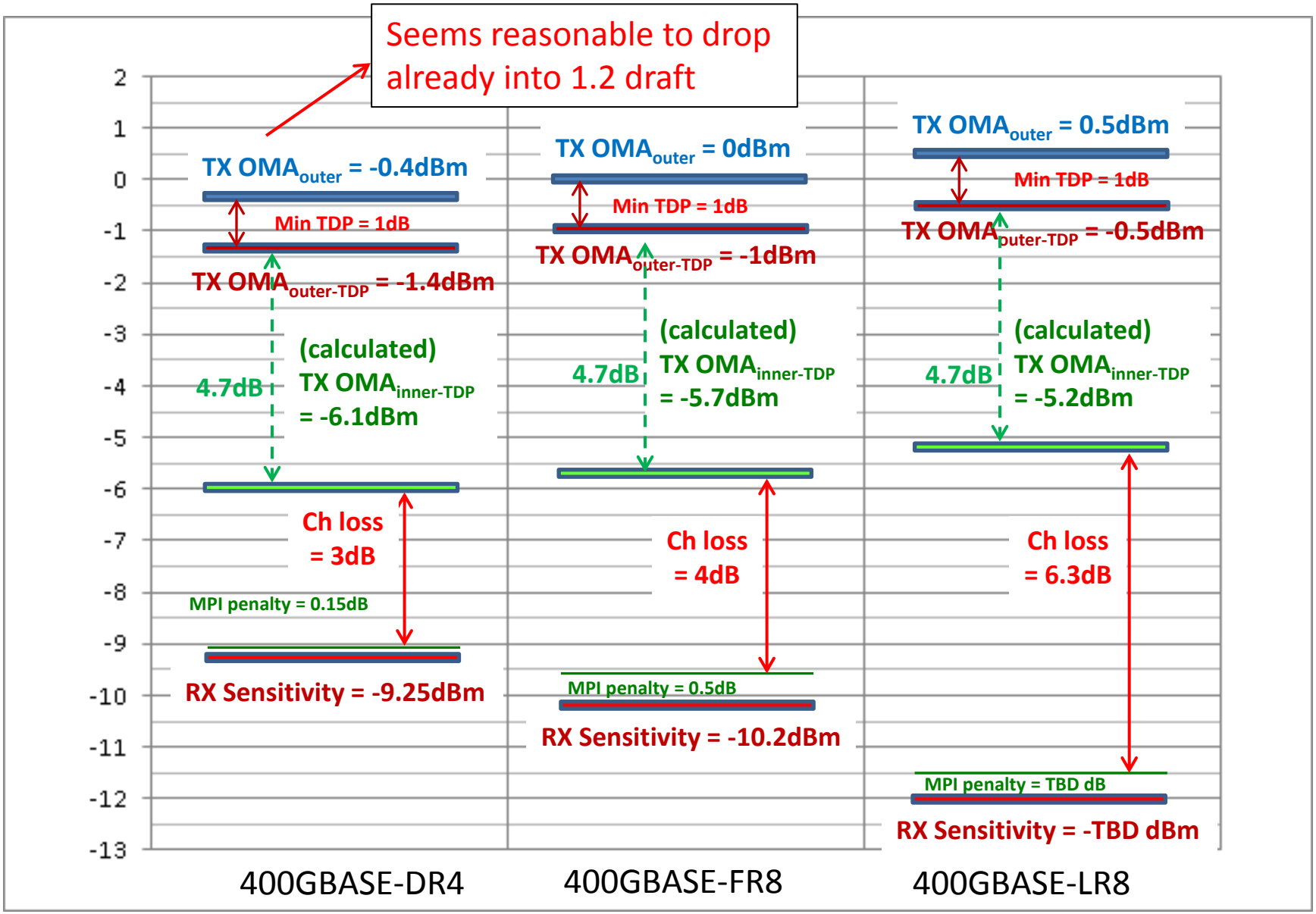
400GBASE-FR8 ≈ 0.5 dB

400GBASE-LR8 ≈ TBD dB

List of proposed steps for PAM4 link budget harmonization.

1. MPI should be included into the power budget as done for 400GBASE-DR4 already.
2. Achievable TX/RX reflectances need to be defined across all PMDs (proposed same 26dB value) to evaluate MPI into details.
3. Considering 35dB RL for duplex LC connector's return loss and 26dB TX/RX reflectance -> bring maximum deterministic MPI to be 0.5 dB for the 400GBASE-FR8 (LR8 need to be analyzed for triple link case).
4. Consider 55dB for MPO APC connector -> proposed max 0.15 dB for 400GBASE-DR4.
5. Assume 4.7dB PAM4 implementation penalty (already proposed by J.King on December 1st ad-hoc call).
6. Go back to Draft 1.0 RX sensitivity for 400GBASE-DR4 (-9.25dBm).

Potential PAM4 budgets...

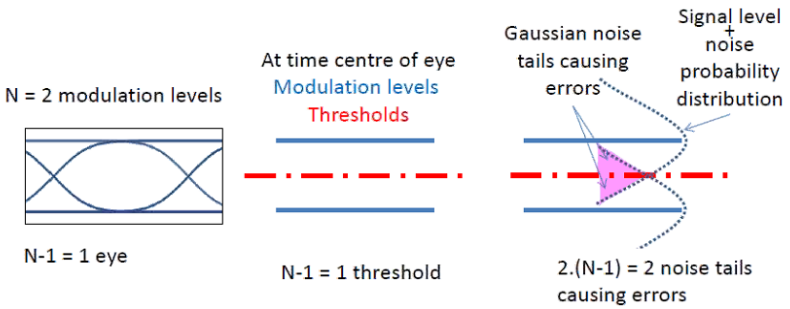


Assuming to include MPI penalty into the link budget.

THANK YOU

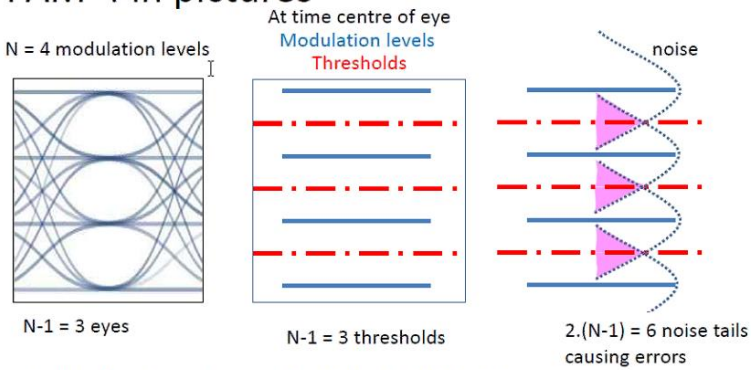
Back-up

PAM-2 in pictures



- Probability of occurrence of each level = 1/N = 1/2
- Relative probability of error per symbol = 2.(N-1)/N = 1
- The error probability associated with a *single* noise tail on a particular signal level = $P_i.½.\mathrm{erfc}((OMA/2)/(\sigma_n.\sqrt{2})$
  - where P_i is the probability of occurrence of the i^{th} signal level and σ_n is the RMS of the Gaussian noise
  - Note: the symbol error ratio equals the bit error ratio for PAM-2

PAM-4 in pictures



- Probability of occurrence of each level = 1/N = 1/4
- Relative probability of errors per symbol = 2.(N-1)/N = 3/2
  - *The symbol error ratio increases !*
  - For Gray coded PAM-4, 1 symbol error produces 1 bit error; but each symbol translates to $\log_2(N) = 2$ bits, so the ratio of SER (symbol error ratio) to BER is: $SER/BER = \log_2(N) = 2$
- Relative probability of errors per bit = $2.(N-1)/(N.\log_2(N)) = 3/4$
  - *The bit error ratio decreases !*

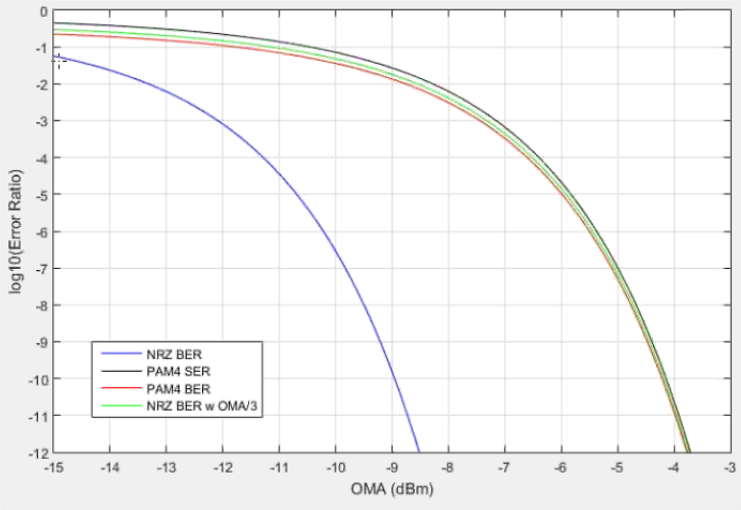
BER to power penalty

For a target BER of 2.4×10^{-4}:

- For ideal NRZ, the Q required is 3.492
- For ideal PAM-4, the Q required is 3.414
  - a negative Q penalty of ~0.098 dB
  - total modulation penalty for PAM-4 is 4.678 dB

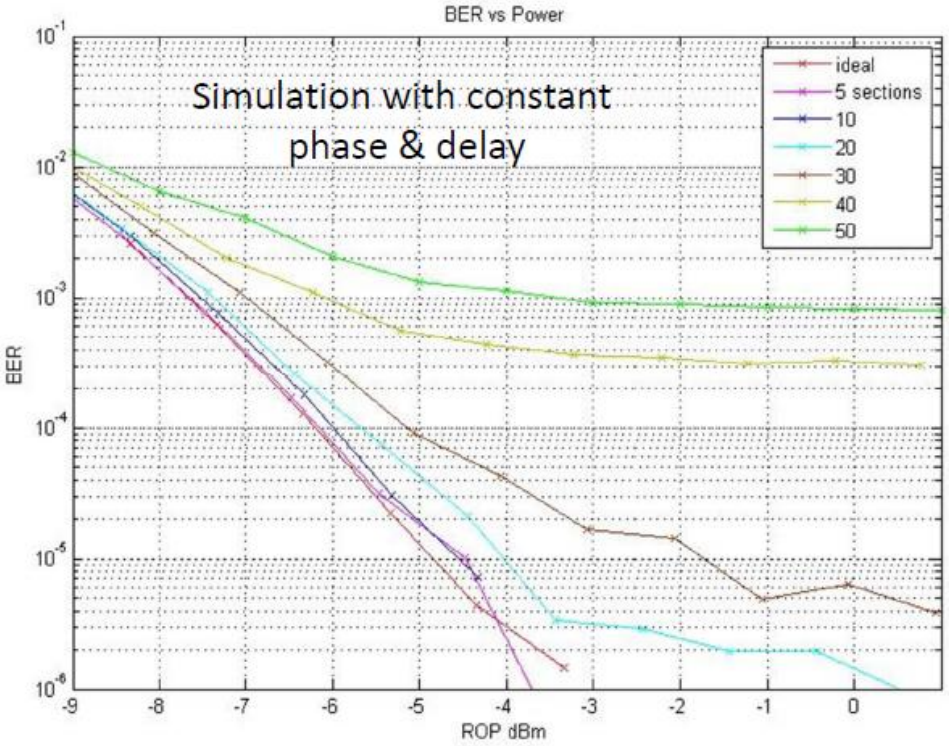
    (including impact of OMA scaling, higher symbol error rate, lower bit error rate, for a given outer eye OMA and fixed receiver noise, at BER of 2.4×10^{-4})

Simulation showing BER vs OMA for ideal Tx



ref. A.Tipper, Dec 2014

Why are the results so different from analytical upper bound models of MPI?



Upper bound methods assume MPI to be the only penalty and it is treated as a power penalty in a high Q environment.

With FEC we are already operating at Low SNR and MPI should be viewed as an additional correlated noise source generating noise floors (see plot) rather than power penalties i.e it is a Q penalty

Low Q operation results in much lower MPI Penalties than non FEC high Q cases

Coherent MPI: 26dB Reflectors, all reflection phases = $\pi/2$ rads. All path delays = 10 symbols