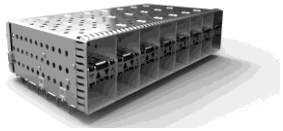

Channel Models for 50Gbps Chip to Module Analysis

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06/18/2014

50G Chip to Module Development

- TE has contributed two chip to module channel models to the OIF for analysis as part of the 56G VSR project. We are providing the same channel models to the IEEE for analysis and feedback as 50G channel development occurs across the industry.
- Due to the importance of the IEEE's 802.3bs project, We are contributing two S-parameter models for use by IEEE attendees.
- Channel models:
  - "Next generation 28Gb/s high density SMT IO"
  - "Next generation 28Gb/s press-fit stacked IO"
- These channels include module connector *concepts* that are being evaluated for 28Gb/s applications. These are NOT existing connectors and they have been designed for *28Gb/s* applications. This is a good time for feedback.

Connector Concepts

- “Next generation 28Gb/s high density SMT IO” is a connector concept that achieves density by placing contacts on a pitch less than 0.6mm
  - The connector interfaces to the host PCB via surface mount attachment
- “Next generation 28Gb/s press-fit stacked IO” is a connector concept that has contact density at 0.6mm
  - The connector is a “stacked” dual port solution and interfaces to the host PCB via press-fit attachment methodology
- Both connector concepts use PCB card edge interfaces as the mating interface

Channel 1

Next Generation 28Gbps High Density SMT IO

Host PCB

- 2.86mm thick, 23 Layers(12 GND planes)
- 2 Layer route out (Layer 10,12)
- Nelco 4000-13SI Material (Dk=3.32, Loss Tangent=0.010)
- 8mil stub on signal vias
- 7.3 dB stripline trace loss added

Module PCB details

- 1mm thick, 6 layer PCB (4 GND Planes)
- Microstrip trace route-out from 0.35x1.4mm mating pads
- Nelco 4000-13SI Material (Dk=3.32, Loss Tangent=0.010)
- 1.2 dB microstrip trace loss added

Data contributed as a Touchstone .s24p file as well as split .s4ps for the THRU and FEXT aggressors used in Power Sum Crosstalk calculations on slide 8.

Channel 2

Next Generation 28Gbps Pressfit Stacked IO

Host PCB

- 3.425mm thick, 26 Layers (15 GND Planes)
- 4 Layer route-out (Layers 7, 11, 17, 21)
- EM-888 Material (Dk=3.8, Loss Tangent=0.012)
- 8mil stub on signal vias
- 7.3 dB stripline trace loss added

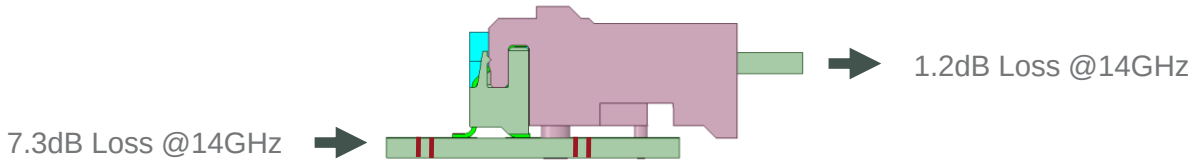
Module PCB details

- 1mm thick, 6 layer PCB (4 GND Planes)
- Microstrip trace route-out from 0.35x1.4mm mating pads
- Nelco 4000-13SI Material (Dk=3.32, Loss Tangent=0.010)
- 1.2 dB microstrip trace loss added

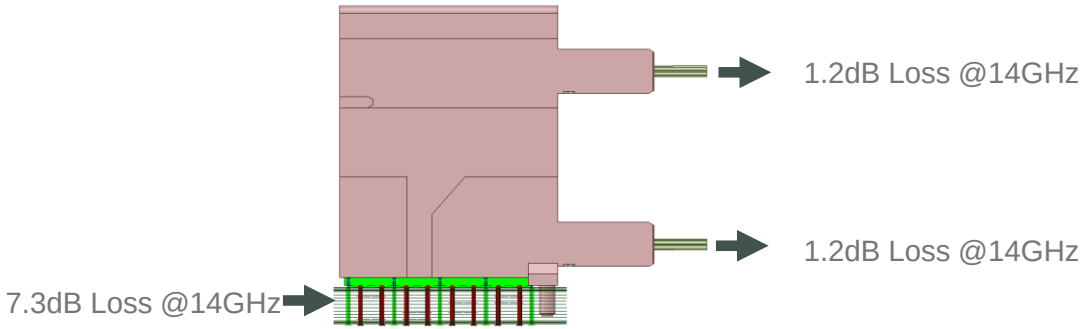
Data contributed as a Touchstone .s48p file as well as split .s4ps for the THRU and FEXT aggressors used in Power Sum Crosstalk calculations on slide 10.

Visual Representation

“Next generation 28Gb/s high density SMT IO”:

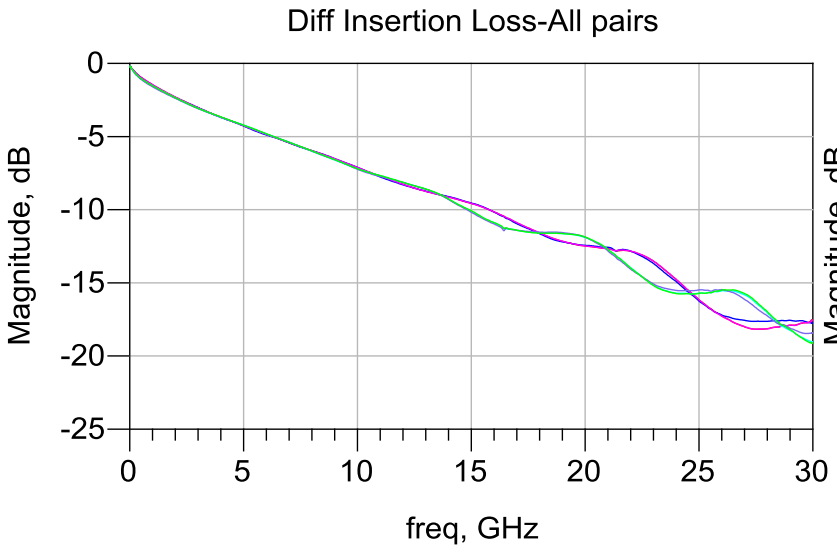


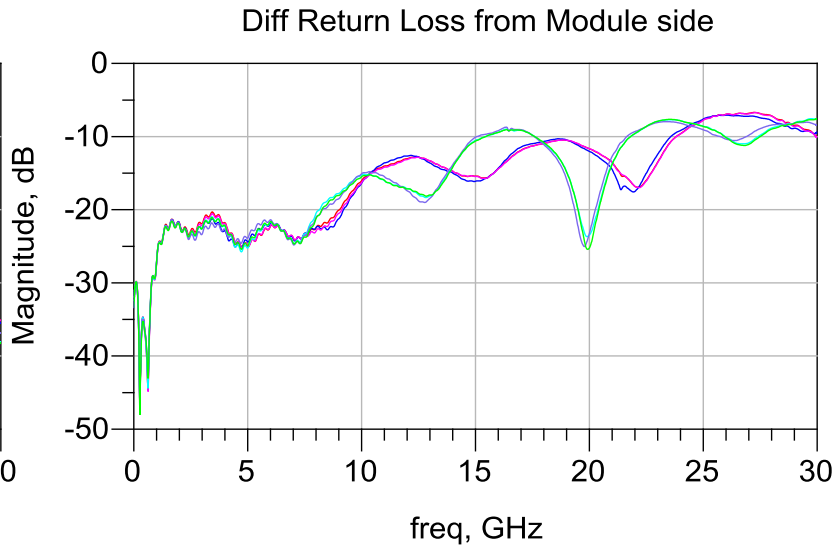
“Next generation 28Gb/s press fit stacked IO”:



Channel 1 THRU Performance

Next Generation 28Gbps High Density SMT IO



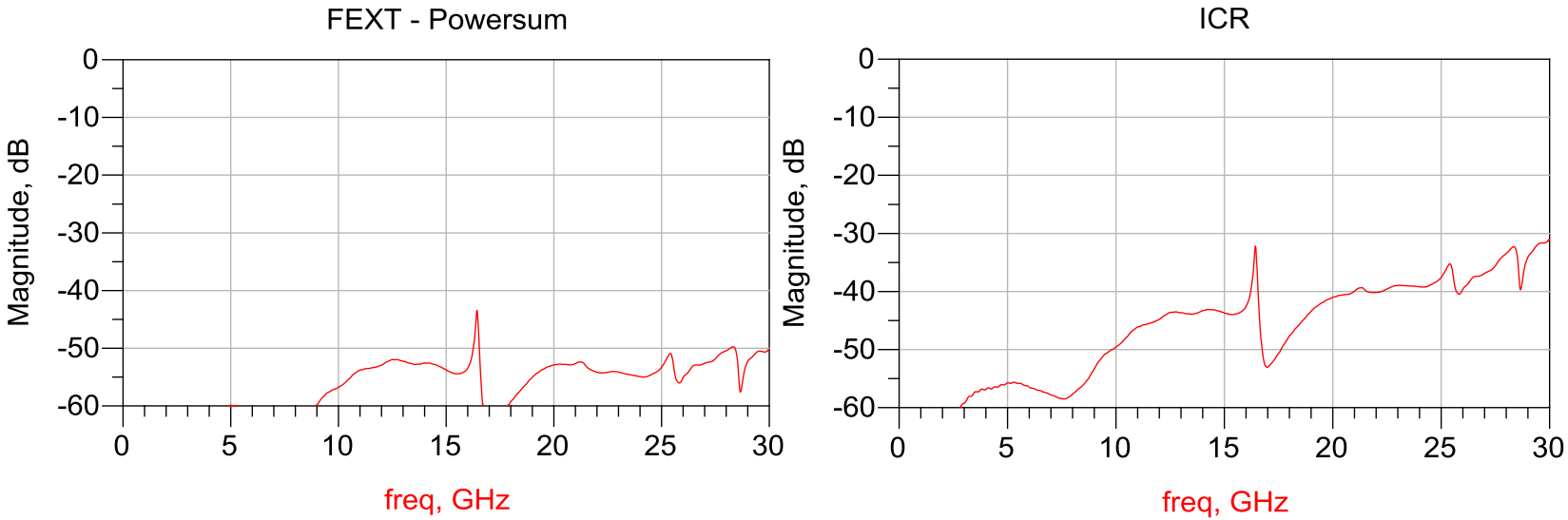


Green – B row pairs
Pink – A row pairs

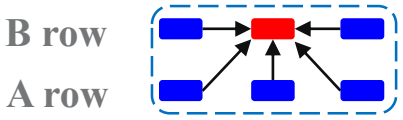
Actual data goes out to 42GHz

Channel 1 Crosstalk Performance

Next Generation 28Gbps High Density SMT IO



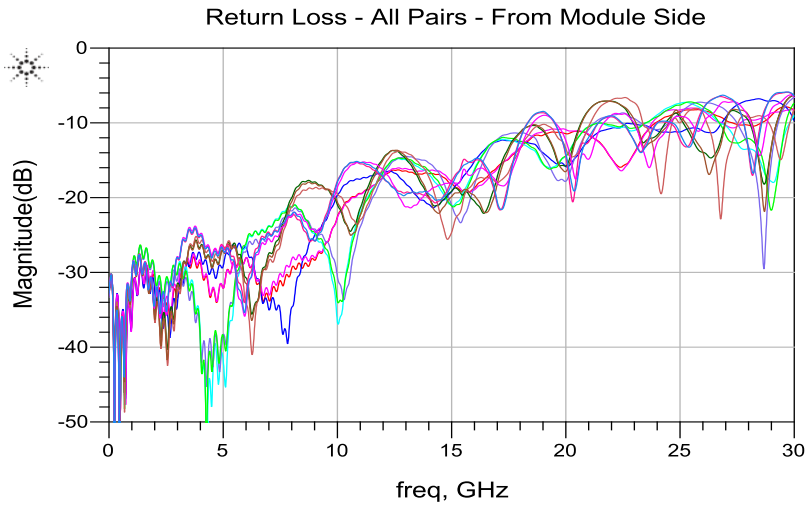
Red - Top row Victim (5 Aggressors)



Actual data goes out to 42GHz

Channel 2 THRU Performance

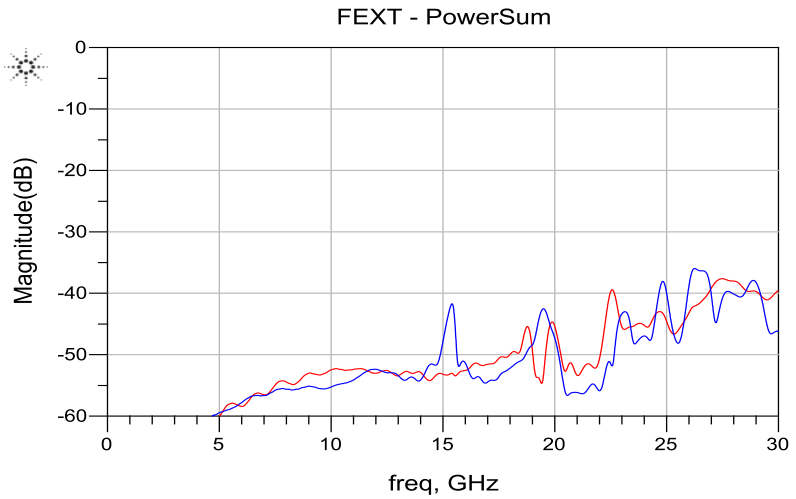
Next Generation 28Gbps Pressfit Stacked IO

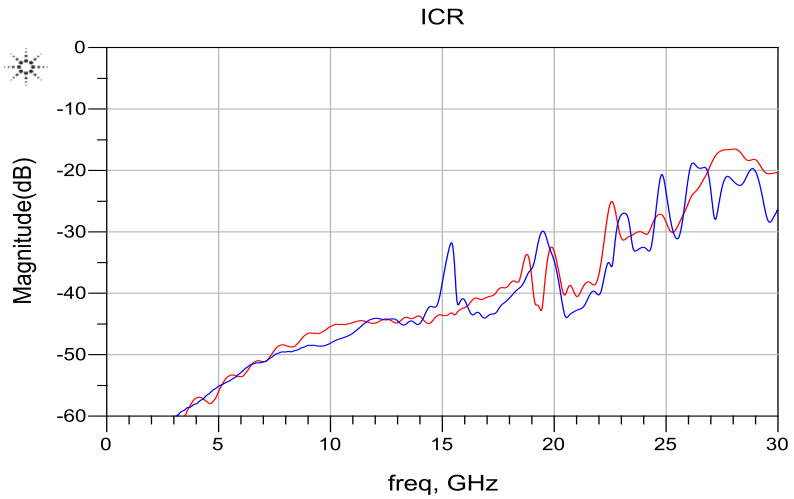


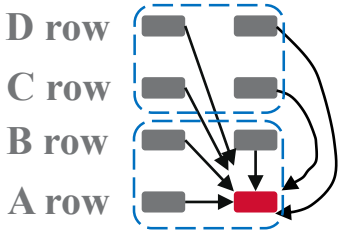
Actual data goes out to 60GHz

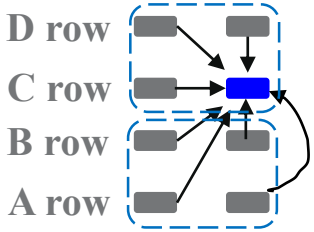
Channel 2 Crosstalk Performance

Next Generation 28Gbps Pressfit Stacked IO









Red – Bot Port Victim (7 Aggressors)

Blue – Top Port Victim (7 Aggressors)

Actual data goes out to 60GHz

Summary

- Two channel models are being considered for IEEE analysis as 50Gb/s channels
- Connector/channel power sum noise and ICR suggest these are good candidates for 50G chip to module analysis
- Both solutions provide high density and use low cost PCB mating interfaces
- One surface mount and one press-fit allow consideration of both mounting conditions
- Feedback is solicited while the connector designs are not finalized