

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 1 SC 1.4 P 20 L 32 # 191  
 Dove, Daniel Dove Networking Solut

Comment Type **TR** Comment Status **X** Definitions

Definition of Single Singature PD doesn't clarify if it applies to all types of PDs, or only specific types. Since Type 1 and 2 PDs were never distinguished by signature type, I'm not clear whether this should only apply to Type 3 and Type 4, or we retro-define Type 1 and Type 2 PDs.

*SuggestedRemedy*  
 Task Force decide which types of PDs will identify as single-signature PDs and change as necessary.

Proposed Response Response Status **W**  
 Task force to discuss.

Cl 1 SC 1.4 P 20 L 34 # 192  
 Dove, Daniel Dove Networking Solut

Comment Type **TR** Comment Status **X** Definitions

Definition of Dual Singature PD doesn't clarify if it applies to all types of PDs, or only specific types. Since Type 1 and 2 PDs were never distinguished by signature type, I'm not clear whether this should only apply to Type 3 and Type 4, or we retro-define Type 1 and Type 2 PDs.

*SuggestedRemedy*  
 Task Force decide which types of PDs will identify as dual-signature PDs and change as necessary. Is such a change within scope of PAR/objectives/Criteria?

Proposed Response Response Status **W**  
 Task force to discuss.

Cl 25 SC 25.4.5 P 24 L 1 # 243  
 Schindler, Fred Seen Simply

Comment Type **TR** Comment Status **D** PMD

Existing text,

"A receiver in a Type 2 or greater Endpoint PSE or Type 2 or greater PD (see Clause 33) shall meet the requirements of 25.4.7. A transmitter in a Type 2 Endpoint PSE or Type 2 PD delivering or accepting more than 13.0 W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TPPMD, or meet the requirements of 25.4.5.1."

should be improved to clarify meaning and to include new Types.

*SuggestedRemedy*  
 "A 100BASE-TX receiver in a Type 2 or greater Endpoint PSE or Type 2 or greater PD (see Clause 33) shall meet the requirements of 25.4.7. A 100BASE-TX transmitter in a Type 2 or greater Endpoint PSE or Type 2 or greater PD delivering or accepting more than 13.0 W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TPPMD, or meet the requirements of 25.4.5.1."

Proposed Response Response Status **W**  
 PROPOSED ACCEPT.

Cl 30 SC 30.9.1.1.6 P 7 L 53 # 165  
 Yseboodt, Lennart Philips

Comment Type **T** Comment Status **D** Management

original text: "An ENUMERATED VALUE that has one of the following entries: ... Class 0 to 4 PD"  
 bt classes missing

*SuggestedRemedy*  
 Append to list:  
 class5Class 5 PD  
 class6Class 6 PD  
 class7Class 7 PD  
 class8Class 8 PD

Add editors note: "Dual signature also needs to be addressed here".

Proposed Response Response Status **W**  
 PROPOSED ACCEPT IN PRINCIPLE.

See comment 8.

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Cl 30 SC 30.9.1.1.6 P 7 L 53 # 8  
 Zimmerman, George CME Consulting, Inc.

Comment Type TR Comment Status D Management

Classifications in Clause 30 need updating to include new PD classes

SuggestedRemedy

Add Classes 5 through 8, and Autoclass to the list of enumerated values.  
 Add editor's note to P8 L5 (after end of paragraph) stating:  
 "Editor's Note (to be removed prior to Working Group ballot): linkage to management registers to be aligned with resolution of issues on how to report more classes than there are bits available in 802.3-2015 Clause 33 PSE status register."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Does Autoclass need an entry in the list? The PD still classifies as class 1-8 before doing Autoclass.

See comment 165

Cl 30 SC 30.12.2.1.14 P 14 L 19 # 166  
 Yseboodt, Lennart Philips

Comment Type T Comment Status D Management

original text: "BIT STRING [SIZE (2)]"  
 "A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD. A PSE shall set this bit to indicate a PSE. A PD shall set this bit to indicate a PD.;"

SuggestedRemedy

"BIT STRING [SIZE (3)]"  
 "A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1, Type 2, Type 3 or Type 4. The first two bits indicate Type 1, Type 2, Type 3 or Type 4. The third bit indicates PSE or PD. A PSE shall set this bit to indicate a PSE. A PD shall set this bit to indicate a PD.;"

Proposed Response Response Status W

PROPOSED ACCEPT.

See comment 10

Cl 30 SC 30.12.2.1.14 P 14 L 23 # 10  
 Zimmerman, George CME Consulting, Inc.

Comment Type TR Comment Status D

"A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2."  
 Needs to be extended to include types 3 & 4

SuggestedRemedy

Add "Editor's Note (to be removed prior to Working Group Ballot) - Need to extend aLdpXdot3LocPowerType or another variable to manage types 3 and 4."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

See comment 166

Cl 30 SC 30.12.2.1.18a P 15 L 38 # 194  
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Management

For these new variables, I could not find a tolerance spec. Should there be one?

SuggestedRemedy

If so, please include a tolerance on the accuracy of the values provided.

Proposed Response Response Status W

Task force to discuss. I assume the answer is no.

Cl 30 SC 30.12.3.1.14 P 23 L 4 # 171  
 Yseboodt, Lennart Philips

Comment Type T Comment Status D Management

original text: "BIT STRING [SIZE (2)]  
 BEHAVIOUR DEFINED AS:  
 A GET attribute that returns a bit string indicating whether the remote system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD."

Add new types

SuggestedRemedy

"BIT STRING [SIZE (3)]"  
 "A GET attribute that returns a bit string indicating whether the remote system is a PSE or a PD and whether it is Type 1, Type 2, Type 3 or Type 4. The first two bits indicate Type 1, Type 2, Type 3 or Type 4. The third bit indicates PSE or PD.;"

Proposed Response Response Status W

PROPOSED ACCEPT.

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Cl 33 SC 33.1 P 27 L 14 # 20  
 Jones, Chad Cisco

Comment Type E Comment Status D

"This clause uses several terms defined in clause 1.4." I took an action item in Bonita Springs to enumerate these new terms.

SuggestedRemedy

add: " - See terms: 1-Event class signature, 1-Event classification, 1000BASE-T, 10BASE-T/100BASE-TX, 2-Event class signature, 2-Event classification, Dual-signature PD, Endpoint PSE, IPort, Link Section, Midpsan, Midpsan PSE, Midspan PSE, Midspan PSE, pairset, Power Interface (PI), Power Sourcing Equipment (PSE), Powered Device (PD), PSE Group, Single-signature PD, TP-PMD, Twisted Pair Medium Dependent Interface (TP MDI), Type 1 PD, Type 1 PSE, Type 2 PD, Type 2 PSE, Type 3 PD, Type 3 PSE, Type 4 PD, Type 4 PSE., VPD, VPSE

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

We have changed "2-Event" to "Multiple-Event" and "1-Event" to "Single-Event"

Cl 33 SC 33.1.1 P 27 L 52 # 13  
 Zimmerman, George CME Consulting, Inc.

Comment Type TR Comment Status D Objectives

"c) Compatibility—Clause 33 utilizes the MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T, without modification.... The clause does not address the operation of 10GBASET. For 10GBASE-T operation, the channel model specified in Clause 55 needs to be met without regard to DTE Power via MDI presence or operation.  
 d) Simplicity—The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, or 1000BASE-T."

Needs to be modified to reflect addition of 10GBASE-T.

SuggestedRemedy

change first sentence of item (c) to read: "10BASE-T, 100BASE-TX, 1000BASE-T and 10GBASE-T without modification."  
 Delete "The clause does not address the operation of 10GBASE-T."  
 change item (d) to read "10BASE-T, 100BASE-TX, 1000BASE-T, or 10GBASE-T."

Proposed Response Response Status W

PROPOSED REJECT.

Didn't we remove the objectives section completely?

We Did. Line 40 has the editing instruction to delete section 33.1.1.

Cl 33 SC 33.1.1 P 27 L 53 # 244  
 Schindler, Fred Seen Simply

Comment Type ER Comment Status D Objectives

Existing text does not cover new types. Legacy text repeats (introduces) cabling requirements. Text covering 10-GBASE-T points to another Clause to get channel requirements. All other PHY data rates place channel requirements for power over DTE in Clause 33. Unnecessary text may confuse the reader.

"Type 1 operation adds no significant requirements to the cabling. Type 2 operation requires ISO/IEC 11801:1995 Class D or better cabling, and a derating of the cabling maximum ambient operating temperature. The clause does not address the operation of 10GBASET.

For 10GBASE-T operation, the channel model specified in Clause 55 needs to be met without regard to DTE Power via MDI presence or operation."

SuggestedRemedy

Replace text with the following,

"Type 1 operation adds no significant requirements to the cabling. Cable requirements for all PSEs are covered in 33.1.4."

Proposed Response Response Status W

PROPOSED REJECT.

This section has been deleted (see line 40.)

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CI 33 SC 33.1.4 P 30 L 9 # 245  
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X Types

The Task Force should discuss the sentence,  
 "The power system is defined by the lowest Type of PSE or PD in a system and has certain basic parameters defined according to Table 33-1. "

The text permits PSEs that can provide class-8 power levels to by be considered class 1 when connected to a PD consuming class 1 power. This permits CAT-3 cabling to be used. This results in a cable power dissipation increase of about 230x, which is about 9x more channel loss than a Type-1 system permits. This comment is related to another comment marked with CONCERN1.

SuggestedRemedy

Change how the power system is defined so that cabling requirements are dictated by,  
 1.The maximum class power the PSE Type can provide, or  
 2.The maximum class power the PSE can provide.  
 The first choice is preferred because users may select PSEs based on Type because historically this has been the case.

Replace the called-out sentence with,  
 "The power system is defined by the highest power class allowed for the Type of PSE in a system and has certain basic parameters defined according to Table 33-1. "

Or

"The power system is defined by the highest power class of the PSE in a system and has certain basic parameters defined according to Table 33-1. "

Proposed Response Response Status W

Task force to discuss.

CI 33 SC 33.1.4 P 30 L 18 # 246  
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X Types

Table 33-1 no longer represents system power levels correctly because Type 4 PSEs may provide class 1 to 8 power levels. Note this concern is related to a comment marked with CONCERN1. This comment may be OBE by another comment marked by CONCERN1 (three comments total).

SuggestedRemedy

Replace Type with the highest power class permitted with the referenced cable system. This results in these changes,

- 1.Replace Table 33-1 title with "System power parameters Vs PSE Class Power"
- 2.Replace Table 33-1 column one title "System Type (Lowest type of PSE and PD)" with "System Power Limit (PSE class)"
- 3.Type 1 becomes Class 3 or 0.
- 4.Type 2 becomes Class 4.
- 5.Type 3 becomes Class 5 and 6.
- 6.Type 4 becomes Class 7 and 8.

Proposed Response Response Status W

Task force to discuss.

CI 33 SC 33.1.4 P 30 L 45 # 229  
 Dwelley, David Linear Technology

Comment Type E Comment Status X Editorial

I believe the study of unbalance and temperature rise has been completed.

SuggestedRemedy

Remove editor's note.

Proposed Response Response Status W

I'm not sure that is true.

Task force to discuss.

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Cl 33 SC 33.1.4 P 30 L 46 # 26  
 Darshan, Yair Microsemi  
 Comment Type E Comment Status X Editorial  
 There is no need for the Editor Note regarding the effect of extended power.  
 SuggestedRemedy  
 Remove the Editor Note  
 Proposed Response Response Status W  
 The note addresses more than extended power.  
 Task force to discuss.

Cl 33 SC 33.1.4 P 30 L 41 # 195  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status D Unbalance  
 Note 2 should only apply for Type 3 when in 4 pair operation. This note doesn't clarify that  
 SuggestedRemedy  
 In Type 3 and Type 4 operation, (when operating on all 4 pairs) the  
 Proposed Response Response Status W  
 PROPOSED REJECT.  
 The note simply points them to the unbalance section which clearly contains this information.

Cl 33 SC 33.1.4.2.1 P 32 L 3 # 230  
 Dwelley, David Linear Technology  
 Comment Type E Comment Status D Unbalance  
 33.1.4.2.1 just says "See Annex 33A", which also appears in 33.1.4.2.  
 SuggestedRemedy  
 Strike 33.1.4.2.1. Replace "within a twisted pair" with "for twisted pair cables" in 33.1.4.2.  
 Fix ISO reference with newer reference that specs pair-to-pair balance. The editor's note in 33.1.4.2.1 can probably be removed as well.  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

Cl 33 SC 33.2.0a P 32 L 33 # 247  
 Schindler, Fred Seen Simply  
 Comment Type TR Comment Status X Types  
 Normative text is not present. The existing text is,  
 "PSEs can be categorized as either Type 1, Type 2, Type 3, or Type 4 PSEs. Table 33-1a shows the permissible PSE types along with supported parameters."  
 SuggestedRemedy  
 Replace the text with,  
 "PSEs can be categorized as either Type 1, Type 2, Type 3, or Type 4 PSEs. PSEs shall meet one or more of the PSE Type requirements provide in Table 33-1a."  
 Proposed Response Response Status W  
 Would this be a duplicate shall to the places where all of these items are discussed in detail. I Imagine so.  
 Task force to discuss (TFTD)

Cl 33 SC 33.2.0a P 32 L 45 # 115  
 Yseboodt, Lennart Philips  
 Comment Type T Comment Status D Types  
 Optional is misleading, see footnote as exception  
 SuggestedRemedy  
 Change to "Optional^2 or Mandatory"  
 Change cell to the left of it (on Phys. Lay. Class.) to "Multiple-Event or Single-Event", so it matches in logical order.  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

Cl 33 SC 33.2.0a P 32 L 47 # 75  
 Johnson, Peter Sifos Technologies  
 Comment Type E Comment Status D Types  
 In Table 33-1a, under "Supports 4-pair power", the phrase "Allowed" is used to say that Type-3, Class 3&4 PSE's may provide 2 or 4 pair power. This is not typical terminology for tables in the standard.  
 SuggestedRemedy  
 Replace "Allowed" with "Optional".  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

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Cl 33 SC 33.2.4.1 P 42 L 27 # 197  
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X PSE SD

I think this sentence only applies to Type 1 and Type 2 PSEs. Does this apply for the case of 4P powering PSE? Example: CC finds DS PD, Seq 0, starts both detections at once.

SuggestedRemedy

Replace "PSE" with "Type 1 or Type 2 PSE"

Proposed Response Response Status W

I'm not sure this is true. If a 4P PSE sees DS and gets an invalid sig on Alt A and an open on Alt B, it could be because there is a 2-Pair Midspan PSE on Alt B. The Alt A PSE should still do another detection within Tdbo...

TFTD

Cl 33 SC 33.2.4.3 P 42 L 53 # 198  
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Pres: Bullock1

A cost improvement is possible if detection for dual-signature PDs can be performed in sequence rather than simultaneously.

SuggestedRemedy

See state diagram changes in bullock\_01\_3bt\_1015 for detail, as I believe Chris addresses this in his presentation.

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.4.4 P 44 L 6 # 59  
 Darshan, Yair Microsemi

Comment Type TR Comment Status D PSE SD

The variable PD\_4pair\_cand in page 44 line 6 and PD\_4pair\_candidate in page 45 line 10:

Not clear they are two separate variables or different variables (the name is different and some of the content).

1. Clarify the intent.
2. The variable PD\_4pair\_can is for Type 3 and Type 4 only since Type 1 and 2 will work only with 2P.
3. the variable PD\_4pair\_candidate is for Type 3 and 4 so I guess it is the correct variable.
4. In the text of PD\_4pair\_candidate on page 45 lines 11-15 we need to use the term "on both modes" instead of "both pairsets" if we want to keep consistency with PD side terminology.

SuggestedRemedy

Clarify the use of the two variables or adopt the following remedy:

1. Delete PD\_4pair\_can in page 44 lines 6 -11.
2. Change from "on both pairsets" on page 45 lines 14 and 15 (two locations) to: "on both modes"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

1. Delete PD\_4pair\_can in page 44 lines 6 -11.

TFTD change # 2.

Cl 33 SC 33.2.4.4 P 44 L 7 # 255  
 Schindler, Fred Seen Simply

Comment Type ER Comment Status D PSE SD

Variable PD\_4pair\_cand on page 66 and PD\_4pair\_candidate on page 67 appear to be for the same purpose. Neither variable is used.

SuggestedRemedy

- 1)Delete both variables and replace one of them with an Editors that reads, Editor's Note: Task force members that want a physical means for determining whether a legacy PD may be powered on both pairsets should provide a solution.

OR

- 2)Use only variable PD\_4pair\_candidate as this variable is used on page 92.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 59.

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CI 33 SC 33.2.4.4 P 45 L 10 # 265  
 Stover, David Linear Technology

Comment Type TR Comment Status D PSE SD

Two versions of the same variable are present, PD\_4pair\_cand and PD\_4pair\_candidate. "cand" is used by SD, "candidate" is used in 33.2.5.6, 4PID requirements.

SuggestedRemedy

Pick a single name and definition. Correct outdated references to whichever name is removed.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 59.

CI 33 SC 33.2.4.4 P 46 L 12 # 29  
 Darshan, Yair Microsemi

Comment Type T Comment Status X PSE SD

The text "Type 3 and Type 4 PSEs shall use this value."  
 The legacy powerup was canceled for Type 3 and 4.  
 In order to keep interoperability between Type 3 systems that operate 4P and those who operate 2P it is better to delete the use of legacy powerup to Type 4 only.

SuggestedRemedy

Change from:  
 "Type 3 and Type 4 PSEs shall use this value."  
 To:  
 "Type 4PSEs shall use this value."

Proposed Response Response Status W

I don't follow the logic.

TFTD.

CI 33 SC 33.2.4.4 P 46 L 27 # 261  
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X PSE SD

Variable mr\_pse\_alternative provides values, A, B, and BOTH, to indicate which PSE Alternative is used. The Task Force needs to decide whether all 2-mosfet PSES drive ALT-A when only one pairset is driven on a PSE that supports BOTH pairsets.

SuggestedRemedy

Recommend using a default of ALT-A for the case called out. This solution is used in the comment marked CONCERN2.

Modify the existing text, on line 31, to provide this informative guidance,  
 Values: A: The PSE uses PSE pinout Alternative A, which is also the default pinout when one pairset is driven on a PSE that supports BOTH pairsets.

Proposed Response Response Status W

Why should we limit it?

TFTD

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Cl 33 SC 33.2.4.4 P 46 L 32 # 57  
 Darshan, Yair Microsemi

Comment Type TR Comment Status D PSE SD

Missing mr\_pse\_alternative A + B(x) in the following text and also we need to correct it while keeping old text unchanged:  
 "mr\_pse\_alternative  
 This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33;V2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.  
 Values:A: The PSE uses PSE pinout Alternative A.  
 B: The PSE uses PSE pinout Alternative B.  
 BOTH: The PSE uses both Alternative A and Alternative B."

SuggestedRemedy

Change from"  
 "mr\_pse\_alternative  
 This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33-2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.  
 Values:  
 A: The PSE uses PSE pinout Alternative A.  
 B: The PSE uses PSE pinout Alternative B.  
 BOTH: The PSE uses both Alternative A and Alternative B."

To:  
 "mr\_pse\_alternative  
 This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33-2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.  
 Values:  
 A: The PSE uses PSE pinout Alternative A.  
 B: The PSE uses PSE pinout Alternative B.  
 BOTH1: The PSE uses both Alternative A and Alternative B.  
 BOTH2: The PSE uses both Alternative A and Alternative B(x)."

Proposed Response Response Status W

PROPOSED REJECT.

Why is this needed in the SD section? We don't list whether the PSE uses Alt A or Alt A(X)...

Cl 33 SC 33.2.4.4 P 46 L 52 # 62  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Bullock1

The variable option\_vport\_lim need to be used in the Type 3 and 4 state machine.

SuggestedRemedy

Clarify where it is being used in Type 3 and 4 state machine.  
 If not used: Add Editor Note: Editor Note: option\_vport\_lim need to be used in Type 3 and 4 state machine in the same way it was used in Type 1 and 2.

Proposed Response Response Status W

Wait for Presentation

Cl 33 SC 33.2.4.4 P 49 L 10 # 63  
 Darshan, Yair Microsemi

Comment Type ER Comment Status D

It is not clear if Table 33-3 is about possible maximum class\_num\_events  
 E.g. Type 3 can use only max of 1,2 or 4 and it may use 3 events.  
 Or Table 33-3 tells that for type 3 we can use only 1,2 and 4.

SuggestedRemedy

Group to clarify the intent.

Proposed Response Response Status W

PROPOSED ACCEPT.

The table defines the allowed values for class\_num\_events variable, which has a definition of:  
 "A variable indicating the maximum number of classification events performed by the PSE.  
 A variable that is set in an implementation-dependent manner."

So clearly, it is the maximum. A Type 3 or 4 PSE can use 3 fingers as shown in the SD.

No changes result from accepting this comment.

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Cl 33 SC 33.2.4.4 P 43 L 5 # 207  
 Dove, Daniel Dove Networking Solut  
 Comment Type E Comment Status X Pres: Bullock1  
 The sentence reads unclearly. It is a state machine that is being communicated with not an alternative.  
 SuggestedRemedy  
 replace with "to the Alternative A State Machine that the Alternative B State Machine is between"  
 Proposed Response Response Status W  
 Wait for Presentation

Cl 33 SC 33.2.4.4 P 43 L 17 # 199  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Pres: Bullock1  
 There are a number of variables that are declared in text one way, and in the State Diagram in another way.  
 SuggestedRemedy  
 Editor review & reconcile all variables in text with diagram. Examples; Alt\_A\_pwr (text) alt\_a\_pwr (diagram)  
 Proposed Response Response Status W  
 Wait for presentation

Cl 33 SC 33.2.4.4 P 43 L 38 # 200  
 Dove, Daniel Dove Networking Solut  
 Comment Type E Comment Status D PSE SD  
 The text is not completely clear on how the negotiation takes place. Its implicit, but not explicit.  
 SuggestedRemedy  
 insert "via L2 classification" at the end of both lines  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.  
 What is the right wording? "DLL" or "LLDP" or "L2"?

Cl 33 SC 33.2.4.4 P 43 L 43 # 201  
 Dove, Daniel Dove Networking Solut  
 Comment Type E Comment Status X Pres: Bullock1  
 Minor editorial suggestion.  
 SuggestedRemedy  
 Insert "to be" between "is" and "2-pair"  
 Proposed Response Response Status W  
 Wait for presentation

Cl 33 SC 33.2.4.4 P 43 L 44 # 202  
 Dove, Daniel Dove Networking Solut  
 Comment Type E Comment Status X Pres: Bullock1  
 Minor editorial suggestion.  
 SuggestedRemedy  
 Insert "to be" between "is" and "4-pair"  
 Proposed Response Response Status W  
 Wait for presentation

Cl 33 SC 33.2.4.4 P 44 L 24 # 203  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X PSE SD  
 pwr\_app\_a is a variable only used by the Type 3 and Type 4 state diagram. Should it be declared as only applying to them. This raises a general question since there are two SDs but the variable list is singular. Should we break out Type 1 and Type 2 variables, Type 3 and Type 4, and common variables? Or leave them all mixed up?  
 SuggestedRemedy  
 I will leave this to the Task Force to decide. It affects a number of variables.  
 Proposed Response Response Status W  
 TFTD

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Cl 33 SC 33.2.4.4 P 44 L 54 # 204  
 Dove, Daniel Dove Networking Solut  
 Comment Type **TR** Comment Status **X** Pres: Bullock1  
 The text in this sentence is incomplete or inaccurate.  
 SuggestedRemedy  
 Replace "POWER\_UP[A]" with "the POWER\_UP[A] or IDLE[A] states."  
 Proposed Response Response Status **W**  
 Wait for presentation

Cl 33 SC 33.2.4.4 P 45 L 8 # 209  
 Dove, Daniel Dove Networking Solut  
 Comment Type **TR** Comment Status **X** Pres: Bullock1  
 The text in this sentence is incomplete or inaccurate.  
 SuggestedRemedy  
 Replace "POWER\_UP[B]" with "the POWER\_UP[B] or IDLE[B] states."  
 Proposed Response Response Status **W**  
 Wait for presentation

Cl 33 SC 33.2.4.4 P 45 L 1 # 205  
 Dove, Daniel Dove Networking Solut  
 Comment Type **TR** Comment Status **X** Pres: Bullock1  
 The text in this sentence is incomplete or inaccurate.  
 SuggestedRemedy  
 Replace "POWER\_UP[A]" with "the POWER\_UP[A] or IDLE[A] states."  
 Proposed Response Response Status **W**  
 Wait for presentation

Cl 33 SC 33.2.4.4 P 45 L 8 # 210  
 Dove, Daniel Dove Networking Solut  
 Comment Type **TR** Comment Status **X** Pres: Bullock1  
 The text in this sentence is incomplete or inaccurate.  
 SuggestedRemedy  
 Replace PSE with "A Type 1 or Type 2 PSE" since Type 3 and Type 4 use pwr\_app\_a/b?  
 Proposed Response Response Status **W**  
 Wait for Presentation

Cl 33 SC 33.2.4.4 P 45 L 2 # 206  
 Dove, Daniel Dove Networking Solut  
 Comment Type **TR** Comment Status **X** Pres: Bullock1  
 The text in this sentence is incomplete or inaccurate.  
 SuggestedRemedy  
 Replace "POWER\_UP[A]" with "the POWER\_UP[A] or IDLE[A] states."  
 Proposed Response Response Status **W**  
 Wait for presentation

Cl 33 SC 33.2.4.4 P 48 L 16 # 211  
 Dove, Daniel Dove Networking Solut  
 Comment Type **TR** Comment Status **D** PSE SD  
 While this was not changed from 802.3at, it appears that the definition of the values for both True and False are incorrect. They appear to be values for pse\_dll\_enabled rather than pse\_dll\_capable.  
 SuggestedRemedy  
 Insert correct definitions.  
 Proposed Response Response Status **W**  
 PROPOSED ACCEPT.

Cl 33 SC 33.2.4.4 P 45 L 7 # 208  
 Dove, Daniel Dove Networking Solut  
 Comment Type **TR** Comment Status **X** Pres: Bullock1  
 The text in this sentence is incomplete or inaccurate.  
 SuggestedRemedy  
 Replace "POWER\_UP[A]" with "the POWER\_UP[A] or IDLE[A] states."  
 Proposed Response Response Status **W**  
 Wait for presentation

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CI 33 SC 33.2.4.4 P 48 L 23 # 212  
 Dove, Daniel Dove Networking Solut  
 Comment Type ER Comment Status D PSE SD  
 A variable cannot probe.  
 SuggestedRemedy  
 replace "probe" with "indicate that the PSE is ready to probe"  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

CI 33 SC 33.2.4.4 P 48 L 46 # 213  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status D PSE SD  
 The text is not completely clear  
 SuggestedRemedy  
 replace "for Tlim within" with "for a time TLIM determined by"  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

CI 33 SC 33.2.4.6 P 51 L 23 # 64  
 Darshan, Yair Microsemi  
 Comment Type TR Comment Status D PSE SD  
 In the text:  
 "When a PD requests a higher Class than a Type 3 or Type 4 PSE can support, the PSE assigns the PD Class 3, 4, or 6, whichever is the highest that it can support."  
 It is not clear why PSE can't assigns the PD Class 3, 4, 5 or 6, whichever is the highest and only assigns the PD Class 3, 4, 5 or 6 as currently stated.  
 SuggestedRemedy  
 Change to:  
 "When a PD requests a higher Class than a Type 3 or Type 4 PSE can support, the PSE assigns the PD Class 3, 4, \*\*5,\*\* or 6, whichever is the highest that it can support."  
 Proposed Response Response Status W  
 PROPOSED REJECT.  
 This is physical layer class and is decribing power demotion. A PSE cannot demote to class 5 since the PD can only tell the difference between 3 class events (class 4) and 4 class events (class 6).

CI 33 SC 33.2.4.6 P 51 L 37 # 65  
 Darshan, Yair Microsemi  
 Comment Type TR Comment Status X PSE SD  
 Addressing dual signature class codes by limiting DS PDs to up to value 4 (class 5).  
 SuggestedRemedy  
 Replace the editor note with the following text:  
 Dual signature PDs is limited to use up to value 4 (class 5) per pairset.  
 Proposed Response Response Status W  
 I don't think that the suggested text covers the entirety of the editor's note.

CI 33 SC 33.2.4.6 P 52 L 5 # 256  
 Schindler, Fred Seen Simply  
 Comment Type ER Comment Status D PSE SD  
 The text on lines 5 and 19,  
 "valid: The PSE has detected a PD requesting power."  
 Should correctly describe what a PSE has completed.  
 SuggestedRemedy  
 Replace text called out on line 5 and line 19 with,  
 "valid: The PSE has detected a valid PD detection signature."  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

CI 33 SC 33.2.4.6 P 53 L 16 # 232  
 Dwelley, David Linear Technology  
 Comment Type E Comment Status X PSE SD  
 "When a Type 2 PSE powers a Type 2, Type 3 or Type 4 PD, the PSE may choose to assign a value of '1' to parameter\_type if mutual identification is not complete (see 33.2.6) and shall assign a value of '2' to parameter\_type if mutual identification is complete." This sentence and the subsequent sentences can be fixed by replacing the last "complete" with "successful".  
 SuggestedRemedy  
 Change "complete" to "successful" in three places. Strike the editor's note.  
 Proposed Response Response Status W  
 TFTD

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Cl 33 SC 33.2.4.6 P 53 L 32 # 233  
 Dwelley, David Linear Technology

Comment Type TR Comment Status X PSE SD

This seems to imply that a Type 3/4 PSE shall only provide 2p power to a Type 1/2 PD:  
 "When a PSE powers a PD of lower Type (TypePD) than its own native type (TypePSE),  
 the PSE shall meet the PI electrical requirements of the PD Type (TypePD), except for  
 ICon, ILIM-2P, IInrush, IInrush-2P, TLIM-2P, and PType (see Table 33-11), for which...".  
 This goes against one goal of the bt project, which is to provide 4p power to existing Type  
 1 and 2 devices where possible.

SuggestedRemedy

Set the sentence in the positive: "A PSE shall meet the Icut-2p and Ihold requirements of  
 the PD it is connected to." These are the only requirements in Table 33-11 I see that might  
 affect this situation. Or strike the sentence - Icut is optional and the Ihold requirements are  
 made clear in 33.2.9. Remove the editor's note.

Proposed Response Response Status W

TFTD

Cl 33 SC 33.2.4.6 P 53 L 33 # 173  
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X PSE SD

"When a PSE powers a PD of lower Type (Type PD ) than its own..."  
 "... the PSE shall meet the PI electrical requirements of the PD Type..."  
 Yes, this paragraph again.

This statement has broad sweeping implications, for instance it forbids 4-pair  
 powering of Type 1/2 PDs.

We have made a lot of changes to parameters for Type 3 and Type 4, it would  
 be impractical for a Type 3/4 PSE to morph into a Type 1/2 PSE.

SuggestedRemedy

Revert this paragraph to the 802.3-2012 version, which only says what a Type 2 PSE must  
 do.

If there are specific interoperability issues between Type 3/4 and Type 1/2, we deal with  
 those  
 separately.

Proposed Response Response Status W

TFTD

Cl 33 SC 33.2.4.7 P 57 L 5 # 266  
 Stover, David Linear Technology

Comment Type TR Comment Status X Pres: Bullock1

Mixed use of e.g., "alt\_a\_pwr" and "alt\_pwr(a)" for inspecting if a particular alt is  
 powered, but only "alt\_a/b\_pwr" variables are defined.

SuggestedRemedy

Defer to PSE SD developer. If there exists a distinction, define "alt\_pwr()". Else, revise  
 SD to use "alt\_a/b\_pwr" nomenclature.

Proposed Response Response Status W

Wait for presentation

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.4.7 P 57 L 7 # 263  
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X Pres: Bullock1

```
TEST_MODE
IF (mr_force_pwr_a) THEN
    Alt_a_pwrd <= TRUE
IF (mr_force_pwr_b) THEN
    Alt_b_pwrd <= TRUE
```

The TEST\_MODE block exit does not facilitate one ALT having a fault while the other is functioning.

*SuggestedRemedy*

Break the existing test,

```
(mr_pse_enable = force_power)*(ovld_det_a + short_det_a+ ovld_det_b + short_det_b)
```

Into two, one path that

```
(mr_pse_enable = force_power)*(ovld_det_a + short_det_a)
```

That goes to a block,

```
TEST_ERROR_A
Alt_a_pwrd <= FALSE
```

Exit the block as was the case in TEST\_ERROR.

And another path that

```
(mr_pse_enable = force_power)*(ovld_det_b + short_det_b)
```

That goes to a block,

```
TEST_ERROR_B
Alt_b_pwrd <= FALSE
```

Exit the block as was the case in TEST\_ERROR.

*Proposed Response* Response Status W

Wait for presentation

Cl 33 SC 33.2.4.7 P 57 L 16 # 267  
 Stover, David Linear Technology

Comment Type TR Comment Status X Pres: Bullock1

Mixed use of e.g., "pwr\_app(a)" and "pwr\_app\_a" for inspecting if power is applied to a particular alt, but only "pwr\_app\_a/b" variables are defined.

*SuggestedRemedy*

Defer to PSE SD developer. If there exists a distinction, define "pwr\_app()". Else, revise SD to use "pwr\_app\_a/b" nomenclature.

*Proposed Response* Response Status W

Wait for presentation

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.4.7 P 59 L 5 # 262  
 Schindler, Fred Seen Simply  
 Comment Type TR Comment Status X Pres: Bullock1

The POWER\_UP block (where in-rush occurs) should check that 4-pair power is permissible. This is also required at block POWER\_ON (where power is stable). A solution provided in a comment marked CONCERN2 is used to deal with the case when a PSE is not allowed to power on both pairsets. This approach mirrors what the existing state diagram does in POWER\_ON. The solution also fixes POWER\_ON block so that both pairsets are used when the PSE provides this option.

```
POWER_UP
IF (mr_pse_alternative = a ) THEN
alt_a_pwr <= TRUE
```

```
IF (mr_pse_alternative = b ) THEN
alt_b_pwr <= TRUE
```

```
IF (sig_type = single) THEN
alt_a_pwr <= TRUE
alt_b_pwr <= TRUE
```

```
POWER_ON
IF (sig_type = single) THEN
IF ( dll_4PID = 0 ) +
(mr_pse_ss_mode = 0)) THEN
alt_a_pwr <= TRUE
alt_b_pwr <= FALSE
ELSE
alt_a_pwr <= TRUE
alt_b_pwr <= TRUE
```

```
IF( mr_PSE_alternative = a) THEN
alt_a_pwr <= TRUE
```

```
IF( mr_PSE_alternative = b) THEN
alt_b_pwr <= TRUE
```

SuggestedRemedy

```
POWER_UP
IF (mr_pse_alternative = a ) THEN
alt_a_pwr <= TRUE
```

```
IF (mr_pse_alternative = b ) THEN
alt_b_pwr <= TRUE
```

```
IF (((sig_type = single) *
```

```
(dll_4PID = 1) ) * (mr_pse_alternative = BOTH)))
THEN
alt_a_pwr <= TRUE
alt_b_pwr <= TRUE
ELSE
alt_a_pwr <= TRUE
```

```
POWER_ON
IF (sig_type = single) THEN
IF(dll_4PID = 0) +
(mr_pse_ss_mode = 0)) THEN
alt_a_pwr <= TRUE
alt_b_pwr <= FALSE
ELSE
IF( mr_PSE_alternative = BOTH) THEN
alt_a_pwr <= TRUE
alt_b_pwr <= TRUE
```

```
IF( mr_PSE_alternative = a) THEN
alt_a_pwr <= TRUE
```

```
IF( mr_PSE_alternative = b) THEN
alt_b_pwr <= TRUE
```

Proposed Response Response Status W  
 Wait for presentation

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.4.7 P 59 L 42 # 110  
 Bennett, Ken Sifos Technologies, In

Comment Type TR Comment Status X PSE SD

The CLASS\_EVAL box outputs in the State diagram of 33-9A needs to be updated.

The Class Eval box currently denies power in all cases when the PD request exceeds the PSE Available power.

The suggested remedy produces the behaviors described in Tables 33D-1 and 33D-2.

( Note: (pse\_avail\_pwr<2); 2="Class 3,0" )

SuggestedRemedy

Change Path leading to POWER\_UP to:

ted\_timer\_done \* [ (pd\_req\_pwr<=pse\_avail\_pwr) + [(pd\_req\_pwr>pse\_avail\_pwr) \* (pse\_avail\_pwr>1)]]

Change Path leading to POWER\_DENIED to:

!ted\_timer\_done + [ (pd\_req\_pwr>pse\_avail\_pwr) \* (pse\_avail\_pwr<2) ]

Proposed Response Response Status W

TFTD

Cl 33 SC 33.2.4.7 P 64 L 10 # 106  
 Bennett, Ken Sifos Technologies, In

Comment Type TR Comment Status D PSE SD

The Type 3 and 4 State diagram in 33-9D needs to be updated to provide the behaviors described in Table 33D-1 and 33D-2.

This is comment 1 of 4 and refers to the output of CLASS\_EV1\_LCF

( Note: (pse\_avail\_pwr<3); 3="Class 4" )

SuggestedRemedy

Change Path leading to MARK\_EV\_LAST to:

Tclf\_timer\_done \* [ [(sig\_type=single) \* [(mr\_pd\_class\_detected<4) + (pse\_avail\_pwr<3)]] + [(sig\_type=dual) \* (pd\_req\_pwr>pse\_avail\_pwr)] ]

Change Path leading to MARK\_EV1 to:

Tclf\_timer\_done \* [ [(sig\_type=single) \* [ (mr\_pd\_class\_detected = 4) \* (pd\_req\_pwr <= pse\_avail\_pwr) ] + [(sig\_type=dual) \* (pd\_req\_pwr <= pse\_avail\_pwr)] ]

Proposed Response Response Status W

PROPOSED ACCEPT.

This is moving power demotion into the SD. TFTD.

Cl 33 SC 33.2.4.7 P 64 L 14 # 174  
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PSE SD

Figure 33-9d, Transition from CLASS\_EV1\_LCF to MARK\_EV1:  
 "tclf\_timer\_done \* !pse\_skips\_multiclass \* ..."

pse\_skips\_multiclass does not apply to Type 3 or Type 4 PSEs.

SuggestedRemedy

XX=remove  
 "tclf\_timer\_done \* XX!pse\_skips\_multiclass \*XX ..."

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.4.7 P 64 L 21 # 107  
 Bennett, Ken Sifos Technologies, In

Comment Type TR Comment Status D PSE SD

The Type 3 and 4 State diagram in 33-9D needs to be updated to provide the behaviors described in Table 33D-1 and 33D-2.

This is comment 2 of 4 and refers to the output of CLASS\_EV2

( Note: (pse\_avail\_pwr>3); 3="Class 4" )

*SuggestedRemedy*

Change Path leading to MARK\_EV\_LAST to:

```
Tcle2_timer_done * (mr_pd_class_detected=temp_var) *
[ [(sig_type=single) * (pd_req_pwr>=pse_avail_pwr)] +
(sig_type!=dual) ]
```

Change Path leading to MARK\_EV2 to:

```
Tcle2_timer_done * (mr_pd_class_detected = temp_var) *
[ [(sig_type=single) * (pse_avail_pwr>3)] +
(sig_type=dual) ]
```

Proposed Response Response Status W

PROPOSED ACCEPT.

This is moving power demotion into the SD. TFTD.

Cl 33 SC 33.2.4.7 P 64 L 27 # 108  
 Bennett, Ken Sifos Technologies, In

Comment Type TR Comment Status D PSE SD

The Type 3 and 4 State diagram in 33-9D needs to be updated to provide the behaviors described in Table 33D-1 and 33D-2.

This is comment 3 of 4 and refers to the output of CLASS\_EV3

( Note: (pse\_avail\_pwr=4, pse\_avail\_pwr>4); 4="Class 5" )

*SuggestedRemedy*

Change Path leading to MARK\_EV\_LAST to:

```
Tcle3_timer_done * [(mr_pd_class_detected=4) +
[ (sig_type=single) * (pd_req_pwr>pse_avail_pwr) * (pse_avail_pwr=4) ] +
[ (sig_type=dual) * [(mr_pd_class_detected = 0) + (pd_req_pwr > pse_avail_pwr)
]]
```

Change Path leading to MARK\_EV3 to:

```
Tcle3_timer_done * [(mr_pd_class_detected!=4) *
[ (sig_type=single) * [(pd_req_pwr>pse_avail_pwr) * (pse_avail_pwr>4)] +
(pd_req_pwr<=pse_avail_pwr) ] +
[ (sig_type=dual) * [(mr_pd_class_detected=3) + (pd_req_pwr<=pse_avail_pwr)] ]
```

Proposed Response Response Status W

PROPOSED ACCEPT.

This is moving power demotion into the SD. TFTD.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 33 SC 33.2.4.7 P 64 L 35 # 109  
 Bennett, Ken Sifos Technologies, In

Comment Type TR Comment Status D PSE SD

The Type 3 and 4 State diagram in 33-9D needs to be updated to provide the behaviors described in Table 33D-1 and 33D-2.

This is comment 4 of 4 and refers to the output of CLASS\_EV4

SuggestedRemedy

Change Path leading to MARK\_EV\_LAST to:

```
Tcle4_timer_done * (mr_pd_class_detected = temp_var) *
[(mr_pd_class_detected<2) +
[(sig_type=single) * (pd_req_pwr>pse_avail_pwr)] +
(sig_type=dual) ]
```

Change Path leading to MARK\_EV4 to:

```
Tcle4_timer_done * (mr_pd_class_detected=temp_var) *
[(mr_pd_class_detected>1) * [(sig_type=single) * (pd_req_pwr<=pse_avail_pwr)] +
(sig_type!=dual)] ]
```

Proposed Response Response Status W

PROPOSED ACCEPT.

This is moving power demotion into the SD. TFTD.

CI 33 SC 33.2.4.7 P 57 L 27 # 215  
 Dove, Daniel Dove Networking Solut

Comment Type ER Comment Status X PSE SD

Throughout the State Diagram, there are numerous connectors that run on-page. This is a question of style, but I believe it would be more readable if only off-page connectors are used and lines tying blocks together used on-page.

SuggestedRemedy

I will leave this to the Task Force to decide. It affects a number of connectors. Example: A is a connector that as an input to IDLE supports numerous off-page connections. For on-page, a line from each state combining together to a single return to A would be easier to follow.

Proposed Response Response Status W

TFTD. So on page connectors may be needed to keep lines from crossing.

CI 33 SC 33.2.4.7 P 57 L 27 # 214  
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Pres: Bullock1

It will enable lower cost implementations if we allow staggering of detection for the dual-signature cases. Please see attached presentation.

SuggestedRemedy

See state diagram changes in bullock\_01\_3bt\_1015 for detail, as I believe Chris addresses this in his presentation.

Proposed Response Response Status W

Wait for presentation

CI 33 SC 33.2.4.7 P 59 L 1 # 216  
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X Pres: Bullock1

We need a connector name here. C1?

SuggestedRemedy

Add connector and ensure that it connects to all appropriate locations within State Diagram.

Proposed Response Response Status W

Wait for presentation

CI 33 SC 33.2.4.7 P 59 L 18 # 217  
 Dove, Daniel Dove Networking Solut

Comment Type E Comment Status D PSE SD

The logic for this arc is located at the entry to the state rather than the exit. Is there a style convention here?

SuggestedRemedy

Follow style convention as it applies. I would presume the logic for exiting a state should go at the exit.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

All of the SDs will need to be redrawn in Frame eventually. Editor to follow IEEE style guide when the time comes.

No changes to the draft result from this comment.

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CI 33 SC 33.2.4.7 P 59 L 20 # 218  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Pres: Bullock1  
 Is there really a need for this state/arcs?The variable gets cleared in IDLE, then set down here. What if its set all the time?  
 SuggestedRemedy  
 There are three POWER\_ON states (alt-A, alt-B, 4P) that all have this loop. Is it necessary? If not, remove.  
 Proposed Response Response Status W  
 Wait for presentation

CI 33 SC 33.2.4.7 P 59 L 23 # 219  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Pres: Bullock1  
 The logic for this state appears not to be as indicated in text. There are other issues about the logic in this state, but if we intend to leave it, I recommend changing it.  
 SuggestedRemedy  
 By the time a 4P SS arrives at POWER\_ON, it has already powered all 4 pair and inrushed them. Is this really how we want this to work? This logic should be (dll\_4PID=0) \* (mr\_pse\_ss\_mode=0) so that EITHER of these variables being 1 will lead to operation in 4P mode.  
 Proposed Response Response Status W  
 Wait for presentation

CI 33 SC 33.2.4.7 P 61 L 13 # 220  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Pres: Bullock1  
 Can't find pse\_avail\_pwr(a) defined. There is a PSE\_avail\_pwr but it doesn't appear to be defined on a pair-set basis, also CAPs rather than lower case.  
 SuggestedRemedy  
 Either add the variable where required or some text that articulates how this variable instance relates to PSE\_available\_power.same goes, for instance with pd\_req\_pwr(a) etc.  
 Proposed Response Response Status W  
 Wait for presentation

CI 33 SC 33.2.4.7 P 64 L 6 # 221  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Pres: Bullock1  
 The logic for the entry arc is not necessarily the same logic as the exit logic on other pages that lead into it.  
 SuggestedRemedy  
 I think striking the logic is fine. The other pages that feed into it should have logic on exit from prior states. Also, this states PSE > 2. Given that it's a Type 3 and Type 4 state machine, wouldn't this always be the case?  
 Proposed Response Response Status W  
 Wait for presentation

CI 33 SC 33.2.4.7 P 64 L 51 # 223  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Pres: Bullock1  
 Exit Arc E is incorrect  
 SuggestedRemedy  
 Replace E with A?  
 Proposed Response Response Status W  
 Wait for presentation

CI 33 SC 33.2.4.7 P 64 L 51 # 222  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Pres: Bullock1  
 Exit Arc C is incorrect  
 SuggestedRemedy  
 Replace C with C1?  
 Proposed Response Response Status W  
 Wait for presentation

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Cl 33 SC 33.2.5.0a P 66 L 35 # 14  
 Zimmerman, George CME Consulting, Inc.

Comment Type TR Comment Status D Connection Check

"The connection check shall be rerun before applying power if power up fails to meet the timing requirements or power is absent on both pairsets simultaneously after reaching the POWER\_UP state."

The timing of this key specification is unclear. how long does power have to be absent for from both pairsets?

'if power up fails to meet the timing requirements' is unclear - which timing requirements, any of them?

SuggestedRemedy

Add 'in Section TBD' after "meet the timing requirements", to reference the timing requirement that needs to be met explicitly by name, table, section, or equation number. (sorry, but its so unclear I don't know which one to point to)

Add 'for at least TBD msec' after 'or power is absent on both pairsets simultaneously after reaching the POWER\_UP state.'

Proposed Response Response Status W

PROPOSED ACCEPT.

Add 'in Table 33-3a or in section 33.2.7.12' after "meet the timing requirements"

TFTD:

Add 'for at least TBD msec' after 'or power is absent on both pairsets simultaneously after reaching the POWER\_UP state.'

Cl 33 SC 33.2.5.5 P 70 L 14 # 77  
 Johnson, Peter Sifos Technologies

Comment Type E Comment Status D Backoff

33.2.5.5 was referenced with regard to PSE's that perform detection using "only Alternative B..." (See 33.2.4.1) So to be consistent, suggest specifying "only Alternative B" here as well.

SuggestedRemedy

"If a PSE that is performing detection using only Alternative B (see 33.2.3)..."

This way, there is no confusion with 4-pair detection cases.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.5.6 P 70 L 25 # 224  
 Dove, Daniel Dove Networking Solut

Comment Type TR Comment Status X 4PID

There is a TBD in the text. This cannot persist into draft 2.0

SuggestedRemedy

This TBD will have to be removed prior to 2.0

Proposed Response Response Status W

TFTD

Cl 33 SC 33.2.6 P 70 L 29 # 175  
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Yseboodt1

This section needs to be made consistent with the new Figures 33-14.

SuggestedRemedy

See presentation yseboodt\_1\_1015\_baseline\_fig3314\_vXX.pdf

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.6 P 71 L 22 # 78  
 Johnson, Peter Sifos Technologies

Comment Type E Comment Status D Editorial

Equation 33-3 was moved to its proper place relative to text, however, the variable descriptions for Eq. 33-3 were not moved.

SuggestedRemedy

Move variable descriptions "where ... Vpse ..." to just below Equation 33-3.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 158

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Cl 33 SC 33.2.6 P72 L1 # 176  
 Yseboodt, Lennart Philips  
 Comment Type **TR** Comment Status **D** PSE Class  
 Table 33-7 does not provide dual-signature classes.  
 SuggestedRemedy  
 See yseboodt\_table\_33\_7\_v1XX.pdf  
 Proposed Response Response Status **W**  
 Waiting for Table

Cl 33 SC 33.2.6 P72 L7 # 95  
 Skinner, John Sifos Technologies, In  
 Comment Type **E** Comment Status **D** PSE Class  
 Table 33-7 Column heading "Number of Classification Events" is not fully descriptive, and does not communicate what the table is trying to convey.  
 SuggestedRemedy  
 Change column heading:  
 "Number of Classification Events"  
 to:  
 "Number of Classification Events Required to Achieve Minimum supported power levels."  
 Proposed Response Response Status **W**  
 PROPOSED ACCEPT.

Cl 33 SC 33.2.6 P72 L16 # 101  
 Beia, Christian STMicroelectronics  
 Comment Type **ER** Comment Status **D** PSE Class  
 Table 33-7  
 Pclass values can be defined as a single number, in order to make the requirement clearer, and easily readable.  
 Today it is needed to compare Pclass with Ptype. The calculation of Ptype requires looking at different tables.  
 - Ptype definition in Table 33-11:  
 Iicable \* Vport\_PSE\_2p\_min for Types1,2, and 3 up to Class4;  
 2\* Iicable \* Vport\_PSE\_2p\_min for Type3 classes 5-8;  
 90W-99.9W for Type4.  
 - Iicable definition in Table 33-1:  
 0.35A for Type1;  
 0.6A for Types2,3;  
 0.96A for Type4.  
 - Vport\_PSE\_2p\_min definition in Table 33-11:  
 44V for Type1;  
 50V for Types2,3;  
 52V for Type4.  
 The result of the calculation of Ptype is:  
 - 15.4W for Type 1  
 - 30.0W for Type 2 and Type 3 classes 0-4  
 - 60.0W for Type 3 classes 5-8  
 - 90W for Type4  
 So, at the end Ptype is never lower than the defined Pclass and can be removed since it doesn't add any restriction to Pclass.

SuggestedRemedy  
 Change Table 33-7, third column (Pclass), classes 4 to 8, as follows:  
 Class 4: 30W  
 Class 5: 45W  
 Class 6: 60W  
 Class 7: 75W  
 Class 8: 90W

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*Proposed Response*      *Response Status*   **W**

PROPOSED REJECT.

This language was extended from the definition of class 4 in this table from AT. If a Type 3 PSE gets connected to a Type 4 PD that is asking for class 8, the minimum supported power is the Ptype for Type 3 (60W), not 90W...

*Cl* **33**      *SC* **33.2.6**      *P* **73**      *L* **37**      # **80**

Johnson, Peter      Sifos Technologies

*Comment Type*   **T**      *Comment Status*   **D**      *PSE Class*

Regarding Type-1 PSE classification with single event: "Valid classification results are Classes 0 up to and including 4, as listed in Table 33-7."

This phrase seems awkward in light of current structure of Table 33-7 where there are now Classes 0-8 and Class 4 row indicates "2 or 3" events. This is mostly non-normative, old text and it might be more accurate if it referenced Table 33-9 instead of Table 33-7. One possible solution is proposed here.

*SuggestedRemedy*

Modify to:

"...Single-Event Physical Layer classification. Valid classification results include Classes 0, 1, 2, 3, or 4 as listed in Table 33-9. A Type-1 PSE detecting Class 4 assigns that PD to Class 0. If a Type-1 PSE does not...."

The normative text for Type-1 PSE treatment of class 4 already exists in 33.2.6.1.

*Proposed Response*      *Response Status*   **W**

PROPOSED ACCEPT.

*Cl* **33**      *SC* **33.2.6.2**      *P* **75**      *L* **22**      # **83**

Johnson, Peter      Sifos Technologies

*Comment Type*   **T**      *Comment Status*   **D**      *PSE Class*

The phrase "PSEs that implement CLASS\_EV1\_LCF, when connected..." is a description of state machine behavior squeezed between other paragraphs that are describing electrical characteristics.

Also, "PSEs that implement CLASS\_EV1\_LCF" is a wordy way of saying "Type 3 and 4 PSEs".

*SuggestedRemedy*

Move this sentence down by 2 or 3 paragraphs to present line 40 (just before "If the result of the first Class...").

Change "PSEs that implement CLASS\_EV1\_LCF" to "Type 3 and Type 4 PSEs".

*Proposed Response*      *Response Status*   **W**

PROPOSED ACCEPT.

*Cl* **33**      *SC* **33.2.6.2**      *P* **75**      *L* **52**      # **84**

Johnson, Peter      Sifos Technologies

*Comment Type*   **E**      *Comment Status*   **D**      *PSE Class*

"...detected during CLASS\_EVE1\_LCF is a 0, a Type 3 or Type 4 PSE treats a dual-signature PD as a Type 1 PD and shall omit the subsequent mark and Class events and classify the PD according to the result of the first Class event."

Since we know the first class event is 0, save some words.

*SuggestedRemedy*

Change to:

"...detected during CLASS\_EVE1\_LCF is a 0, a Type 3 or Type 4 PSE treats a dual-signature PD as a Type 1 PD and shall omit the subsequent mark and Class events and classify the PD as Class 0."

*Proposed Response*      *Response Status*   **W**

PROPOSED ACCEPT.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 33 SC 33.2.6.2 P 76 L 7 # 85  
 Johnson, Peter Sifos Technologies

Comment Type T Comment Status D PSE Class

"... The PSE shall classify the PD only once. Classification..."

Once for all time ? (there is a "shall" here...)

Also, the first half of this paragraph seems to apply to Single-Signature PD's. Suggest splitting this into two paragraphs.

Finally, the 2nd to last sentence "See Annex 33E..." needs to go - the following sentence "See Annex 33D..." is the one that belongs.

SuggestedRemedy

Modify to:

"... The PSE shall classify the PD only once following successful detection. Classification..."

Start new paragraph with "A Type 3 or Type 4 PSE connected to a dual-signature PD shall skip...."

Remove 2nd to last sentence starting with "See Annex 33E..."

Proposed Response Response Status W  
 PROPOSED ACCEPT.

CI 33 SC 33.2.6.2 P 76 L 7 # 118  
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PSE Class

The sentence: "The PSE shall classify the PD only once".  
 Seems to preclude classification of dual signature altogether. After all, a DS PD is ONE PD, but it needs to be classified on each pairset.

SuggestedRemedy

Remove "The PSE shall classify the PD only once"

Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.

This sentence is intended only for single-signature PDs.

It seems that a few paragraphs have been combined.

CI 33 SC 33.2.6.2 P 76 L 16 # 177  
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PSE Class

Table 33-9 shows a direct link between class currents and "Class".  
 This was true for af/at, but this is more complicated now.

The PSE section does not have a Table 33-16a equivalent. This should still be done.

SuggestedRemedy

Change "Class" to "class signature" in Table 33-9

Proposed Response Response Status W  
 PROPOSED ACCEPT.

CI 33 SC 33.2.6.2 P 77 L 27 # 119  
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PSE Class

Table 33-10, item 8 on T\_ME2.

The add. info says:

"The maximum value of T ME2 cannot exceed the maximum allowed time from end of detection until power-on which is limited by 33.2.7.12."

This means the maximum time is Tpon, which is not the intention.

SuggestedRemedy

"The maximum value of T ME2 cannot cause a violation of Tpon, as defined in section 33.2.7.12."

Alternative: remove add. info.

Proposed Response Response Status W  
 PROPOSED ACCEPT.

CI 33 SC 33.2.6.2 P 77 L 51 # 44  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X PSE Class

Table 33-10 item 13 TCLE 3 max value needs more margin.  
 Increase it to 20msec.

SuggestedRemedy

Increase TCLE 3 max value to 20msec.

Proposed Response Response Status W  
 TFTD.

This affects total class time and power dissipation in the PD.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.6.3 P 88 L 43 # 257  
 Schindler, Fred Seen Simply

Comment Type ER Comment Status D Autoclass

The units of Pac\_margin and PAutoclass appear to be Watts but this is not called out. These variables are used in the formula above their description.

SuggestedRemedy

Call out Watts by adding the following text before the period on line 44, ", both variables are in Watts."

Proposed Response Response Status W

PROPOSED REJECT.

We don't specify this in any of the other equations that have parameters in volts, amps, or watts.

Cl 33 SC 33.2.7 P 79 L 33 # 74  
 Johnson, Peter Sifos Technologies

Comment Type T Comment Status X Icon

Icon in Table 33-11, item 4, is defined as the "Continuous total output current capability in POWER\_ON state". The minimum value is then expressed as Pclass/Vport\_pse\_2p. This then requires that Pclass is the total power furnished by a PSE to a PD.

In draft 1.3, paragraph 33.2.6 added (p. 70, line 52) "For Type 3/DS and Type 4/DS PDs, Pclass applies to each pairset independently." This statement is also a problem with regard to the description of the Pclass equation where it says "...or Rchan = Rch/2 when powering using tow pairsets...".

These elements are contradictory and must be reconciled.

SuggestedRemedy

This may be a smaller piece of a bigger issue relating to Dual Signature PD's and whether those PD's generally constitute dual independent loads that are policed per pairset or without concern for pair-pair unbalance. Or if they are shared load devices where pair-pair unbalance interferes with policing per pairset.

I am not proposing a solution at this point for fear that this is not an easy fix until more funatmental issues about dual signature PD's are resolved.

If nothing else, an editors comment adjacent to Table 33-11 indicating that Icon and Pclass as used in Table 33-11 are not presently consistent with the handling of Dual Signature PD's.

Proposed Response Response Status W

TFTD

Cl 33 SC 33.2.7 P 79 L 37 # 46  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan1

Table 33-11 item 4a. Icon-2P\_unb is equal to lcut-2P minimum at its worst case conditions (at Vport\_PSE minmum and worst case Rch in terms of E2EP2PRub).

Therefore for increasing design flexibility, we can specify Icon-2P\_unb as a fixed value as it is done currently or as a function of Kicut\*Pclass/Vport\_PSE-2P which is equal to lcut-2P min in similar concept used in 802.3at with the addition of Kicut factor to account for E2EP2PRunb.

See details in darashan\_01\_1015.pdf page 16.

SuggestedRemedy

See two options for remedy in darashan\_01\_1015.pdf page 16.

Proposed Response Response Status W

wait for presentation

Cl 33 SC 33.2.7 P 79 L 37 # 30  
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Darshan1

Table 33-11 item 4a, Icon-2P\_unb need to be updated due to the following changes made for D1.2:

1. Increasing PSE Vdiff to 10mV instead of 2mV.
- In addition, the following changes we made for Type 3 system:
2. Increasing system Vdiff for Type 3 to 70mV instead of 60mV to increase margins.
3. Type 4 systems stayed total 60mV vdiff:

SuggestedRemedy

Update Table 33-11 item 4a per darshan\_01\_1015.pdf page 3.

Proposed Response Response Status W

wait for presentation

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 33 SC 33.2.7 P 79 L 49 # 43  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan2

Table 33-11 item 5.  
 Only PSE Type 1 and 2 should support Inrush=0.4A min to Type 1 and 2 PDs.  
 We should not force Type 3 and 4 PSEs to meet this requirement as well due to the fact that PD type 1 and 2 need to meet much higher currents than 0.9A.  
 Rationale:  
 a) It could be a feature and not mandatory requirements.  
 b) System vendors cannot be liable for poorly designed PDs or non-compliant PDs.  
 See darshan\_02\_1015.pdf for details.

SuggestedRemedy

In Table 33-11 item 5, restore PSE Type as 1,2 and delete "all"

Proposed Response Response Status W

wait for presentation.

l^2\*t?

CI 33 SC 33.2.7 P 80 L 7 # 45  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan2

Table 33-11 item 5a.  
 PSE Types 3 and 4 can support all PDs and not only Type 3 and 4 PDs.  
 Compliant PDs should stand more than 0.4A per pair set or total 0.9A.  
 System vendors cannot be liable for poorly designed PDs or non-compliant PDs.  
 See darshan\_02\_1015.pdf for details.

SuggestedRemedy

In Table 33-11 item 5a: In the additional information:  
 Delete "For Type 3 and 4 PDs" or replace with "For all PDs".

Proposed Response Response Status W

wait for presentation

CI 33 SC 33.2.7 P 80 L 15 # 25  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan1

Table 33-11 item 7, Additional Information K\_lcut values need to be updated due to the following changes made for D1.2:  
 1. Increasing PSE Vdiff to 10mV instead of 2mV.  
 In addition, the following changes we made for Type 3 system:  
 2. Increasing system Vdiff for Type 3 to 70mV instead of 60mV to increase margins.  
 3. Type 4 systems stayed total 60mV vdiff:

SuggestedRemedy

Update Table 33-11 item 7, K\_lcut values per darshan\_01\_1015.pdf page 4.

Proposed Response Response Status W

wait for presentation

CI 33 SC 33.2.7 P 80 L 25 # 100  
 Beia, Christian STMMicroelectronics

Comment Type E Comment Status D PSE Power

Table 33-11  
 The definition of Ilim\_2P is explicit for all classes, except for Type2 Class 4 where it is 1.14\*Icable.  
 It can be calculated using Icable definition in Table 33-1 (0.6A for Types 2,3)

SuggestedRemedy

Replace Ilim\_2P, column min, row PSE Type 2, 1.14\*Icable, with 0.684

Proposed Response Response Status W

PROPOSED ACCEPT.

I assume this was done for Type 2 during AT so that when attached to a Type 1 PD, the short circuit min could be lower (I cable = 0.35).

Should we do something similar for Types 3 and 4, or is this covered by the sentence that allows a higher type PSE to take on electrical characteristics of a lower type. I think it is.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7 P 80 L 28 # 31  
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Darshan1

Table 33-11 item 9, ILIM-2P need to be updated due to the following changes made for D1.2:

1. Increasing PSE Vdiff to 10mV instead of 2mV.
- In addition, the following changes we made for Type 3 system:
2. Increasing system Vdiff for Type 3 to 70mV instead of 60mV to increase margins.
3. Type 4 systems stayed total 60mV vdiff:

*SuggestedRemedy*

Update Table 33-11 item 7 per darshan\_01\_1015.pdf page 5.

Proposed Response Response Status W

wait for presentation

Cl 33 SC 33.2.7 P 81 L 7 # 102  
 Beia, Christian STMicroelectronics

Comment Type ER Comment Status D PSE Power

Table 33-11  
 PSE power type minimum value can be calculated instead of leaving the burden to the reader.  
 This makes the table clearer and avoids misinterpretations.

- Icable definition in Table 33-1:  
 0.35A for Type1;  
 0.6A for Types2,3;  
 0.96A for Type4.

- Vport\_PSE\_2p\_min definition in Table 33-11:  
 44V for Type1;  
 50V for Types2,3;  
 52V for Type4.

The result of the calculation of Ptype is:

- 15.4W for Type 1
- 30.0W for Type 2 and Type 3 classes 0-4
- 60.0W for Type 3 classes 5-8

*SuggestedRemedy*

- Change Table 33-11 Item 12:
- split the first row and make one for PSE Type1 and another for PSE Type 2
- For PSE Type 1 replace comumn Min Icable \* (Vport\_PSE-2p min) with 15.4
- For PSE Type 2 replace comumn Min Icable \* (Vport\_PSE-2p min) with 30.0
- For PSE Type 3(note1) replace comumn Min Icable \* (Vport\_PSE-2p min) with 30.0
- For PSE Type 3 replace comumn Min 2\*Icable \* (Vport\_PSE-2p min) with 60.0

Proposed Response Response Status W

PROPOSED ACCEPT.

Again I think this was done in order to combine types 1,2 in AT...

Cl 33 SC 33.2.7 P 81 L 21 # 36  
 Darshan, Yair Microsemi

Comment Type T Comment Status D PSE Power

Table 33-11 item 14, Turn on rise time need to be per pairset.

*SuggestedRemedy*

Change "Turn on rise time" to "Turn on rise time per pairset".

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7 P 81 L 25 # 37  
 Darshan, Yair Microsemi  
 Comment Type T Comment Status D PSE Power  
 Table 33-11 item 15, Turn off time need to be per pairset.  
 SuggestedRemedy  
 Change "Turn off time" to "Turn off time per pairset".  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

Cl 33 SC 33.2.7 P 82 L 19 # 38  
 Darshan, Yair Microsemi  
 Comment Type T Comment Status D PSE Detection  
 Table 33-11 item 23, Detection Timing, additional information:  
 The time to complete detection of a PD is per a pairset or supply a reference for how to  
 treat completion of detection for SS and DS PDs.  
 SuggestedRemedy  
 Change from: "Time to complete detection of a PD"  
 To : "The per pairset time to complete detection of a PD"  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.

Change from: "Time to complete detection of a PD"  
 To : "Time to complete detection on one pairset."

Cl 33 SC 33.2.7 P 82 L 23 # 39  
 Darshan, Yair Microsemi  
 Comment Type T Comment Status D PSE Power  
 Table 33-11 item 24, Error delay Timing, additional information:  
 The time to is per pairset.

SuggestedRemedy  
 Change from:  
 "Delay before PSE may attempt subsequent powering after power removal because of  
 error condition."  
 To:  
 "The per pairset delay before PSE may attempt subsequent powering after power removal  
 because of error condition."

Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.

Change from:  
 "Delay before PSE may attempt subsequent powering after power removal because of  
 error condition."  
 To:  
 "Delay before PSE may attempt subsequent powering of a pairset after power removal  
 from that pairset because of error condition."

Cl 33 SC 33.2.7 P 82 L 30 # 163  
 Yseboodt, Lennart Philips  
 Comment Type E Comment Status X PSE Power  
 Figure(s) 33-14 describe the required current capabilities and the current limits of a PSE.  
 As such, these Figures do not belong in the short-circuit section, their scope is beyond  
 that, but  
 should be placed right after Table 33-11.  
 SuggestedRemedy  
 Move Figure 33-14, 33-14a and 33-14b right after Table 33-11.  
 Proposed Response Response Status W  
 TFTD

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7 P 82 L 39 # 235  
 Dwelley, David Linear Technology  
 Comment Type E Comment Status X PSE Power  
 An active-balanced PSE needs no extra specs - it will act like a normal PSE with coincidentally perfect balance and should meet all unbalance specs easily  
 SuggestedRemedy  
 Remove Note 3.  
 Proposed Response Response Status W  
 TFTD  
 Should it be forced to support Icon-2p-unb?  
 See comment 54

Cl 33 SC 33.2.7 P 82 L 42 # 236  
 Dwelley, David Linear Technology  
 Comment Type E Comment Status D Editorial  
 Tlim\_max is adequately described in 33.2.7.7: "Power shall be removed from the a pairset PI of a PSE before the pairset PI current exceeds the "PSE upperbound template" in Figure 33-14..."  
 SuggestedRemedy  
 Remove Note 4.  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

Cl 33 SC 33.2.7 P 85 L 17 # 54  
 Darshan, Yair Microsemi  
 Comment Type TR Comment Status X PSE Power  
 Addressing the editor note # 3 in page 82 lines 39-40 by adding text in page 85 after line 17. We need to address the case when PSE is using active or passive pair to pair current balancing. It will affect the minimum requirements for Icon-2P\_unb, lcut-2P and ILIM-2P only for the pairs were the current is sensed.  
 SuggestedRemedy  
 Add the following text in page 85 line 17:  
 PSEs that use active or passive pair to pair current or resistance balancing over the pairs were the current is sensed may optionally use lower Icon-2P\_unb, lcut-2P and ILIM-2P per the following equation TBD.

Proposed Response Response Status W  
 TFTD  
 See 235.

Cl 33 SC 33.2.7.4 P 83 L 46 # 48  
 Darshan, Yair Microsemi  
 Comment Type TR Comment Status X Pres: Darshan3  
 See darshan\_03\_1015.pdf for details.  
 The Icon-TBD need to be replaced with Icon-2P\_unb.  
 Rationale:  
 DS PDs can have unbalance too in the positive pairs, in the negative pairs, or both. There is no way to know if it is single load or dual load unless the dual load present different class signature. In this case, no need to meet Icon-2P\_unb  
 SuggestedRemedy  
 Change from:  
 "PSEs connected to a single-signature PD shall meet Icon and Icon-2P\_unb as specified in Table 33-11. PSEs connected to a dual-signature PD shall meet Icon-TBD on each pairset as specified in Table 33-11."  
 To:  
 "PSEs connected to a single-signature PD shall meet Icon and Icon-2P\_unb as specified in Table 33-11.  
 PSEs connected to a dual-signature PD with the same class over each pairset shall meet Icon-2P\_unb on each pairset as specified in Table 33-11.  
 PSEs connected to a dual-signature PD with a different class signature over each pairset are not required to meet Icon-2P\_unb.  
 PSEs connected to an isolated dual-signature PD are not required to meet Icon-2P\_unb."

Proposed Response Response Status W  
 Wait for presentation

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7.4 P 83 L 46 # 97  
 Skinner, John Sifos Technologies, In

Comment Type ER Comment Status D Pres: Darshan3

First paragraph uses the parameter name Icon-TBD when discussing dual-signature PDs, "as specified in Table 33-11."

There is no parameter named Icon-TBD in Table 33-11.

*SuggestedRemedy*

Add the parameter "Icon-TBD" to Table 33-11, identify as Item 4b. If this parameter is not yet worked out, the Min and Max values should be listed as TBD.

Alternatively - replace the reference to "Icon-TBD" in 33.2.7.4 line 46 with the parameter name "Icon", as the remainder of the normative statement specifies this is the continuous current on each pairset, and the existing parameter Icon already defines the continuous current on a pairset. If this remedy is accepted, the parameter "Icon-TBD" in the first sentence of the paragraph on page 84 line 1 will also need to be replaced with the parameter name "Icon".

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.7.4 P 84 L 1 # 178  
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Darshan3

original text: "When connected to a dual-signature PD, Icon-TBD is the minimum current of a pairset that a PSE has to support."

Get rid of TBD in variable name.

*SuggestedRemedy*

See presentation yseboodt\_1\_1015\_baseline\_fig3314\_vXX.pdf

Proposed Response Response Status W

wait for presentation

Cl 33 SC 33.2.7.4 P 84 L 25 # 33  
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Darshan1

Updating Equation 33-4a (The Kipeak equation) due to the following changes made for D1.2:

1. Increasing PSE Vdiff to 10mV instead of 2mV.
- In addition, the following changes we made for Type 3 system:
2. Increasing system Vdiff for Type 3 to 70mV instead of 60mV to increase margins.
3. Type 4 systems stayed total 60mV vdiff:

*SuggestedRemedy*

Update Equation 33-4a per darshan\_01\_1015.pdf page 7.

Proposed Response Response Status W

wait for presentation

Cl 33 SC 33.2.7.4.1 P 85 L 2 # 32  
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Darshan1

Updating Equation 33-4b (PSE PI spec.) due to the following changes made for D1.2:

1. Increasing PSE Vdiff to 10mV instead of 2mV.
- In addition, the following changes we made for Type 3 system:
2. Increasing system Vdiff for Type 3 to 70mV instead of 60mV to increase margins.
3. Type 4 systems stayed total 60mV vdiff:

*SuggestedRemedy*

Update Equation 33-4b per darshan\_01\_1015.pdf page 6.

Proposed Response Response Status W

wait for presentation

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7.5 P 85 L 40 # 47  
 Darshan, Yair Microsemi

Comment Type TR Comment Status D PSE Inrush

We need to allow A Type 3 or Type 4 PSE that is connected to a Class 0-4 single-signature PD and is in the POWER\_UP state to transition between 2-pair and 4-pair power at any time, including after the expiration of Tinrush-2P.

SuggestedRemedy

Add the following text after line 40 in page 85:  
 A Type 3 or Type 4 PSE that is connected to a Class 0-4 single-signature PD and is in the POWER\_UP state may transition between 2-pair and 4-pair power at any time, including after the expiration of Tinrush-2P.

Proposed Response Response Status W

PROPOSED REJECT.

This is already included in the text isn't it? There is no requirement on how many pairs to use for inrush, just that both pairsets must be finished with inrush by a certain time. PSEs can transition between 2 and 4 pair power (when connected to class 0-4 PDs) in the POWER\_ON state.

What is not covered by these conditions?

Cl 33 SC 33.2.7.5 P 85 L 45 # 237  
 Dwelley, David Linear Technology

Comment Type TR Comment Status X Pres: DwelleyXX

linrush-2p should be linrush for all SS PDs (and DS single-load PDs if we define a way to identify them).

SuggestedRemedy

Change linrush-2p to linrush at lines 45, 47, and 49. Add a new sentence to the end of bullets a and b: "When connected to a DS PD, the minimum linrush specs apply to each pairset." Table 33-11 items 5 and 5a will need adjusting as well when we determine the final values for inrush.

Proposed Response Response Status W

Wait for presentation

This would change the effective minimum inrush current (which this comment doesn't directly call out, but is its intent).

Cl 33 SC 33.2.7.5 P 85 L 49 # 238  
 Dwelley, David Linear Technology

Comment Type TR Comment Status X Pres: DwelleyXX

linrush-2p minimum doesn't allow for unbalance effects when connected to a single-load PD. One pairset may fail to meet the minimum requirement when an unbalanced load is connected.

SuggestedRemedy

Define linrush (minimum) as total current for SS PDs (and DS single-load PDs if we define a way to identify them). See presentation dwelley\_3bt\_xx\_1015.pdf.

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.7.5 P 85 L 51 # 49  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X PSE Inrush

The text:  
 "For Type 1 PSE, measurement of minimum linrush-2P requirement to be taken after 1 ms to allow startup transients."  
 Is correct for all PSE types and not only Type 1 PSE.

SuggestedRemedy

Change from:  
 "For Type 1 PSE, measurement of minimum linrush-2P requirement to be taken after 1 ms to allow startup transients."  
 To:  
 "For all PSE types, measurement of minimum linrush-2P requirement to be taken after 1 ms to allow startup transients."

Proposed Response Response Status W

TFTD

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7.5 P 85 L 52 # 28  
 Darshan, Yair Microsemi

Comment Type ER Comment Status D PSE Inrush

The text:  
 A Type 2 PSE that uses 1-EventSingle-Event Physical Layer classification, and requires the 1 ms settling time, shall power up a cClass 4 PD as if it used 2Multiple-Event Physical Layer classification.

-----  
 It is not clear why this text should be part of the POWER\_UP and not part of classification.

SuggestedRemedy

Move this text to classification section or clarify why it is inserted here.

Proposed Response Response Status W

PROPOSED REJECT.

This was done through maintenance between AT and now. We don't have a right to change it. Additionally, this is an inrush spec not a classification spec and belongs here.

Cl 33 SC 33.2.7.5 P 86 L 6 # 239  
 Dwellley, David Linear Technology

Comment Type T Comment Status X PSE Inrush

Figure 33-13: The figure is described on line 26 as a template, but no minimum inrush current is shown. This could imply that the minimum inrush current is zero (especially since Figure 33-14 shows min and max).

SuggestedRemedy

Add a minimum line marked 0.40A(TBD), and adjust as needed based on agreement about Type 3 and 4 inrush levels (this may require adding extra figures as we did with Figure 33-14). Change "linrush-2p" labels to "linrush". Add a new sentence at the end of the section (after equation 33-5): "When connected to a DS PD, the linrush template applies to each pairset."

Proposed Response Response Status W

TFTD

Cl 33 SC 33.2.7.5 P 86 L 24 # 69  
 Johnson, Peter Sifos Technologies

Comment Type E Comment Status X PSE Inrush

"Figure 33-13 - linrush-2P current..." figure description is missing a reference to Inrush from Table 33-11, item 5.

SuggestedRemedy

Re-title this to "Figure 33-13- linrush and linrush-2p current..."

Proposed Response Response Status W

See 239.

Cl 33 SC 33.2.7.6 P 86 L 42 # 114  
 Yseboodt, Lennart Philips

Comment Type ER Comment Status D PSE Power

original text: "If IPort-2P, the current supplied per pairset by the PSE to the PI, exceeds ICUT-2P for longer than TCUT-2P, the PSE may remove power from that pairset."

It should be Icut-2P(min) and Tcut-2P(min)

SuggestedRemedy

"If IPort-2P, the current supplied per pairset by the PSE to the PI, exceeds ICUT-2P(min) for longer than TCUT-2P( min), the PSE may remove power from that pairset."

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7.7 P 87 L 5 # 250  
 Schindler, Fred Seen Simply

Comment Type TR Comment Status D Figure 33-14

The text is should be normative.  
 "Equation (33-6), Equation (33-7) and Figure 33-14 apply to PSEs that operate in 2-pair mode, as well as to Type 3 and Type 4 PSEs connected to dual-signature PDs. Equation (33-6a), Equation (33-7a) and Figure 33-14a apply to Type 3 PSEs connected to single-signature PDs, operating in 4-pair mode. Equation (33-6b), Equation (33-7b) and Figure 33-14b apply to Type 4 PSEs connected to single-signature PDs, operating in 4-pair mode."

*SuggestedRemedy*

Replace the text with,

"Equation (33-6), Equation (33-7) and Figure 33-14 shall apply to PSEs that operate in 2-pair mode, as well as to Type 3 and Type 4 PSEs connected to dual-signature PDs. Equation (33-6a), Equation (33-7a) and Figure 33-14a shall apply to Type 3 PSEs connected to single-signature PDs, operating in 4-pair mode. Equation (33-6b), Equation (33-7b) and Figure 33-14b shall apply to Type 4 PSEs connected to single-signature PDs, operating in 4-pair mode."

Proposed Response Response Status W

PROPOSED REJECT.

The sentences that describe the behavior have the normative "shalls" in them...

Example: Power shall be removed from the a pairset of a PSE before the pairset current exceeds the "PSE upperbound template" in Figure 33-14, Figure 33-14a, and Figure 33-14b.

Cl 33 SC 33.2.7.7 P 87 L 12 # 251  
 Schindler, Fred Seen Simply

Comment Type TR Comment Status X

The existing text,  
 " When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."  
 provides unnecessary guidance. The prior sentence,  
 "Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template" ...."  
 provides requirement.

On pages 100 to 101,  
 "Power may be removed from both pairsets any time power is removed from one pairset. Editor's Note: All other instances of the above statement to be removed from draft. If commentators find any please comment against them." The first sentence called out in this comment is fits the concern expressed in the Editor's note.

The requirement in this section prevents one or both of the pairsets from crossing the PSE upperbound template. Concerns about delays in turning off one pairset then a second pairset may not warranted because the device connected to the PSE is no longer considered a PD. Having the ability to control pairsets individually permits system providers to build systems capable of removing power from a fault while still providing power on a nonfaulting pairset.

*SuggestedRemedy*

Strike the sentence,  
 " When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Proposed Response Response Status W

TFTD

See 50, 51, 52

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 33 SC 33.2.7.7 P 87 L 12 # 51  
 Darshan, Yair Microsemi

Comment Type **TR** Comment Status **X** PSE Power

The text in lines 12-14:  
 "When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

When PD gets to this situation it is already damaged so it is irrelevant if it takes TLIM or 2xTLIM to remove power.

*SuggestedRemedy*  
 Remove the text:  
 "When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Proposed Response Response Status **W**  
 TFTD

See 50, 52, 251

CI 33 SC 33.2.7.7 P 87 L 12 # 52  
 Darshan, Yair Microsemi

Comment Type **TR** Comment Status **X**

The text in lines 12-14:  
 "When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

If power is removed from the first pair set, then all the current is going through one pair set and then power will be removed from that pair set too.  
 This is already covered by the lines 10-12 therefore lines 12-14 is redundant.

*SuggestedRemedy*  
 Remove the text:  
 "When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Proposed Response Response Status **W**  
 TFTD

See 50, 51, 251

CI 33 SC 33.2.7.7 P 87 L 12 # 50  
 Darshan, Yair Microsemi

Comment Type **TR** Comment Status **X** PSE Power

The text in lines 12-14:  
 "When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."  
 is redundant.  
 The requirement is already covered by previous lines lines 10-12:  
 Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template" in Figure 33-14, Figure 33-14a, and Figure 33-14b.

*SuggestedRemedy*  
 Remove the text:  
 "When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Proposed Response Response Status **W**  
 TFTD

See 51, 52, 251

CI 33 SC 33.2.7.7 P 87 L 37 # 60  
 Darshan, Yair Microsemi

Comment Type **TR** Comment Status **X** Pres: Darshan4

Figure 33-14 title is incorrect.  
 See details in updated Figure 33-14/a/b/c in page 6 of darshan\_04\_1015.pdf.

*SuggestedRemedy*  
 Replace:  
 Figure 33-14—POWER\_ON state, per pairset operating current templates for PSEs that operate in 2-pair mode, Type 3 and Type 4 dual-signature PSEs

With:  
 Figure 33-14—POWER\_ON state, operating current templates for Type 1 and Type 2 PSEs or Type 3 and Type 4 PSEs that operate in 2-pair mode.

Proposed Response Response Status **W**  
 wait for presentation

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7.7 P 88 L 11 # 55  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Yseboodt??

- Figure 33-14a on Iport-2P axis:  
To update the constant 0.8A/TBD to 0.9A for better margin.
- Figure 33-14a on Iport axis:  
To update the 1.6A/TBD to (60W/50V)\*1.15=1.38A ==> 1.4A  
(The total current doesnt include unbalance so there is no need for twice the value of Iport-2P.)
- Page 89 line 19 equation 33-6a: To change from 0.8A to 0.9A

SuggestedRemedy

- Figure 33-14a on Iport-2P axis:  
To update the constant 0.8A/TBD to 0.9A for better margin.
- Figure 33-14a on Iport axis:  
To update the 1.6A/TBD to 1.4A
- Page 89 line 19 equation 33-6a: To change from 0.8A to 0.9A

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.7.7 P 88 L 13 # 56  
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Yseboodt??

Figure 33-14a line 13 and Figure 33-14b line 41:  
As a greed in last meeting, we need to change the min equation and replace it with Icon-2P = Icon - Iport-2P-Other. We can also add in the baseline text that the max value of Icon-2P is Icon-2P\_unb.

SuggestedRemedy

- Make the following changes in Figure 33-14b:
- Replace "min(Icon-Iport-2P\_other, Icon-2P\_unb) with Icon-2P.  
In the baseline text specify:  
Icon-2P=Icon-Iport-2P\_other or min(Icon-Iport-2P\_other, Icon-2P\_unb).  
See good example in Lennart's presentation.

Proposed Response Response Status W

Wait for presentation

Cl 33 SC 33.2.7.7 P 88 L 26 # 127  
 Yseboodt, Lennart Philips

Comment Type E Comment Status X Editorial

Figures 33-14 a and b have incorrect aspect ratio.

SuggestedRemedy

Do not change aspect ratio.

Proposed Response Response Status W

Huh, what do you want here Lennart?

Cl 33 SC 33.2.7.7 P 88 L 43 # 128  
 Yseboodt, Lennart Philips

Comment Type E Comment Status D Figure 33-14

Figure 33-14b: TLIMMIN is not consistent with TLIMMIN-2P in rest of figures

SuggestedRemedy

Change to: TLIMMIN-2P

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 33.2.7.10.1 P 119 L 19 # 4  
 Zimmerman, George CME Consulting, Inc.

Comment Type TR Comment Status X Unbalance

CONFUSION IN Rpair:  
"Rpair\_max and Rpair\_min represents PSE and channel effective source impedance that includes the effect of VPort\_PSE\_diff as specified by Table 33-11 item 1a."

This is unclear, and possibly in conflict with P85 lines 10-14:  
"RPair\_max is the maximum PSE common mode effective resistance in the powered pairs of same polarity.  
RPair\_min is the minimum PSE common mode effective resistance in the powered pairs of same polarity."

Do RPair\_min and RPair\_max include the channel, or are they just in the PSE? Are they the combination of the PSE and channel? Are they maximum and minimum requirements OVERALL, or are they just the greater and lesser of the two Rpair values in a given installation? (that seems to be the case, but I am not sure).

SuggestedRemedy

Clarify what the definitions of Rpair\_max and Rpair\_min are. Delete either the definition on page 119 or the definition on page 85, and reference it in the other place.

Proposed Response Response Status W

TFTD

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.2.7.11 P91 L 33 # 260  
Schindler, Fred Seen Simply

Comment Type TR Comment Status X Types

Type-4 PSEs, optimize power transferred to the PD by, using a fixed polarity, a higher supply voltage than other PSE Types, and provide 4-pair-only operation. The sentence,

"Type 4 PSEs are not required to support PType if they are restricted to Class 7 power or lower."

permits Type-4 PSEs to limit output power to class levels 1 to 7. Levels 1 to 6 are already provided by Type 1, 2, and 3, PSEs.

This allowance introduces interoperability issues and adds unnecessary complexity when describing a system to customers or when providing requirements for a specification (see another comment market CONCERN1). Very little system power optimization benefit is provided. For example, a Type-4 PSE providing 25.5W to a PD attached with 30 m of CAT-5e requires 25.97W. The same transfer requires 26.01W from a 4-pair Type-3 PSE. This performance difference is not visible when using three significant digits used within this specification. Note that a Type-3 PSE can have identical performance to a Type-4 PSE when their voltage levels match.

Legacy systems may be described using Type, which covers system power levels, and the cable infrastructure required. A Type-2 PSE powered a Type-2 PD. The added sentence introduces six Type-4 PSEs that will not power a Type-4 class-7 or 8 PD. The cable infrastructure for Type-4 systems needs to be determined using class power levels, which results in three different cabling infrastructures for Type-4 PSEs.

*SuggestedRemedy*

Strike the referenced sentence, which results in Type-4 PSE providing class-7 or 8 power limits. This restores previous conventions and removes many cases that result in interoperability issues. This restriction also increases the likelihood that computer networks can co-exist with networks used to power lighting.

Proposed Response Response Status W  
TFTD

Cl 33 SC 33.2.7.11a P91 L 35 # 259  
Schindler, Fred Seen Simply

Comment Type TR Comment Status X PSE Power

The input average current has been calculated with at least a 1 second window for the Type 1 and 2. It does not make sense to change the window to 4 seconds for Type 4, which increase the energy transferred when the PSE is providing power at the highest power level possible in this clause.

*SuggestedRemedy*

Have the Task Force discuss this. The preferred solution is to use a sliding window size of 1 second.

Proposed Response Response Status W  
TFTD

Cl 33 SC 33.3.2 P97 L 1 # 104  
Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status D PD Class

The second sentence at the top of the page states:  
Type 4/DS PDs only advertise Class 5.

Which does not match the two statements below:

Pg 96, Ln 54: "Type 4/DS PDs advertise a Class signature of 5 on at least one pairset."  
Pg 107, Ln 45: "Dual-signature PDs may advertise a different Class signature on each pairset."

*SuggestedRemedy*

Change pg 97 Line 1 to:

...Type 4/DS PDs advertise Class 5 on at least one pairset.

Proposed Response Response Status W  
PROPOSED ACCEPT.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 33 SC 33.3.2 P 97 L 5 # 254  
 Schindler, Fred Seen Simply

Comment Type TR Comment Status D PD Class

The modified legacy text exists to require PDs to provide an indication of under power. Unfortunately, the power level at which this is possible is not precisely called out. Ideally, the indicator should operate at the lowest PSE power class-1 level.

"A Type 2, Type 3 or Type 4 PD that does not successfully observe a Multiple-Event Physical Layer classification or Data Link Layer classification shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer."

SuggestedRemedy

Change the sentence to,  
 "A Type 2, Type 3 or Type 4 PD that does not successfully observe a Multiple-Event Physical Layer classification or Data Link Layer classification shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer.

Type 3 or Type 4 PDs shall provide the active indication while operating within PD power class 1."

Proposed Response Response Status W

PROPOSED REJECT.

Do we really want to restrict them to class 1? Type 1, yes.

This would seem to be a feature, but not a requirement for interoperability.

CI 33 SC 33.3.5 P 105 L 10 # 149  
 Yseboodt, Lennart Philips

Comment Type ER Comment Status X Editorial

Table 33-15a says in a Table note: "Any PD that is limited to Class 0-3 power levels may omit DLL support."

Next we have text that says (or should say, see other comment):

"Single-signature PDs not capable of drawing more than Class 3 power levels may omit Data Link Layer classification (see 33.6)."

Slightly different statement with the same effect, on the same page.

SuggestedRemedy

Remove the text on line 46-48.

Change Table 33-15a note to:

"Single-signature PDs not capable of drawing more than Class 3 power levels may omit Data Link Layer classification (see 33.6)."

Proposed Response Response Status W

Do we want to include this information as a note only?

TFTD

CI 33 SC 33.3.5 P 105 L 46 # 180  
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PD Class

"PD's of all Types not capable of drawing more than Class 3 power levels may omit Data Link Layer classification (see 33.6)."

Only true for SS PDs. DS PDs always need to support DLL + spell fix.

SuggestedRemedy

"Single-signature PDs not capable of drawing more than Class 3 power levels may omit Data Link Layer classification (see 33.6)."

Possibly OBE by previous comment. (149)

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 33 SC 33.3.5 P 105 L 46 # 269  
 Stover, David Linear Technology  
 Comment Type E Comment Status D Editorial  
 Typo  
 SuggestedRemedy  
 Replace "PD's" with "PDs"  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.  
 OBE by 180

CI 33 SC 33.3.5.2 P 106 L 48 # 98  
 Skinner, John Sifos Technologies, In  
 Comment Type E Comment Status D PD Class  
 The descriptive text includes "DO\_CLASS\_EV6", which is also shown in Figure 33-16. The state diagram in Figure 33.9d, and the related tables and text in subclause 33.2.6 only define five class events (CLASS\_EV5 the last).  
 There appears to be no use of, and therefore no need to describe a sixth class event in subclause 33.3.  
 SuggestedRemedy  
 Remove "DO\_CLASS\_EV6" from the paragraph at line 48, and remove the state "DO\_CLASS\_EVENT\_6" from Figure 33-16.  
 If this remedy is accepted, it will also be necessary to remove "DO\_CLASS\_EVENT6" from the third paragraph under 3.3.5.2.1, page 108, line 34.  
 Proposed Response Response Status W  
 PROPOSED REJECT.  
 The 6th class event state is used to define PD behavior for any class event greater than 5. It is needed, just as class event 3 was defined as part of AT. Defined behaviors make things much easier in case we need to add some more states later.

CI 33 SC 33.3.5.2 P 107 L 7 # 70  
 Johnson, Peter Sifos Technologies  
 Comment Type T Comment Status X PD Class  
 Per earlier comment to D1.2, I still see the state variable names "class\_sig\_A" and "class\_sig\_B" as asking for trouble and creating confusion with Dual-Signature PD classification.  
 Prior response was AIP but needing a better substitute.  
 SuggestedRemedy  
 Solution 1:  
 Change 'class\_sig\_A' to 'class\_sig\_init'  
 Change 'class\_sig\_B' to 'class\_sig\_final'  
 Solution 2 (picture the 2 and 3 events?):  
 Change 'class\_sig\_A' to 'class\_sig\_U'  
 Change 'class\_sig\_B' to 'class\_sig\_W'  
 Solution 3:  
 Change 'class\_sig\_A' to 'class\_sig\_m'  
 Change 'class\_sig\_B' to 'class\_sig\_n'  
 Change will require search and replace over 33.3 portions of document.  
 Proposed Response Response Status W  
 TFTD

CI 33 SC 33.3.5.2 P 107 L 45 # 121  
 Yseboodt, Lennart Philips  
 Comment Type T Comment Status X PD Class  
 "Dual-signature PDs may advertise a different Class signature on each pairset."  
 Do we really want to write this out in the standard ?  
 It adds significant complication as it has:  
 - unique behaviour / rules for continuous power  
 - power demotion very tricky  
 SuggestedRemedy  
 Remove this sentence.  
 We don't forbid DS/unequal classes, we simply do not specify it at all.  
 Proposed Response Response Status W  
 TFTD

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.3.5.2 P 108 L 18 # 122  
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD Class

Table 33-17, item 7 is Long first Class Event timing, Tlcf\_pd, with range 75.5 to 87.5 ms. Tlcf = 88 to 105 ms.

The minimum makes sense, the maximum does not.  
 This parameter determines the conditions where a PD is allowed to deem a class event as 'long'.  
 As soon as a class event exceeds 88ms (= Table 33-10 / T\_LCF).

Also see 33.3.8:  
 "Types 3 and 4 PDs which detect a long first Class event in the range of T LCF\_PD may ..."

*SuggestedRemedy*

Remove maximum.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

The text should read something like:

"The default value for short\_mps is FALSE. A PD may set short\_mps to TRUE if the first class finger is longer than Tlcf\_pd min. A PD shall set short\_mps to True if the first class finger is longer than Tlcf\_pd max."

Cl 33 SC 33.3.5.3 P 108 L 49 # 72  
 Johnson, Peter Sifos Technologies

Comment Type T Comment Status D Autoclass

The phrase "A PD implementing Autoclass shall remove its classification current at Tacs (as defined in Table 33-17a), resulting in a classification signature of '0' for the remainder of CLASS\_EV1." suggests 0mA class signature. This is inconsistent with 33.2.6.2 where it states "....lclass in the range of Class 0 after Tacs...".

So what is the actual requirement ? Class 0 or 0 mA ? (note this does have a 'shall' in it...)

Also, this requirement only has meaning if CLASS\_EV1 is an LCF. In the PSE State Diagram, that state is now CLASS\_EV1\_LCF. We should stipulate that this only happens given Type 3 or Type 4 PSE.

*SuggestedRemedy*

Alter the phrase to:

"When connected to a Type3 or Type 4 PSE, a PD implementing Autoclass shall present a Class 0 signature starting at Tacs (as defined in Table 33-17a) for the remainder of CLASS\_EV1\_LCF."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

See 53

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 33 SC 33.3.5.3 P 108 L 49-5 # 53  
 Darshan, Yair Microsemi  
 Comment Type TR Comment Status D Autoclass

The following text is not clear:  
 "A PD implementing Autoclass shall remove its classification current at TACS (as defined in Table 33-17a), resulting in a classification signature of '0' for the remainder of CLASS\_EV1. A PD implementing Autoclass carries out the rest of the Physical Layer classification as defined in section 33.3.5.1 or 33.3.5.2."

1. It says that the PD shall remove its classification current at TACS (table 33-17a) = 75.5msec to 87.5ms which is identical to the Long First Class event timing T\_LCF\_PD=75.5msec to 87.5msec (Table 33-17) resulting in a classification signature of '0' for FOR THE WHOLE periode of the class event and not only for the remainder of CLASS\_EV1.  
 So the "remiander of CLASS\_EV1" is incorrect to use. If TACS WAS < T\_LCF\_PD than it was OK.

The text:  
 "A PD implementing Autoclass carries out the rest of the Physical Layer classification as defined in section 33.3.5.1 or 33.3.5.2." may need further clarrrification by saying:  
 "A PD implementing Autoclass carries out the rest of the Physical Layer classification (\*\*the PD class response to the 2nd or more class events\*\*) as defined in section 33.3.5.1 or 33.3.5.2."

SuggestedRemedy

Group to clarify the questions of adopt the following remedy:  
 "A PD implementing Autoclass shall remove its classification current at TACS (as defined in Table 33-17a), resulting in a classification signature of '0' for the (Delete "remainder" \*\*duration\*\* of CLASS\_EV1).  
 A PD implementing Autoclass carries out the rest of the Physical Layer classification \*\*(the PD class response to rest of class events)\*\* as defined in section 33.3.5.1 or 33.3.5.2."  
 -----

Note: I am aware of the fact that it takes time to PD to remove class current so the time left with class 0 is less than CLASS\_EV1 so "remainder" may be OK to use but the whole thing is not so clear (what to do with the time when it is not class 0? etc.) but this is the best what I could suggest to start a discussion.

Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.

Change to:

"A PD implementing Autoclass shall respond to Physical Layer classification as specified in 33.3.5.1 and 33.3.5.2 with the exception that the PD shall change its classification signature during the first class event to '0' no earlier than TACS min and no later than

TACS max (as defined in Table 33-17a). "

CI 33 SC 33.3.5.3 P 109 L 1 # 182  
 Yseboodt, Lennart Philips  
 Comment Type TR Comment Status D Autoclass

"After power up, a PD implementing Autoclass shall draw its highest required power throughout the period bounded by ..."

This statement may lead the reader to believe that a PD using Autoclass is not subject to power demotion (which it is).

SuggestedRemedy

"After power up, a PD implementing Autoclass shall draw its highest required power, subject to the requirements on Pclass\_pd in 33.3.7.2, throughout the period bounded by ..."

Proposed Response Response Status W  
 PROPOSED ACCEPT.

CI 33 SC 33.3.5.3 P 109 L 1 # 73  
 Johnson, Peter Sifos Technologies  
 Comment Type T Comment Status D Autoclass

Current text is:

"After power up, a PD implementing Autoclass shall draw its highest required power throughout the period bounded by ..."

So what happens when a Type 3 or Type 4 PSE cannot support Pclass\_pd for this PD? Full loading by the PD during Autoclass will lead to power cycling with the PSE. Either the PD must restrict Autoclass load to its maximum power requirement GIVEN any particular power grant from the PSE (e.g. 13W, 25.5W, etc) or the Autoclass process needs to somehow abort.

SuggestedRemedy

Assuming the solution is that PD's must restrict Autoclass loads to PD's maximum power requirement \*GIVEN\* any particular power grant from the PSE:

"After power up, a PD implementing Autoclass shall draw its highest required power, in accordance with the pse\_power\_level resolved during classification, throughout the period bounded by ...."

Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.

OBE by 182.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.3.5.3 P 109 L 13 # 88  
 Skinner, John Sifos Technologies, In

Comment Type T Comment Status D Autoclass

Tacs Max 87.5ms as defined in Table 33-17a does not appear to provide sufficient margin for a PD that supports Autoclass to be correctly recognized by a PSE that supports Autoclass.

A PSE is allowed to terminate CLASS\_EV1\_LCF at Tlcf min 88ms (as defined in Table 33-10). If there is any timer inaccuracy between the PSE and PD, the 500usec margin afforded by Tacs max could lead to a case where a PDs autoclass capability will not be identified, even though that PD is changing the class signature within the specified time frame. (would admittedly be poor design practice, but conformant)

A conservative approach would be to reduce the value of Tacs Max in Table 33-17a, to provide adequate margin to account for any timer inaccuracy between the PSE and PD.

SuggestedRemedy

Change the value of Tacs Max in Table 33-17a, Item 1 to 85.5 ms.

Proposed Response Response Status W

PROPOSED REJECT.

This value was increased in D1.3 due to PD timing margin requirements. It is up to the PSE to check the PD class current before it ends the LCF. 88ms is a minimum. I imagine most PSEs will have a timer set for 95ms or so and then will check the class current and then transition to mark...

Cl 33 SC 33.3.5.3 P 108 L 50 # 189  
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Autoclass

"A PD implementing Autoclass shall remove its classification current at T ACS (as defined in Table 33-17a), resulting in a classification signature of '0' for the remainder of CLASS\_EV1."

Contradiction since classification signature of '0' is between 1mA and 4mA.

SuggestedRemedy

"A PD implementing Autoclass shall reduce its classification current at T ACS (as defined in Table 33-17a), resulting in a classification signature of '0' for the remainder of CLASS\_EV1."

Proposed Response Response Status W

See 53.

Cl 33 SC 33.3.6 P 109 L 30 # 123  
 Yseboodt, Lennart Philips

Comment Type T Comment Status D Mutual ID

"A PD shall identify a PSE Type as a Type lower or equal to its own Type"  
 "A PD connected to a higher PSE Type than its own may identify that PSE as its own Type."  
 What does this do ?  
 How can it be tested ?

SuggestedRemedy

Remove sentences ?

Proposed Response Response Status W

PROPOSED REJECT.

TFTD

This is part of mutual ID. It is clearly shown in the PD SD.

Cl 33 SC 33.3.7 P 112 L 1 # 240  
 Dwelley, David Linear Technology

Comment Type E Comment Status D PD Power

Note seems obsolete: item 4 no longer has values.

SuggestedRemedy

Strike this editor's note.

Proposed Response Response Status W

PROPOSED ACCEPT.

The value has been moved to Table 33-16a.

The note was there to remind us that we rounded up... I believe we are all ok with this.

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 33 SC 33.3.7.2 P 112 L 23 # 103  
 Bennett, Ken Sifos Technologies, In

Comment Type ER Comment Status X PD Power

It's not clear that the PClass\_PD limit in table 33-18 is determined by the Class assigned (or allocated) by the PSE. The suggested remedy adds a clarifying sentence to 33.3.7.2.

SuggestedRemedy

Add the following after the first sentence of 33.3.7.2:

PClass\_PD in table 33-18 is determined by the Class assigned by the PSE.

Proposed Response Response Status W

TFTD is this clarification is needed.

Cl 33 SC 33.3.7.3 P 113 L 4 # 21  
 Jones, Chad Cisco

Comment Type TR Comment Status X PD Inrush

This is a reminder of MR1277 that has been assigned to this TF for closure. Changes were previously made to close the MR and then subsequently further changes were made that may backed out the fix. This comment is being filed so that the TF can review the MR and ensure it is being properly addressed and to provide an Editor's Note warning of any future changes to the text.

MR 1277: "RATIONALE FOR REVISION:

PDs in the field turn on their DC-DC load during inrush. This leads to PD cap not charging up fully (even if PD cap is <180uf PSE is following inrush rules from Section 33.2.7.5). This may lead to operational problems after inrush. There is a Voff requirement in PD table 33-18 to ensure power supply remains turned off for V<30V, but customers seem to read this as applicable only "after power on" not during "power on" - hence ether turn on their DC-DC during inrush causing problems.

PROPOSED REVISION TEXT:

Request the following text be added as note to section 33.4.1

Add the following to section 33.3.7.3

"PDs shall not draw more than the maximum current allowed by a PSE during inrush as outlined in section 33.2.7.5" Change 2nd paragraph of Section 33.3.7.1 as follows (change shown in  ) "The PD shall not turn on until a voltage greater than Voff and less than or equal to Von"

SuggestedRemedy

Restore the text as it stood after D0p4. Also, add an Editor's Note to the end of the paragraph to be removed before publishing, "Editor's Note: this paragraph has changed as a result of MR1277. Do not change this paragraph without consulting the request of MR1277."

History:

D0p1:"Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with VPort\_PD requirements as defined in Table 33-17, and ending when CPort is charged to 99 % 13 of its final value. This period should be less than TInrush min per Table 33-10."

D0p4: "Inrush current per pair-set is drawn beginning with the application of input voltage at the pair-set compliant with Vport\_PD-2P requirements as defined in Table 33-18, and ending before TInrush-2P min per Table 33-11. After TInrush-2P min, the PD shall not exceed its per pair-set current threshold corresponding to its class level."

D1p3:"Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with Vport\_PD-2P requirements as defined in Table 33-16a, and ending when CPort has reached a steady state and is charged to 99% of its final value. This period shall be less than TInrush-2P min per Table 33-11. After TInrush-2P min, Class 6 or Class 8 PDs shall meet Pclass at the PSE PI; all other PDs shall meet PClass\_PD as specified in Table 33-18."

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*Proposed Response*      *Response Status* **W**

Chad to walk us through...

**Cl 33**      **SC 33.3.7.3**      **P 113**      **L 30**      # 150

Yseboodt, Lennart      Philips

*Comment Type* **ER**      *Comment Status* **X**      *PD Inrush*

original text: "See PSE-PD simplified Cport implementation model in Annex TBD."  
Do we really need an Annex to explain this implementation issue ?

BC:EYO

*SuggestedRemedy*

Remove this line.  
If it really needs explanation that cannot be done in 33.3.7.3 we should submit actual Annex contents.

*Proposed Response*      *Response Status* **W**

TFTD

**Cl 33**      **SC 33.3.7.9**      **P 118**      **L 46**      # 184

Yseboodt, Lennart      Philips

*Comment Type* **TR**      *Comment Status* **D**      *Unbalance*

Table 33-18a, item 4, PD Power has value "Set to maximum per its Class".  
How exactly can the PD power be set ? This is not a controllable parameter in most PDs.

*SuggestedRemedy*

Remove item 4, perhaps add to the text that the PD should be put in a mode where it consumes maximum power where applicable.

*Proposed Response*      *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Need appropriate text

**Cl 33**      **SC 33.3.8**      **P 119**      **L 27**      # 185

Yseboodt, Lennart      Philips

*Comment Type* **TR**      *Comment Status* **D**      *MPS*

"In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI."

This language prohibits NOT showing MPS if the goal is to become unpowered.

*SuggestedRemedy*

"A PD that requires power from the PI shall provide a valid Maintain Power Signature (MPS) at the PI."

This makes the 'shall' conditional upon needing power or not.

*Proposed Response*      *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

That is legacy text. I agree that your suggestion is better. Do we want to change it?

There is text later in the section that

**Cl 33**      **SC 33.3.8**      **P 119**      **L 41**      # 186

Yseboodt, Lennart      Philips

*Comment Type* **TR**      *Comment Status* **D**      *MPS*

"PDs using Autoclass shall use the I port\_MPS associated with the PD Class advertised during Physical Layer classification."

The PSE MPS rules are determined by the Class assigned to the PD, not what it advertized.

Example: A Class 5/Autoclass PD, that gets power demoted to Class 4, gets to use Class 4 MPS rules.

*SuggestedRemedy*

"PDs using Autoclass shall use the I port\_MPS associated with the PD Class assigned by the PSE during Physical Layer classification."

*Proposed Response*      *Response Status* **W**

PROPOSED ACCEPT.

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Cl 33 SC 33.3.8 P 119 L 44 # 151  
 Yseboodt, Lennart Philips  
 Comment Type ER Comment Status D Editorial  
 "Editor's Note: To add line for Type 1 and Type 2 dual-signature."  
 I don't think we want to describe the behaviour of Type 1/Type 2 dual-signature.  
 SuggestedRemedy  
 Remove editors note.  
 Proposed Response Response Status W  
 PROPOSED ACCEPT.

Cl 33 SC 33.3.8 P 119 L 44 # 241  
 Dwelley, David Linear Technology  
 Comment Type ER Comment Status D Editorial  
 "Editor's Note: To add line for Type 1 and Type 2 dual-signature." Such PDs do not officially exist and must meet the same specs as T1/2 SS PDs.  
 SuggestedRemedy  
 Strike this editor's note.  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.  
 OBE by 151.

Cl 33 SC 33.3.8 P 119 L 50 # 152  
 Yseboodt, Lennart Philips  
 Comment Type ER Comment Status D MPS  
 "A PD that does not maintain the MPS components mentioned above may have its power removed..."  
 Reference by relative physical location in the draft probably a bad idea.  
 SuggestedRemedy  
 "A PD that does not maintain the MPS components in section 33.3.8 may have its power removed..."  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.  
 This is section 33.3.8 so I don't like the self reference.  
 How about moving sentence to line end of paragraph on line 31 and changing it to:  
 "A PD that does not maintain these MPS components may have its power removed..."

Cl 33 SC 33.4.4 P 125 L 8 # 19  
 Zimmerman, George CME Consulting, Inc.  
 Comment Type TR Comment Status D AES  
 "For 10GBASE-T systems, TBD mV peak, for 1 MHz to 500 MHz."  
 Need to fill in a number. Initial analysis of 35-40dB common mode to differential mode conversion magnetics suggests that 50mVpp (same as 100 and 1000BASE-T) would be about right. Phy developers are asking to mark with a TBD for now.  
 SuggestedRemedy  
 change "TBD mV peak" to "50 mVpp (TBD)"  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.

See 42

Cl 33 SC 33.4.4 P 125 L 8 # 42  
 Darshan, Yair Microsemi  
 Comment Type T Comment Status D AES  
 Replace TBD with:  
 50 mV peak from 1MHz to 100MHz and 20 mV peak from > 1MHz and up to 500MHz.  
 SuggestedRemedy  
 Replace TBD with:  
 50 mV peak from 1MHz to 100MHz and 20 mV peak from > 100MHz and up to 500MHz.  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.  
 See 19  
 Where did these numbers come from?

Cl 33 SC 33.4.9.1.4 P 113 L 16 # 23  
 Maguire, Valerie Siemon  
 Comment Type T Comment Status X Cabling  
 Not sure if this is in scope, but Category 5 cord requirements do not reside in ANSI/TIA-568-C.2  
 SuggestedRemedy  
 Replace "ANSI/TIA-568-C.2" with "ANSI/TIA/EIA-568-A:1995"  
 Proposed Response Response Status W  
 Chair, is this in scope?

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Cl 33 SC 33.5.1.2 P 138 L 40 # 9  
 Zimmerman, George CME Consulting, Inc.  
 Comment Type TR Comment Status D Management

Need to allocate classes 5 through 8 and autoclass.

SuggestedRemedy

replace "101 Invalid Class" with "101 Class 5"  
 replace "110 Reserved" with "110 Class 6"  
 replace "111 Reserved" with "111 Class 7"  
 add after table - "Editor's Note (to be removed before Working Group ballot) - Status register bits are used up, and clause 22 address space is used up as well. Contributions requested as to how to expand status, at a minimum to report Class 8 PD and Autoclass"

In 33.5.1.2.10, delete P140 L36: "The combinations '110' and '111' for bits 12.6:4 have been reserved for future use."

Proposed Response Response Status W  
 PROPOSED ACCEPT.

Cl 33 SC 33.6 P 141 L 11 # 187  
 Yseboodt, Lennart Philips  
 Comment Type TR Comment Status D DLL

"Type 2, Type 3 and Type 4 PDs that require more than 13.0 W support Data Link Layer classification (see 33.3.5).  
 Data Link Layer classification is optional for all other devices."

Dual-signature PDs must support DLL regardless of power consumption.

SuggestedRemedy

"Type 2, Type 3 and Type 4 PDs that require more than Class 3 power levels, or Type 3/DS and Type 4/DS PDs support Data Link Layer classification (see 33.3.5). Data Link Layer classification is optional for all other devices."

Proposed Response Response Status W  
 PROPOSED ACCEPT.

Cl 33 SC 33.6.3.1 P 142 L 14 # 258  
 Schindler, Fred Seen Simply  
 Comment Type ER Comment Status X DLL

Clarify values used for PD\_DLL\_MAX\_VALUE, PD\_INITIAL\_VALUE, and PSE\_INITIAL\_VALUE.

SuggestedRemedy

After the variable PSE\_INITIAL\_VALUE description (line 3 on page 143) add, "Variables PD\_DLL\_MAX\_VALUE, PD\_INITIAL\_VALUE, and PSE\_INITIAL\_VALUE, round up values to provide margin. Additional information on power levels for classes 6 and 8 may be found at 33.3.7.2."

Proposed Response Response Status W  
 Im not sure I follow.

Cl 33 SC 33.6.3.2 P 142 L 53 # 105  
 Bennett, Ken Sifos Technologies, In  
 Comment Type TR Comment Status X DLL

PSE\_INITIAL\_VALUE settings for Class 6 and Class 8 are currently the extended-power limits. A range should be used for these so that non-extended values can be used.

SuggestedRemedy

Change "600" to "<= 600"  
 Change "900" to "<= 900"

Proposed Response Response Status W  
 TFTD

Cl 33 SC 33.6.3.5 P 147 L 12 # 226  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Management

Just observing that pse\_dll\_enabled not required on this arc? Is it possible that pse\_dll\_ready can be true while pse\_dll\_enabled is false?

SuggestedRemedy

address as appropriate.

Proposed Response Response Status W  
 I'm not sure what arc you are referring to.

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CI 33 SC 33.6.3.5 P 147 L 12 # 227  
 Dove, Daniel Dove Networking Solut  
 Comment Type TR Comment Status X Management  
 Just observing that pd\_dll\_enabled not required on this arc? Is it possible that pd\_dll\_ready can be true while pd\_dll\_enabled is false?  
 SuggestedRemedy  
 address as appropriate.  
 Proposed Response Response Status W  
 I'm not sure what arc you are referring to.

CI 33 SC 33.8.3.5 P 165 L 18 # 22  
 Maguire, Valerie Siemon  
 Comment Type T Comment Status X Cabling  
 Not sure if this is in scope, but Category 5 cord requirements do not reside in ANSI/TIA-568-C.2  
 SuggestedRemedy  
 Replace "ANSI/TIA-568-C.2" with "ANSI/TIA/EIA-568-A:1995"  
 Proposed Response Response Status W  
 Chair, is this in scope?

CI 33 SC 33A.5 P 172 L 10 # 34  
 Darshan, Yair Microsemi  
 Comment Type T Comment Status X Pres: Darshan1  
 Updating Annex 33A.5 due to the following changes made for D1.2:  
 1. Increasing PSE Vdiff to 10mV instead of 2mV.  
 In addition, the following changes we made for Type 3 system:  
 2. Increasing system Vdiff for Type 3 to 70mV instead of 60mV to increase margins.  
 3. Type 4 systems stayed total 60mV vdiff:  
 SuggestedRemedy  
 Update Annex 33A.5 per darshan\_01\_1015.pdf page 9.  
 Proposed Response Response Status W  
 Wait for presentation

CI 33 SC Annex 33B P 173 L 43 # 35  
 Darshan, Yair Microsemi  
 Comment Type T Comment Status X Pres: Darshan1  
 Updating Annex 33B Table 33B-1 due to the following changes made for D1.2:  
 1. Increasing PSE Vdiff to 10mV instead of 2mV.  
 In addition, the following changes we made for Type 3 system:  
 2. Increasing system Vdiff for Type 3 to 70mV instead of 60mV to increase margins.  
 3. Type 4 systems stayed total 60mV vdiff:  
 SuggestedRemedy  
 Update Table 33B-1 per darshan\_01\_1015.pdf page 10.

Proposed Response Response Status W  
 Wait for presentation

CI 33A SC 33A.3 P 171 L 13 # 1  
 Zimmerman, George CME Consulting, Inc.  
 Comment Type TR Comment Status X Annex  
 "Operation for all types requires that the resistance unbalance shall be 3% or less."  
 Informative text cannot have requirements - no "shall" or "must" statements.  
 SuggestedRemedy  
 Replace "shall" with "should" in the above sentence.

Proposed Response Response Status W  
 Is this an informative annex?

CI 33A SC 33A.5 P 172 L 10 # 5  
 Zimmerman, George CME Consulting, Inc.  
 Comment Type T Comment Status D Annex  
 "Rpair\_max\_PD" and "Rpair\_min\_PD"  
 Rpair\_max and Rpair\_min were defined twice before (pages 107 and 141) in terms of the PSE. This is the only place Rpair\_max\_PD (or min) occur in the draft. Even though its a guideline, it needs a definition.  
 SuggestedRemedy  
 Define Rpair\_max\_PD, Rpair\_min\_PD. in 33A.5. (sorry, I really don't know what is the intended definition).  
 Proposed Response Response Status W  
 PROPOSED ACCEPT IN PRINCIPLE.

Need definition, Yair?

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CI **33B** SC **33B** P **173** L **1** # **3**  
 Zimmerman, George CME Consulting, Inc.

Comment Type **T** Comment Status **X** Annex

Perhaps we moved too much to the annex. Annex 33B (normative) appears to contain new requirements on PSEs that are not in the main body of Clause 33. The use of normative annexes, per the IEEE style guide is: "for conformance test procedures, tables, or printed source code. Normative annexes may also be used for context-specific applications of the standard."

The key requirement references Equation 33-4b in 3.2.7.4.1, but it seems that Table 33B-1 is a set of additional requirements, perhaps in conflict with the main body of the text.

A lot of what is in this annex appears to be test procedures, but the main requirement seems to be here too, and maybe should be in the body of clause 33.

*Suggested Remedy*

Move page 173, lines 16 - 52 ("Equation (33-4b)..." through "attached to PSE PI." to the end of 33.2.7.4.1 page 85, line 17.

Proposed Response Response Status **W**

TFTD

CI **79** SC **79.3.2** P **9** L **27** # **87**  
 Skinner, John Sifos Technologies, In

Comment Type **TR** Comment Status **X** TLV

Draft P802.3/D1.3 contains a modified Figure 79-3-Power Via MDI TLV format. This same figure designation was used in the 802.3at specification to define the Power Via MDI TLV format. Modifying Figure 79-3 is invalid, as it would therefore modify the specification of how the Power Via MDI TLV (in use today by Type 2 PSEs and PDs that conform to 802.3at) is formatted.

(There should be no expectation that existing parsers will recognize the new format, as the length field is the ONLY distinguishing characteristic that is now used to determine whether the received TLV is the old form defined by 802.1AB or the new form defined by 802.3at. This new form will indicate a different length, forcing newer parsers to handle 3 possible formats...).

The existing figure could be altered in such a way as to show the existing 12 octet version, and the extensions for the new (currently 22 byte) version. However, this would lead to an overly complicated figure. It would be much clearer to use a separate figure to describe the (extended, revised) TLV.

*Suggested Remedy*

Remove the edits from "Figure 79-3-Power Via MDI TLV format", restoring it to the same figure as originally published in 802.3at.

Add a new figure, titled "Figure 79-3a-Power Via MDI TLV extended format", at the top of page 10, to document the new 22 octet form of the Power Via MDI TLV.

Modify the existing last two sentences in the explanatory paragraph located between lines 32 and 33 on page 9, which read:

"This TLV is also required to perform Data Link Layer classification as defined in 33.6. Figure 79-3 shows the format of this TLV."

to this statement:

"This TLV is also required to perform Data Link Layer classification as defined in 33.6. The format of the TLV to be used to perform Data Link Layer classification by Type 2 PSEs and PDs is shown in Figure 79-3. The format of the TLV to be used to perform Data Link Layer classification by Type 3 and Type 4 PSEs and PDs is shown in Figure 79-3a."

Proposed Response Response Status **W**

TFTD

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

CI 79 SC 79.3.2 P 9 L 53 # 86  
 Skinner, John Sifos Technologies, In

Comment Type ER Comment Status D TLV

In Figure 79-3-Power Via MDI TLV format, the TLV information string length field states "TLV information string length = 14". This does not account for the additional fields "PD measurements" and "PSE Measurements", which are each 4 octets in length (therefore 8 octets total).

*SuggestedRemedy*

Correct the TLV information string length in Figure 79-3-Power Via MDI TLV format to indicate "...length = 22".

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 79 SC 79.3.2 P 10 L 3 # 89  
 Skinner, John Sifos Technologies, In

Comment Type ER Comment Status X TLV

There is an explanatory paragraph at the top of Page 10 that describes the revisions made to the legacy Power via MDI TLV originally defined by 802.1AB.

As the 802.3bt specification is again revising the Power via MDI TLV (most recently revised by and defined in 802.3at), an additional explanatory paragraph is warranted to describe the extensions that are being added to support Type 3 and Type 4 devices.

*SuggestedRemedy*

Add the following sentence to the end of the paragraph on Page 10, line 10:

"The TLV shown in Figure 79-3 has been and will continue to be used by Type 2 power entities."

Insert the following paragraphs after line 11, before the heading '79.3.2.1 MDI power support':

"The TLV shown in Figure 79-3a is a revision of the Power Via MDI TLV originally defined in 802.3at-2009 clause 79.3.2, and defines an extended format which includes additional fields that shall be used by Type 3 and Type 4 power entities.

In order to support Type 2 PDs, Type 3 and Type 4 PSEs will need to be able to recognize the TLV shown in Figure 79-3, as well as the TLV shown in Figure 79-3a. Per 79.3.2.7, only one format TLV should be present in an LLDPDU."

[NOTE that the figure reference in this remedy is related to acceptance of the comment that requires that a new figure titled "Figure 79-3a-Power Via MDI TLV extended format" be added to 79.3.2.]

Proposed Response Response Status W

TFTD

IEEE P802.3bt D1.3 4-Pair PoE 6th Task Force review comments

Cl 79 SC 79.3.2.2 P 10 L 44 # 90  
 Skinner, John Sifos Technologies, In

Comment Type E Comment Status D TLV

IETF RFC 3621 pethPsePortPowerPairs only defines "signal(1)" and "spare(2)". There is no allowance for other integer values (for example, 0 indicating unknown, or 3 indicating both pairs).

*SuggestedRemedy*

Add sentence at the end of the existing paragraph that is located on lines 43 and 44:

"Type 3 or Type 4 PSEs that are furnishing power on a single pairset shall use the value that defines that pairset (signal=Alternative A, spare=Alternative B). Either pairset may be indicated when furnishing power on both pairsets, as that condition is communicated by the PSE power status value field defined in 79.3.2.6a."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 79 SC 79.3.2.5 P 12 L 14 # 91  
 Skinner, John Sifos Technologies, In

Comment Type T Comment Status D TLV

The valid values for the requested power value field in Table 79-5 have been changed from "decimal 1 through 255" to "decimal 1 through 999".

This field as defined for use by Type 2 power entities was the range "decimal 1 through 255". Values greater than 255 are not valid for pre-existing Type 2 implementations.

*SuggestedRemedy*

Change the statement in the Value/meaning column of Table 79-5 to:

"Valid value for these bits are decimal 1 through 255 for Type 2 PDs, and decimal 1 through 999 for Type 3 and Type 4 PDs."

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 79 SC 79.3.2.6 P 12 L 38 # 92  
 Skinner, John Sifos Technologies, In

Comment Type T Comment Status D TLV

The valid values for the requested power value field in Table 79-6 have been changed from "decimal 1 through 255" to "decimal 1 through 999".

This field as defined for use by Type 2 power entities was the range "decimal 1 through 255". Values greater than 255 are not valid for pre-existing Type 2 implementations.

*SuggestedRemedy*

Change the statement in the Value/meaning column of Table 79-6 to:

"Valid value for these bits are decimal 1 through 255 for Type 2 PSEs, and decimal 1 through 999 for Type 3 and Type 4 PSEs. When a Type 3 or Type 4 is furnishing power to a Type 2 PD, the valid values will be limited to the Type 2 range, decimal 1 to 255."

Proposed Response Response Status W

PROPOSED ACCEPT.