Cl **1** *SC* **1.4** *P* **20** *L* **32** # 26

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *Editorial*

"Dual-signature PD: A property of a PD where it shares the same detection signature, classification signature, and maintain power signature between both pairsets (see IEEE 802.3, Clause 33)."

'A property of a PD where it'... Feels like a strange construction to say this.

SuggestedRemedy

"Dual-signature: A property of a PD that has independent detection signatures, classification signatures, and maintain power signatures on each pairset."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

New wording would be nice but your suggested remedy is worse (in my opinion).

How does a property (of a PD) have independent signatures?

Cl **1** *SC* **1.4** *P* **20** *L* **32** # 25

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *Editorial*

"Single-signature PD: A property of a PD where it shares the same detection signature, classification signature, and maintain power signature between both pairsets (see IEEE 802.3, Clause 33)."

'A property of a PD where it'... Feels like a strange construction to say this.

SuggestedRemedy

"Single-signature: A property of a PD that shares the same detection signature, classification signature, and maintain power signature between both pairsets (see IEEE 802.3, Clause 33)."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See 26.

Cl **1** *SC* **4** *P* **20** *L* **39** # 190

Lukacs, Miklos Silicon Labs

Comment Type **TR** *Comment Status* **D** *Definitions*

the term 'mode' - as a synonym for pairset - is not definet yet

SuggestedRemedy

Replace 'modes' with 'pairsets'

Proposed Response *Response Status* **W**

PROPOSED REJECT.

There is a reference in the definition to see clause 33. The reader will find a definition of mode near the beginning of the PD section.

Cl **1** *SC* **1.4** *P* **20** *L* **46** # 191

Lukacs, Miklos Silicon Labs

Comment Type **TR** *Comment Status* **D** *Definitions*

The term 'mode' - as a synonym for pairset - is not definet yet.

SuggestedRemedy

Replace 'Modes' with 'pairsets'

Proposed Response *Response Status* **W**

PROPOSED REJECT.

There is a reference in the definition to see clause 33. The reader will find a definition of mode near the beginning of the PD section.

Cl **25** *SC* **25.4.5** *P* **24** *L* **3** # 27

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Editorial*

"A 100BASE-TX transmitter in a Type 2 or greater Endpoint PSE or Type 2 or greater PD delivering or accepting more than 13.0 W average power shall meet either the..."

Refer to Class rather than power.

SuggestedRemedy

"A 100BASE-TX transmitter in a Type 2 or greater Endpoint PSE or Type 2 or greater PD delivering or accepting more than Class 3 average power shall meet either the..."

Proposed Response *Response Status* **W**

Should we put a pointer in for where class 3 is defined (as this is clause 25).

TFTD

Cl **25** *SC* **25.4.10** *P* **27** *L* **33** # 168

Maguire, Valerie Siemon

Comment Type **T** *Comment Status* **X** *Cabling*

I believe that "STP" used in this context refers to 150 ohm Type 1 cable (as opposed to shielded 100 ohm balanced twisted-pair cable). To avoid confusion, text should be revised as shown below.

SuggestedRemedy

Line 33:

Replace "STP" with "150 ohm Type 1 STP"

Line 34:

Replace: "(for both UTP and STP)" with (for both balanced twisted-pair and 150 ohm Type 1 STP")

Proposed Response *Response Status* **W**

Why are we editing this section? We haven't touched it yet.

Cl **33** *SC* **33.2** *P* **48** *L* **1** # 187

Lukacs, Miklos Silicon Labs

Comment Type **TR** *Comment Status* **D** *Editorial*

The location and structure of this paragraph is confusing:
"An unplugged link section is one instance when power is no longer required. In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD."

The classification requirement should be included into the PSE functions list at the previous page.

SuggestedRemedy

Add the following bullet to the PSE functions list on page 47 as a second bullet:
- to execute power classification mechanism to determine the power needs of the PD.

Remove the sentence from page 48 line 2 "In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is all legacy text. I believe the reason it does not mention classification in the bulleted list is that Type 1 PSEs were not required to do classification.

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **16** # 188

Lukacs, Miklos Silicon Labs

Comment Type **TR** *Comment Status* **D** *Pres: PSE SD*

CC_DET_SEQ possible value of 3 is not defined in 33.2.4.3 Constants on page 59

SuggestedRemedy

define CC_DET_SEQ value = 3 in 33.2.4.3 Constants on page 59

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Wfp

Cl **33** *SC* **33** *P* **43** *L* **1** # 102

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Editorial*

Clause 33 has become very complicated. See presentation to start a new Clause.

SuggestedRemedy

See yseboodt_1_1115_newclause_v1xx.pdf

Editor to:
- Implement all comments on D1.4 into D1.5 as intermediate draft.
- Create a new Clause (133?) and copy the contents of D1.5 Clause 33 into it, retaining only the text that describes Type 3 and Type 4 behavior. This becomes D1.6 against which we will comment.
- Restore Clause 33 from latest maintenance project (but implement pending MRs)

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.1.4** *P* **46** *L* **40** # 170

Stover, David — Linear Technology Cor

Comment Type **E** *Comment Status* **D** *Unbalance*

A consequence of redefining Table 33-1, "System power parameters Vs Maximum PSE Class" as a function of class and not Type, Note 2 (regarding pair-to-pair system resistance unbalance of T3/T4 PSEs) now applies to all four system power limit entries.

SuggestedRemedy

Apply Note 2 ("In Type 3 and Type 4 operation, the current per pairset will be impacted by pair-to-pair system resistance unbalance. See section 33.2.7.4.1") to Icable for "Class 0 to 3" and "Class 4" entries.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Yes, the note does apply since it says "the current per pairset will be impacted…"

However, we have agreed that class 0-4 PDs have no unbalance restrictions and PSEs must be able to supply the entire current over one pairset. Thus, the "Nominal Highest Current per pair (Icable, A)" is still 0.350 for Class 0 to 3 and 0.6 for Class 4. it will never be higher than that (as it is 100% unbalance) which is the true purpose of the note. Maybe the note should be reworded?

Cl **33** *SC* **33.1.4** *P* **46** *L* **44** # 106

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **X** *Editorial*

"I Cable is the current on one twisted pair in the multi-twisted pair cable."
Confusing. Are we twisting multiple times?

SuggestedRemedy

"I Cable is the current on one twisted pair in the twisted pair cable."

Proposed Response *Response Status* **W**

This is existing text. Do we want to change it? I understand the the desire to point out that there are multiple twisted pairs in the cable and this is the current on one of them.

Cl **33** *SC* **33.2.4.1** *P* **58** *L* **5** # 109

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **D** *Editorial*

D1.3:
Detection, classification, and power turn-on timing shall meet the specifications in Table 33-4, Table 33-10, and Table 33-11.

D1.4:
Connection Check timing requirements are specified in Table 33-3a.
Detection timing requirements are specified in Table 33-4.
Classification timing requirements are specified in Table 33-10.
Autoclass timing requirements are specified in Table 33-10a.
Power turn-on timing requirements are specified in Table 33-11.

Comment #58 changed this but also removed the word 'shall'.
Was that shall redundant ?

SuggestedRemedy

If yes: no action needed.
If no:
Connection Check timing shall meet the requirements as specified in Table 33-3a.
Detection timing shall meet the requirements as specified in Table 33-4.
Classification timing shall meet the requirements as specified in Table 33-10.
Autoclass timing shall meet the requirements as specified in Table 33-10a.
Power turn-on timing shall meet the requirements are specified in Table 33-11.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The shall was reduntant because all of those tables have shalls associated with them.

No changes result from accepting this comment

Cl **33** *SC* **33.2.4.6** *P* **69** *L* **34** # 215

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *Types*

The text may be improved to better deal with new PSE Types and to take into account power demotion.

Existing text,
"set_parameter_type
This function is used by a Type 2, Type 3 and Type 4 PSE to evaluate the type of PD connected to the link based on Physical Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements defined in Table 33-11 are set to values corresponding to either a Type 1, or Type 2, Type 3, or Type 4 PSE. This function returns the following variable:

parameter_type: A variable used by a Type 2, Type 3 or Type 4 PSE to pick between Type 1, and Type 2, Type 3 and Type 4 PI electrical requirement parameter values defined in Table 33-11.
Values: 1: Type 1 PSE parameter values (default)
2: Type 2 PSE parameter values
3: Type 3 PSE parameter values
4: Type 4 PSE parameter values

When a Type 2 PSE powers a Type 2, Type 3 or Type 4 PD, the PSE may choose to assign a value
of '1' to parameter_type if mutual identification is not complete (see 33.2.6) and shall assign a
value of '2' to parameter_type if mutual identification is complete.

Editor's Note: This paragraph requires further study."

SuggestedRemedy

Replace the existing sentence, "When a Type 2 PSE powers …" with
"When a PSE of Type greater than Type-1 powers a Type 2, Type 3 or Type 4 PD, the PSE may choose to assign a value of '1' to parameter_type if mutual identification is not completed (see 33.2.6) and shall assign a value corresponding to a Type that is capable of providing the negotiated power to parameter_type if mutual identification is complete."

Strike the Editor's note referenced above.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **6** # 210

Schindler, Fred — Seen Simply

Comment Type **ER** *Comment Status* **D** *PSE SD*

The entry condition to TEST_MODE checks for a current fault before applying power. A current fault is not possible without power. The state diagram is broken if this case needs to be checked.

SuggestedRemedy

Remove the checks for current faults for the TEST_MODE entry path.
Existing text that should be removed,
"!(ovld_det_a + short_det_a) * !(ovld_det_b + short_det_b)"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **6** # 208

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE SD*

The second entry path into IDLE has a typo.

Existing condition is,

Pse_reset + error_condition * (mr_pse_enable = enable)

SuggestedRemedy

Replace the error condition with,
"Pse_reset + !error_condition * (mr_pse_enable = enable)"

,which checks that no error_condition exists.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

I'm not sure that is the intention. That would leave a logic statement that says "the PSE is reset OR we don't have an error AND the PSE is enabled."

That doesn't make sense. It would force us back to IDLE any time that we don't have an error and the PSE is enabled.

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **6** # 225

Dove, Daniel — Dove Networking Solut

Comment Type **T** *Comment Status* **X** *PSE SD*

The "DISABLED" state has no value other than its name. The logic performed in this state is repeated in the IDLE state which follows immediately.

SuggestedRemedy

One could add "+ mr_pse_enable = disable" to the IDLE state entry logic and eliminate this state.

Proposed Response *Response Status* **W**

TFTD.

This is a direct extension of how the Type 1/2 state diagram handled this.

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **6** # 228

Dove, Daniel — Dove Networking Solut

Comment Type **TR** *Comment Status* **D** *Pres: Dove1*

During the Catania meeting, it was observed that the state diagram has an excessive number of intrapage connectors. This creates a more confusing drawing than necessary.

SuggestedRemedy

A proposal to fix this will be given in presentation dove_01_3bt_1115.pdf

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **6** # 227

Dove, Daniel — Dove Networking Solut

Comment Type **TR** *Comment Status* **X** *Pres: Dove1*

During the Catania meeting, it was observed that the state diagram was going through two separate sequences at the same time.

SuggestedRemedy

A proposal to fix this will be given in presentation dove_01_3bt_1115.pdf Additional flags/variables will be required to properly trigger/return from the dual-signature detection state diagrams.

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **6** # 226

Dove, Daniel — Dove Networking Solut

Comment Type **TR** *Comment Status* **X** *Pres: Dove1*

There are a number of variables used within the state diagram that are either not initialized, or not assigned in sequence with the state diagram. This allows one to potentially change the value of a variable asynchronously with the state diagram, and could cause unanticipated behavior. Example, mr_pse_alternative should be defined in the IDLE state and changes to 11.3:2 should not affect SD operation outside that state.

SuggestedRemedy

I will provide a presentation dove_01_3bt_1115.pdf on the addition of some of these variables, but here is my list.
mr_pse_alternative <= reg 11.3:2
Alt_Pref <=User_Defined
PI_SM <= False
Alt_X_Done <= False
Alt_Y_Done <= False

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **6** # 214

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE SD*

No exit from TEST_MODE is provided for mr_pse_enable being set to disable.

SuggestedRemedy

For all existing exit conditions for TEST_MODE, TEST_ERROR_A, and TEST_ERROR_B, replace the existing condition check, "mr_pse_enable = enable" with "(mr_pse_enable = enable) + (mr_pse_enable = disable)".

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Doesn't the global "mr_pse_enable = disable" entry into the DISABLED state take care of this?

Cl **33** *SC* **33.2.4.7** *P* **72** *L* **23** # 171

Stover, David — Linear Technology Cor

Comment Type **E** *Comment Status* **D** *PSE SD*

Arc from START_CXN_CHK to CXN_CHK_EVAL has transition logic "do_cxn_chk_done * (tcc_timer > tcc_min)" tcc_min is undefined.

SuggestedRemedy

Define tcc_min

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Need specific suggested remedy.

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **6** # 212

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **X** *PSE SD*

The processing within POWER_ON checks for one-pairset powering and forces ALT-A to be used. Then the processing checks what ALT should be enabled. These steps have already been done in state POWER_UP.

SuggestedRemedy

Delete all steps within POWER_ON.

This keeps the power already applied on.

Note that the Task Force should discuss whether PDs are permitted to change whether they are dll_4PID capable. If this is allowed, then this block correction needs to be redone.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **7** # 219

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **X** *PSE SD*

During the State Diagram ad hoc the Task Force needs to discuss processing faults on PSE Modes separately. For example, the Ted timer needs to be considered for each Modes so that one Mode could be okay while the other Mode may have a Ted delay to process.

The same method used for selecting the preferred Mode of the PSE may be used for selecting the variable to be processed.

SuggestedRemedy

If the Task Force does not resolve processing these situations. Add an Editor's note to this section.

Editor's Note: The PSE SD needs to process faults on each Mode using a unique variables for each Mode. For example, Ted_A and Ted_B.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **13** # 229

Dove, Daniel — Dove Networking Solut

Comment Type **TR** *Comment Status* **X** *Pres: Dove1*

There are a few issues with the logic in the POWER_UP state.
1) I find no way for a sig_type=dual to ever enter this state, so having logic asking for sig_type=single is a wasted logic term.
2) Since DLL has not been enabled yet, there is no way that dll_4PID=1 to occur in this state.
3) A simpler logic can be used to perform the necessary POWER_UP.

SuggestedRemedy

A proposal to fix this will be given in presentation dove_01_3bt_1115.pdf

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **14** # 18

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PSE SD*

Dual Signature is not adressed in POWER_UP state
IF (mr_pse_alternative = a) THEN
alt_a_pwrd <= TRUE
IF (mr_pse_alternative = b) THEN
alt_b_pwrd <= TRUE
IF (((sig_type = single) + (dll_4PID = 1)) *
(mr_pse_alternative = both)) THEN
alt_a_pwrd <= TRUE
alt_b_pwrd <= TRUE

SuggestedRemedy

Add Editor Note after Figure 33-9a:
Editor's Note: To adress dual signature PD in POWER_UP state.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Power up of dual signature is taken care of by power_up[A] and power_up[B] on pages 76 and 78.

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **14** # 17

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X**

Clause 33.2.4.7 Figure 33-9a page 74 line 14:
In the POWER_UP state, the physical layer 4PID confirmation is missing.
IF (((sig_type = single) + (dll_4PID = 1)) *(mr_pse_alternative = both)) THEN

SuggestedRemedy

Change from:
IF (((sig_type = single) + (dll_4PID = 1)) *(mr_pse_alternative = both)) THEN
To:
IF (((sig_type = single) + (dll_4PID = 1)+(pd_cls_4PID=TRUE)) *(mr_pse_alternative = both)) THEN

Proposed Response *Response Status* **W**

Where did "pd_cls_4PID" come from?

TFTD.

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **26** # 230

Dove, Daniel Dove Networking Solut

Comment Type **TR** *Comment Status* **X** *Pres: Dove1*

There are a few issues with the logic in the POWER_ON state.
1) I find no way for a sig_type=dual to ever enter this state, so having logic asking for sig_type=single is a wasted logic term.
2) Since DLL has not been enabled on initial entry into this state, a 4-pair PSE will be forced to power-down alt-B after having powered it up. This makes no sense and creates a disruptive behavior. Correct behavior would be to allow the PSE to continue powering alt-B if mr_pse_alternative=both.
3) A simpler logic can be used to perform the necessary POWER_ON logic.

SuggestedRemedy

A proposal to fix this will be given in presentation dove_01_3bt_1115.pdf

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **27** # 19

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PSE SD*

Dual Signature is not adressed in POWER_ON state

IF (sig_type = single) THEN
IF ((dll_4PID = 0) +
(mr_pse_ss_mode = 0)) THEN
alt_a_pwrd <= TRUE
alt_b_pwrd <= FALSE
ELSE
IF (mr_pse_alternative = both) THEN
alt_a_pwrd <= TRUE
alt_b_pwrd <= TRUE
IF (mr_pse_alternative = a) THEN
alt_a_pwrd <= TRUE
IF (mr_pse_alternative = b) THEN
alt_b_pwrd <= TRUE

SuggestedRemedy

Add Editor Note after Figure 33-9a:
Editor's Note: To adress dual signature PD in POWER_ON state.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Power up of dual signature is taken care of by power_on[A] and power_on[B] on pages 76 and 78.

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **27** # 20

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *PSE SD*

Clause 33.2.4.7 Figure 33-9a page 74 line 27:
1.In the POWER_ON state, the physical layer 4PID part is missing.
2.The other case were
"alt_a_pwrd <= FALSE
alt_b_pwrd <= TRUE" is not covered.

"IF (sig_type = single) THEN
IF ((dll_4PID = 0) + (mr_pse_ss_mode = 0)) THEN
alt_a_pwrd <= TRUE
alt_b_pwrd <= FALSE
ELSE.."

SuggestedRemedy

1. Change from
"IF (sig_type = single) THEN
IF ((dll_4PID = 0) + (mr_pse_ss_mode = 0)) THEN
alt_a_pwrd <= TRUE
alt_b_pwrd <= FALSE
ELSE..":

To:
"IF (sig_type = single) THEN
IF ((dll_4PID = 0) + (pd_cls_4PID=FALSE) + (mr_pse_ss_mode = 0)) THEN
alt_a_pwrd <= TRUE
alt_b_pwrd <= FALSE
ELSE.."
2. Add Editor Note after Figure 33-9a:
Editors Note: To also adress in POWER_ON state the case that
"alt_a_pwrd <= FALSE
alt_b_pwrd <= TRUE"

Proposed Response *Response Status* **W**

This goes to the primary/secondary updates that Chris/Dylan were going to make.

TFTD.

Cl **33** *SC* **33.2.4.7** *P* **74** *L* **42** # 213

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **X** *PSE SD*

Entry paths to ERROR_DELAY do not consider a fault on only one pairset. The State Diagram needs to facilitate systems that may keep a nonfaulting pairset powered.

SuggestedRemedy

The Task Force should review this during the State Diagram ad hoc. An Editor's note should be made if this is not resolved during the ad hoc.

Place in this section
Editor's note: Entry paths to ERROR_DELAY for Type 3 and 4 PSEs do not consider a fault on only one pairset. The State Diagram needs to facilitate systems that may keep a nonfaulting pairset powered.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.4.7** *P* **79** *L* **1** # 234

Dove, Daniel — Dove Networking Solut

Comment Type **E** *Comment Status* **X** *PSE SD*

Assuming the Task Force agrees that the current classification state diagram only serves single-signature PD operation, move this diagram up in position with all other single-signature diagrams to make them contiguous. Do the same order of diagrams for dual-sig[a] and dual-sig[b] also.

SuggestedRemedy

Assuming the Task Force agrees that the current classification state diagram only serves single-signature PD operation, move this diagram up in position with all other single-signature diagrams to make then contiguous. Do the same order of diagrams for dual-sig[a] and dual-sig[b] also.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.4.7** *P* **79** *L* **6** # 233

Dove, Daniel — Dove Networking Solut

Comment Type **T** *Comment Status* **X** *PSE SD*

The classification diagram has a fundamental problem. For dual signature PDs, there is no explanation in the diagram or text about how the variables behave if classification is performed simultaneously on different pair-sets, or which value of classification holds if they are done sequentially.

SuggestedRemedy

Remove all references to dual signature cases from this diagram and create class[a] and class[b] set of diagrams designed to handle dual-signature PDs for cases where the classification occurs in parallel and/or sequence and correct the connectors into the rest of the state diagram as necessary.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.4.7** *P* **80** *L* **7** # 120

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **X** *Pres: Lennart2*

The Type 3/4 state machine does not have the right MPS behavior which is different for 2P, 4P single-sig and 4P dual-sig.
In addition we also need a double MPS monitoring state machine and variables.

SuggestedRemedy

yseboodt_2_1115_mps_state_machine_v1xx.pdf

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.5.0a** *P* **81** *L* **43** # 182

Dwelley, David — Linear Technology

Comment Type **TR** *Comment Status* **X** *Connection Check*

"Editor's Note:…"
We haven't defined compliance testing for Connection Check yet

SuggestedRemedy

See dwelley_1_1115.pdf

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.5.6** *P* **85** *L* **23** # 172

Stover, David — Linear Technology Cor

Comment Type **E** *Comment Status* **D** *Editorial*

"Type 3 and Type 4 PSEs shall determine whether an attached PD with classes 0 to 4…" Class is not capitalized

SuggestedRemedy

Capitalize Class

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Lennart, shouldn't this be capitalized based on your rule? It's not in your list…

Cl **33** *SC* **33.2.6** *P* **85** *L* **48** # 124

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **X** *Editorial*

"... and the PD responds to each class event with a current representing one of a limited number of power classifications."

power classifications is not a defined term.

SuggestedRemedy

"... and the PD responds to each class event with a current representing one of a limited number of classification signatures."

Proposed Response *Response Status* **W**

power classifications was used in the AT spec and is the title of table 33-7.

TFTD

Cl **33** *SC* **33.2.6** *P* **85** *L* **48** # 125

Yseboodt, Lennart — Philips

Comment Type **T** *Comment Status* **X**

"Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto a pairset and the PD ..."

Seems to preclude applying the class voltage on both pairsets at the same time.

SuggestedRemedy

"Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto one or both pairsets and the PD ..."

Proposed Response *Response Status* **W**

We should think through how this effects the rest of the text dealing with the PD responding to that voltage and producing a current (on that pairset, on both pairsets, etc.).

Cl **33** *SC* **33.2.6** *P* **85** *L* **52** # 15

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *PSE Classification*

To clarify where in the spec one classification event + mark event consider to be multiple event?

SuggestedRemedy

If there is no existing definition, to add after line 52:
"Multiple-Event Physical Layer classification is at least one class event and one mark event"

Proposed Response *Response Status* **W**

The definition is in the state diagram for type 3/4 PSEs. The text says all Type 3/4 PSEs use multiple event and the state diagram shows a single event followed by mark.

If this is not enough, TFTD adding suggested remedy.

Cl **33** *SC* **33.2.6** *P* **86** *L* **13** # 216

Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **D**

The formula 33-3, is not assigned correctly because of a Typo.

SuggestedRemedy

Replace "Class" with "PClass_PD".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This should be PClass. Right?

Cl **33** *SC* **33.2.6** *P* **87** *L* **7** # 3

Darshan, Yair Microsemi

Comment Type **ER** *Comment Status* **D** *Editorial*

Table 33-7 clarity can be improved by the following actions:
1. Columns "Requested Class" is better to switch places with Column "Number of Classification Events" since this is PSE spec and the order of things is what PSE do, what is the PD requested class, what is the Assigned class and then what is the minimum supported power etc.
2. Column "Requested Class" is actually "PD Requested Class".
3. Column "Number of Classification Events" is actually "Number of PSE Classification Events"

SuggestedRemedy

1. Switch place of Columns "Requested Class" with Column "Number of Classification Events".
2. Change column "Requested Class" with "PD Requested Class".
3. Change column "Number of Classification Events" with "Number of PSE Classification Events"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

2. Change column "Requested Class" with "PD Requested Class".
3. Change column "Number of Classification Events" with "Number of PSE Classification Events"

Cl **33** *SC* **33.2.6** *P* **87** *L* **14** # 128

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE Class*

Table 33-7 is lacking the row that describes Type 1 and Type 2 power demotion (Request Class 4, 1 Event => Assign Class 0, 15.4W).

SuggestedRemedy

Add row as second row contents:
4^Note, 1, 0, 15.4 W
With Table Note 3:
"Only for Type 1 and Type 2 PSEs"

Proposed Response *Response Status* **W**

It could also be fixed by having Type 1/2 assign class 3 in this case (no behavior change).

TFTD.

Cl **33** *SC* **33.2.6** *P* **87** *L* **27** # 21

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PSE Class*

Table 33-7-Physical Layer power classifications (PClass)
The text: "NOTE 2-Data Link Layer classification takes precedence over Physical Layer classification."

Note 2 looks not belong to this table, it is better to integrate it with lines 19-21 in page 88: "The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation."

In addition, this is also the right place to integrate the requirement that PD Physical Layer classification indicates the maximum power a PD will ever draw.

SuggestedRemedy

Proposed Remedy
1.Remove Note 2 from Table 33-7.
2.Change the text in page 88 lines 19-21 to be:
"The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation. Data Link Layer classification takes precedence over Physical Layer classification.
The Physical Layer classification of the PD is the maximum power that the PD draws across all output voltages and operational modes."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

I believe the note should still stay attached to this table. Also, the physical layer class sentence is still not normative…

Change the text in page 88 lines 19-21 to be:

"The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation. Data Link Layer classification takes precedence over Physical Layer classification.
The Physical Layer classification of the PD is the maximum power that the PD draws across all output voltages and operational modes."

Cl **33** *SC* **33.2.6** *P* **87** *L* **38** # 4

Darshan, Yair Microsemi

Comment Type **ER** *Comment Status* **D** *PSE Class*

Table 33-7a clarity can be improved by the following actions:
1. Columns "Requested Class ALT A" and "Requested Class ALT B" is better to switch places with Column "Number of Classification Events on alt A" and "Number of Classification Events on alt B" since this is PSE spec and the order of things is what PSE do, what is the PD requested class, what is the Assigned class and then what is the minimum supported power etc.
2. Column "Requested Class ALT A" is actually "PD Requested Class mode A" and "Requested Class ALT B" is actually "PD Requested Class mode B".

SuggestedRemedy

1. Switch columns "Requested Class ALT A" and "Requested Class ALT B" with column "Number of Classification Events on alt A" and "Number of Classification Events on alt B".
2. Change "Requested Class ALT A" with "PD Requested Class mode A"
3. Change "Requested Class ALT B" with "PD Requested Class mode B".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

2. Change "Requested Class ALT A" with "PD Requested Class mode A"
3. Change "Requested Class ALT B" with "PD Requested Class mode B".

Cl **33** *SC* **33.2.6.2** *P* **92** *L* **1** # 200

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **X** *PSE Class*

"If the class signature detected during CLASS_EV1_LCF is 0, a Type-3 or Type-4 PSE treats a dual-signature PD as a Type-1 PD and shall omit...."

This is probably one of a number of examples where any distinctions between equal and non-equal dual-signature PD's are not clear. For example, does this rule apply to each pairset of a dual signature PD independently ? What if PD is Class 0 on one pairset and Class 4 on another pairset ? What if PD is Class 0 on both pairsets ?

SuggestedRemedy

For now, this is probably an editor's note covering section 3.2.6 in general to clean up distinctions between dual-signature even verus non-even class PD's.

In an ideal world, we might organize much of 33.2.2.6 along the lines of Single Signature PD's, Dual Signature Equivalent Class PD's, and Dual Signature Non-Equivalent Class PD's.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.6.3** *P* **94** *L* **46** # 134

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *Editorial*

"P_ac_margin is minimum margin the PSE must add to the measured power P Autoclass in Watts".

The word 'must' should not be used.

SuggestedRemedy

"P_ac_margin is minimum margin the PSE adds to the measured power P Autoclass in Watts".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This needs to be changed, but where is this number/equation used. It is no longer referenced in the text.

Cl **33** *SC* **33.2.7** *P* **95** *L* **9** # 135

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE Power Removal*

"Power may be removed from both pairsets any time power is removed from one pairset."
Also (page 104, line 29):
"When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

A Type 3/4 PSE supplying power Class 5 or greater, must do this over 4P.
If a pairset is shut down, for whatever reason, the PSE now operates in an incorrect mode that may persist forever (depending on PD consumption & ICut value), with cable current that exceeds Icable.
PSEs should not operate in incorrect modes.

SuggestedRemedy

Add after "Power may be removed from both pairsets any time power is removed from one pairset.":
"Power shall be removed from both pairsets within (TBD time) any time power is removed from one pairset, when connected to a single-signature PD assigned to Class 5 or higher."

Remove "When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset." from page 104/line 29.

Proposed Response *Response Status* **W**

TFTD.

Cl **33** *SC* **33.2.7** *P* **96** *L* **4** # 173

Stover, David Linear Technology Cor

Comment Type **E** *Comment Status* **D** *Editorial*

Classes is not capitalized in title of Table 33-11

SuggestedRemedy

Capitalize Classes

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

OBE by… 30?

Cl **33** *SC* **33.2.7** *P* **96** *L* **33** # 138

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *Unbalance*

Table 33-11, item 4a (Icon-2p_unb) does not have a complete Types listing.

SuggestedRemedy

Class 0-4 => PSE Type: All
Class 5 => PSE Type: 3,4
Class 6 => PSE Type: 3,4
Class 7 => PSE Type: 4
Class 8 => PSE Type: 4

Addressed in yseboodt_3_1115_Table_33_11_item4a.pdf

Proposed Response *Response Status* **W**

Possible OBE by 136

Cl **33** *SC* **33.2.7** *P* **96** *L* **33** # 136

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *Unbalance*

In Table 33-11 we have Icon-2P_unb which specifies the minimum unbalanced current a PSE must be able to supply.
It is specified for Class 5 through 8.

If a PD assigned Class 4 or lower is getting 4P power, there is no limit to the amount of unbalance.
This is currently not specified.

SuggestedRemedy

Add extra row for item 4a for Class 0-4 setting Icon-2P_unb to I_Con:

4a, Pairset current including unbalance for Class 0-4, Icon-2p_unb, A, I_Con, 3, See 33.2.7.4 and 33.2.7.4.1.

Addressed in yseboodt_3_1115_Table_33_11_item4a.pdf

Proposed Response *Response Status* **W**

TFTD (show new Table)

Cl **33** *SC* **33.2.7** *P* **96** *L* **50** # 11

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *Pres: Darshan4*

Table 33-11 item 5a Inrush-2P: Addressing the requirements for Type 3 and 4 including unbalance effects.
Addressing PD Cport when PSE is responsible for limiting Iinrush.

SuggestedRemedy

See darshan_04_1115.pdf for proposed baseline text.

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.2.7** *P* **97** *L* **9** # 139

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE Power*

The current definition of I_CUT-2P includes unbalance current for BOTH pairsets, requiring the PSE to support a positive unbalance current on both pairsets.

SuggestedRemedy

See yseboodt_10_1115_Figure_33_14_v3xx.pdf (that file addresses more than just this comment)

Proposed Response *Response Status* **W**

wfp

I don't have this document yet.

Cl **33** *SC* **33.2.7** *P* **97** *L* **33** # 141

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE Power*

Table 33-11, item 9 (Ilim-2P) is now a Class based parameter.
For this item, the Class is listed in the Additional information field, whereas for Icon-2P_unb the class distinction is made in the Parameter field.

SuggestedRemedy

See yseboodt_4_1115_Table_33_11_item9.pdf

Proposed Response *Response Status* **W**

TFTD (Show Table).

Cl **33** *SC* **33.2.7** *P* **97** *L* **45** # 203

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **X** *PSE Power*

Table 33-11, item 12 should better reflect what is required and remove repeated information.

Footnote-1 text:
A Type 3 PSE that is limited to Class 3 power may use Type 1 values for Icable and Vport_pse-2p min. A Type 3 PSE that is limited to Class 4 power may use Type 2 values for Icable and Vport_pse-2p min.

SuggestedRemedy

When Type 3 PSEs to provide at least class-3 power values, PDs provide an active indication when they are under powered.

Item 12 first row, PSE Type column, replace, "1" with "1, 3". Move the footnote on item 12, row 3, PSE Type column, to the first row so that it now applies to the Type 3 in row one. Delete item 12, row 3 and 4.

Replace footnote-1 with,
"A Type 3 PSE that is limited to Class 3 power may use Type 1 values for Icable. A Type 3 PSE that is limited to Class 4 power may use Type 2 values for Icable. A Type 3 PSE that is limited to Class-5 or Class-6 power may use Type 3 values for Icable."

This comment is related to a comment marked COMMENT1.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.2.7** *P* **97** *L* **51** # 207

Schindler, Fred — Seen Simply

Comment Type **T** *Comment Status* **D** *Pres: Lennart?*

Permit Type-4 PSE to provide a minimum of class-7 power or 75.0 W.

SuggestedRemedy

Replace Table 33-11, item 12, the row for Type-4, Min column, with "75.0".
This comment is related to a comment marked COMMENT1.

Proposed Response *Response Status* **W**

wfp from Lennart about Ptype

Cl **33** *SC* **33.2.7** *P* **98** *L* **16** # 32

Yseboodt, Lennart — Philips

Comment Type **ER** *Comment Status* **X** *PSE MPS*

Table 33-11, Items 17, 17a and 17b are for Ihold.
There is a lot of information crammed into these items, some of which is better explained in section 33.2.9.1.2.

SuggestedRemedy

See yseboodt_5_1115_Table_33_11_item17.pdf

Proposed Response *Response Status* **W**

TFTD (show Table)

Cl **33** *SC* **33.2.7** *P* **99** *L* **28** # 33

Yseboodt, Lennart — Philips

Comment Type **ER** *Comment Status* **X** *Pres: Lennart6*

Note 1 below Table 33-11:
"A Type 3 PSE that is limited to Class 3 power may use Type 1 values for I cable and V port_pse-2p min. A Type 3 PSE that is limited to Class 4 power may use Type 2 values for I cable and V port_pse-2p min."

This note is no longer needed if proposed modifications to PType are adopted in yseboodt_6_1115_Ptype_baseline_v1xx.pdf

SuggestedRemedy

Remove note 1.

Proposed Response *Response Status* **W**

TFTD (wfp)

Cl **33** *SC* **33.2.7** *P* **99** *L* **28** # 34

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *PSE MPS*

Note 2 and 3 below Table 33-11:
"2 Item 17 and 17a apply to PSEs that implement MPS detection per pairset."
"3 Item 17b applies to PSEs that implement MPS detection by measuring the sum of the pair currents of the same polarity."

If yseboodt_5_1115_Table_33_11_item17.pdf is adopted, the numbering is no longer correct.

SuggestedRemedy

"2 Item 17 applies to PSEs that measure currents per pairset to check the MPS."
"3 Item 17a applies to PSEs that measure the sum of the pair currents of the same polarity to check the MPS."

Proposed Response *Response Status* **W**

TFTD (show table)

Cl **33** *SC* **33.2.7** *P* **99** *L* **40** # 7

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *Pres: Darshan5*

Editor Note #2.
"2. The following case needs to be addressed: If PSE is using active or passive pair-to-pair current balancing circuitry, K_Icut may be lower (down to 0.5) per equation TBD."
We need to adress PSE requirements when active or passive current balancing is used that effects Icut-2P, ILIM-2P.

SuggestedRemedy

See presentation and proposed Remedy in darshan_05_1115.pdf

Proposed Response *Response Status* **W**

TFTD (wfp)

Cl **33** *SC* **33.2.7.4** *P* **100** *L* **48** # 218

Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **D** *Editorial*

Variable Icon-2P is defined on page 100 formula 33-3c and on page 101 formula 33-3e. Only one definition should exist.

SuggestedRemedy

Replace existing references to 33-3e with 33-3c.

Replace existing text on page 101,
"Note that for these PDs ICon-2P is calculated using Equation (33-3e) for each pairset independently."

With
"Note that for these PDs Icon-2P is calculated using Equation (33-3c) for each pairset independently."

Strike formula 33-3e.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.7.4** *P* **101** *L* **24** # 40

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *Pres: Lennart10*

A PSE must currently support a "double unbalance" Ipeak current.

SuggestedRemedy

See yseboodt_10_1115_Figure_33_14_v3xx.pdf (that file addresses more than just this comment)

Proposed Response *Response Status* **W**

TFTD (wfp)

Cl **33** *SC* **33.2.7.4** *P* **101** *L* **34** # 8

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *Unbalance*

The text "For Type 3 and Type 4 PSEs, operating in 4-pair mode and connected to single-signature PDs, the value of KIpeak is given by Equation 33-4a. For all other cases the value of KIpeak is 0. Dual-Signature PDs TBD."

The text above can be updated after the discussion results of D1.3.
Now it is clear that for dual signature PDs with different class signature Kipeak=0 too.

SuggestedRemedy

Change:
"For Type 3 and Type 4 PSEs, operating in 4-pair mode and connected to single-signature PDs, the value of KIpeak is given by Equation 33-4a. For all other cases the value of KIpeak is 0. Dual-Signature PDs TBD."
To:
"For Type 3 and Type 4 PSEs, operating in 4-pair mode and connected to single-signature PDs and dual-signature PDs with the same class signature on each pairset, the value of KIpeak is given by Equation 33-4a. For all other cases the value of KIpeak is 0."

Proposed Response *Response Status* **W**

TFTD

Did we decide to give unbalance to dual-sig PDs with the same class? How do we spec the isolation/3-pair power requirement?

Cl **33** *SC* **33.2.7.4.1** *P* **102** *L* **5** # 41

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *Editorial*

"... the maximum pair current due to E2EP2PRunb, is not exceeding I con-2P-unb as defined in Table 33-11 during normal operating conditions."

Reword.

SuggestedRemedy

"... the maximum pair current does not exceed I con-2P-unb as defined in Table 33-11 during normal operating conditions due to unbalance."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

"... the maximum pair current including unbalance does not exceed I con-2P-unb as defined in Table 33-11 during normal operating conditions."

Cl **33** *SC* **33.2.7.6** *P* **104** *L* **11** # 45

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE Power*

"The I CUT-2P threshold may be greater than or equal to the I Peak-2P value determined by Equation (33-4). The I CUT-2P threshold needs to be below I LIM_MIN as described by Figure 33-14."

The I_CUT-2P range is defined by Table 33-11.
This text does not match with what should be in Table 33-11.

Icut-2 min is Icon-2P and Icut-2p max is defined by the relevant upperbound template.

SuggestedRemedy

Remove both sentences. The definition is clear from Table 33-11 and we should not double-specify.

Proposed Response *Response Status* **W**

TFTD.

Should 4-pair policing be based on total current (minimum = Icon)?

Cl **33** *SC* **33.2.7.7** *P* **104** *L* **29** # 23

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *PSE Power*

The text in lines 12-14:
"When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."
is redundant.
The requirement is already covered by previous lines lines 10-12:
Power shall be removed from a pairset PI of a PSE before the pairset PI current exceeds the "PSE upperbound template" in Figure 33-14, Figure 33-14a, and Figure 33-14b.

SuggestedRemedy

Change from:
"When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template"

To:
"When connected to a single signature PD, a Type 3 or Type 4 PSE may remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset."

Proposed Response *Response Status* **W**

TFTD.

Cl **33** *SC* **33.2.7.7** *P* **106** *L* **12** # 47

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Pres: Lennart6*

In Figure 33-14c, I_TBDNAME should be renamed.

SuggestedRemedy

Change I_TBDNAME to I_LPS.
OBE if adopt yseboodt_6_1115_Ptype_baseline_v1xx.pdf

Proposed Response *Response Status* **W**

TFTD (wfp)

Cl **33** *SC* **33.2.7.11a** *P* **109** *L* **42** # 206

Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **D** *PSE Power*

The existing text, "PType (min) is the minimum power a PSE must support to enable the highest Class that a PSE of that Type can support.

Type 3 PSEs are not required to support PType if they are restricted to Class 5 power or lower.
Type 4 PSEs are not required to support PType if they are restricted to Class 7 power or lower."

May be misinterpreted by some readers.

SuggestedRemedy

Replace the first sentence with,
"PType (min) is the minimum power a PSE shall source."

Strike the next two sentences, "Type 3 …" and "Type 4 …" because Table 33-11 already provides the value for Ptype.

This comment is related to a comment marked COMMENT1.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

You can't force a PSE to source power. A PSE can only make power available, it is up to the PD to draw it.

Cl **33** *SC* **33.2.8** *P* **110** *L* **43** # 220

Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **D** *PSE Power*

The existing text,
"Editor's Note: Text needs to be added to mutual ID section to assign PD Class during power demotion."

May no longer apply because demotion is indirectly covered on page 92 Line 5.

SuggestedRemedy

Strike the Editor's note if the Task Force believes the concern has been covered.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

"When a PD requests a higher Class than a Type 3 or Type 4 PSE can support, the PSE assigns the PD Class 3, 4, or 6, whichever is the highest that it can support."

Does seem to desribe power demotion. However, what happens if a PSE can't even support class 3?

Cl **33** *SC* **33.2.9.1.2** *P* **112** *L* **49** # 183

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **X** *Pres: Dwelley1*

"A PSE shall consider the DC MPS component to be present…"
Diode unbalance in a PD complicates disconnect measurement - similar to connection check, we should define compliance testing for the PSE

SuggestedRemedy

See dwelley_1_1115.pdf

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.3.2** *P* **115** *L* **7** # 56

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Types*

"PDs can be categorized as either Type 1, or Type 2, Type 3/SS, Type 3/DS, Type 4/SS or Type 4/DS. Table 33-13a shows the permissible PD types along with supported parameters."

Table 33-13a and supporting text combines 'signature' and Type.
These are separate concepts.

SuggestedRemedy

Change text to:
"PDs can be categorized as either Type 1, Type 2, Type 3, or Type 4.
PDs can be constructed as single-signature or dual-signature as defined in 1.4 and 33.2.5.0a.
Table 33-13a shows the permissible PD types along with supported parameters."

Change Table 33-13a to yseboodt_7_1115_Table_33_13a_v1xx.pdf

Proposed Response *Response Status* **W**

TFTD (show Table)

Cl **33** *SC* **33.3.2** *P* **116** *L* **16** # 58

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **X**

original text: "Editor's Note: Need to move two normative requirements from section 33.3.2."

Let`s move them. Which two ?

SuggestedRemedy

TFTD

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.3.4** *P* **122** *L* **1** # 184

Dwelley, David Linear Technology

Comment Type **E** *Comment Status* **D** *PD Detection*

"When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive VPD and Negative VPD of PD Mode A and PD Mode B as defined in 33.3.1."
This could be more clear.

SuggestedRemedy

Change to: "When a PD presents a detection signature (either valid or non-valid), it shall present that signature at its PI at both the Mode A and Mode B pairsets, as defined in 33.3.1."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is legacy text. Do we really want to mess with it?

Cl **33** *SC* **33.3.5** *P* **104** *L* **43** # 22

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *PD Class*

Missing "Shall" in the following text:
"The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes."

If "Shall" is not used, it will lead to interoperability issues when DLL is used in a way to request more power than the advertised physical layer class.

SuggestedRemedy

Change from:
"The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes."
To:
"The Physical Layer classification of the PD shall be the maximum power that the PD draws across all input voltages and operational modes."

Proposed Response *Response Status* **W**

TFTD

This will affect Type 1/2 as written.

See 63.

Cl **33** *SC* **33.3.5** *P* **123** *L* **39** # 62

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X**

original text: "Editor's Note: The interaction of DLL and Physical Layer Classification needs to be clarified. Comments are welcome."

SuggestedRemedy

Either:
- clarify editor`s not as to which interaction is unclear, or
- remove note.

Proposed Response *Response Status* **W**

I believe this is meant to draw comments such as 22.

Cl **33** *SC* **33.3.5** *P* **123** *L* **46** # 63

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X**

"The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes."

The intent is clear, a shall was forgotten.

SuggestedRemedy

"The Physical Layer classification of the PD is the maximum power that a Type 1 or Type 2 PD draws across all input voltages and operational modes.

The advertised class during Physical Layer classification of the PD is the maximum power that a Type 3 or Type 4 PD shall draw across all input voltages and operational modes."

Proposed Response *Response Status* **W**

TFTD. See 22

Cl **33** *SC* **33.3.5.2** *P* **126** *L* **6** # 201

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **D** *Editorial*

This is a third attempt to better name state variables "class_sig_A" and "class_sig_B" in Table 33-16a and other locations. As before, concern is confusion with classifying ALT-A and ALT-B on dual-signature PD's. Prior comments were AIP but 4 prior remedies have been rejected.

So.....try try again!

SuggestedRemedy

Name class_sig_A as 'class_EV1_sig' and class_sig_B as 'class_EV3_sig'.

These newest terms reflect headers in Tables 33D-1 and 33D-2 (appendix) where the names "CLASS_EV1_LCF signature" and "CLASS_EV3 signature" are used. Seems like if they are okay in the appendix, they might be alright here....????

IF NOT....perhaps there is an issue in the appendix ???

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Better names are welcome. TFTD this suggestion. The Appendix will likely be removed.

Cl **33** *SC* **33.3.7** *P* **129** *L* **45** # 69

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **D** *PSE Power*

Table 33-18, Item 1, Item 7 and Item 10 can be compacted by writing the parameter name only once.
This is similar to my proposals in Table 33-11.

SuggestedRemedy

Implement yseboodt_9_1115_Table_33_11_item1_7.pdf

Proposed Response *Response Status* **W**

TFTD (show table).

Cl **33** *SC* **33.3.7** *P* **130** *L* **50** # 71

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **X** *Editorial*

Warning: legacy text!
"... with a series resistance within the range of valid Channel Resistance."

SuggestedRemedy

"... with a series resistance within the range R_ch"

Proposed Response *Response Status* **W**

TFTD.

Chair?

Cl **33** *SC* **33.3.7.1** *P* **130** *L* **32** # 2

Darshan, Yair Microsemi

Comment Type **ER** *Comment Status* **X** *PD Power*

Table 33-18 items 11, 12 and 13 (PD power supply turn on voltage, PD power supply turn off voltage, and PD classification stability time):
need to be per pairset.

SuggestedRemedy

Add to each parameter name of items 11 , 12, and 13: "per pairset"

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.3.7.2** *P* **131** *L* **5** # 156

Bennett, Ken Sifos Technologies, In

Comment Type **TR** *Comment Status* **D** *PD Power*

For Draft 1.3, Comment 103 was accepted as follows:
"PClass_PD in Table 33–18 is determined by the Class assigned by the PSE."
The reference to table 33-18 was changed during editing to Table 33-16a.

The reference to table 33-18 specifically targeted item 4, which must set the PD limit to meet a PSE's allocation. Table 33-16a only describes PClass_PD for PDs when they are granted full power. Table 33-7 does show a PSE's "assigned class", and could be used as an additional reference.

SuggestedRemedy

Change the table reference back to the accepted version:

PClass_PD in Table 33–18 is determined by the Class assigned by the PSE.

Optionally expand it to:

PClass_PD in Table 33–18 is determined by the Class assigned by the PSE (see Table 33-7). PClass_PD values for each Class are shown in Table 33-16a.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Optionally expand it to:

PClass_PD in Table 33–18 is determined by the Class assigned by the PSE (see Table 33-7). PClass_PD values for each Class are shown in Table 33-16a.

Cl **33** *SC* **33.3.7.3** *P* **131** *L* **54** # 202

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *Inrush*

"Input inrush current at startup is limited by the PSE if Cport per pairset < 180uF,..."

This statement may open the door to any PD (Type-1, 2, etc) that has 180uF on EACH pairset, or 360uF combined before PD has responsibility for current limiting.

SuggestedRemedy

Specify that the 180uF applies to "powered" pairsets so a given and case of 2-pair powering, 180uF is the maximum allowed capacitance before PD current limiting.

"Input inrush current at startup is limited by the PSE if Cport per powered pairset < 180uF,..."

This may/will probably be further affected as inrush gets worked out in future drafts.

Proposed Response *Response Status* **W**

TFTD

I'm not sure if I understand the distiction Peter is trying to draw.

Cl **33** *SC* **33.3.7.3** *P* **132** *L* **11** # 221

Darshan, Yair — Microsemi

Comment Type **T** *Comment Status* **X** *Inrush*

D1.4 This an update of a similar comment in round 1.
This is the response to the remedy of comment # 150 in D1.3 which says:
To delete the text "See PSE-PD simplified Cport implementation model in Annex TBD."
From:
"Cport in Table 33-18 is the total PD input capacitance during POWER UP and POWER ON states that a PSE sees when connected to a single-signature PD over a pairset or both pairsets. When PSE is connected to dual-signature PDs, Cport value requirements are specified in 33.3.7.6.
"Yair is invited to provide figure and new text (no Annex)".

SuggestedRemedy

1. Change from:
"Cport in Table 33-18 is the total PD input capacitance during POWER UP and POWER ON states that a PSE sees when connected to a single-signature PD over a pairset or both pairsets. When PSE is connected to dual-signature PDs, Cport value requirements are specified in 33.3.7.6."

To:
Cport in Table 33-18 is the total PD input capacitance during POWER UP and POWER ON states that a PSE sees when operating one or both pairsets, when connected to a single-signature PD. When PSE is connected to dual-signature PDs, Cport value requirements are specified in 33.3.7.6."
See Figure 33-17.1 for PSE-PD simplified Cport interpretation model."

2. Add figure 33-17.1 after the above text as described in page 3 of darashan_02_1115.pd.

Proposed Response *Response Status* **W**

TFTD (show figure)

Cl **33** *SC* **33.3.7.4** *P* **132** *L* **23** # 157

Bennett, Ken — Sifos Technologies, In

Comment Type **TR** *Comment Status* **X** *Extended Power*

For Class 6 and 8:

Section 33.3.7.2 allows extended average power when "additional information is available to the PD regarding actual channel DC resistance."

Section 33.3.7.4. always allows extended peak power. Section 33.3.7.4 needs the "additional information" qualifier.

The remedy adds the "additional information" requirement to the Peak Power.

For reference, the existing peak power text in 33.3.7.4 is:

At any static voltage at the PI, and any PD operating condition, with the exception of Class 6 or Class 8 PDs, the peak power shall not exceed PClass_PD max for more than TCUT-2P min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed PPeak max.

For Class 6 and Class 8 PDs in any operating condition with any static voltage at the PI, the peak power shall not exceed PClass at the PSE PI for more than TCUT min, as defined in Table 33–11 and with 5% duty cycle.

SuggestedRemedy

1. Remove "With the exception of class 6 and class 8 PDs" from line 18.

2. Change the sentence at line 23 to:

For Class 6 or Class 8 PDs, when additional information is available to the PD regarding actual channel DC resistance, the peak power for any operating condition and any static voltage at the PI shall not exceed PClass at the PSE PI for more than TCUT min, as defined in Table 33–11 and with 5% duty cycle.

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.3.7.10** *P* **137** *L* **9** # 186

Beia, Christian — STMicroelectronics

Comment Type **TR** *Comment Status* **X** *Pres: Darshan?*

The requirement in the text is conditioned to a measurement, which is not appropriate, because it must apply regardless of anything.

Moreover, figure 33-18a does't really help to understand the relevant text because it is not clear what "Rsource_max/Rsource_min" means.
But since it is not easy to draw a figure which shows all the cases of Rmin/Rmax, I suggest to modify 33.3.7.10 text, adding some more information.

SuggestedRemedy

Replace the following text:

PDs shall meet this requirement when connected to a common source voltage through a resistance of Rsource_min =0.16 Ohm± 1% and Rsource_max
=0.19 Ohm± 1% to PD PI pairs of the same polarity for all PD operating conditions as shown in Figure 33–18a.

With:

PDs shall have the pair currents measured when the PD PI pairs of the same polarity are connected to a common source voltage through two common mode resistances of Rsource_min=0.16 Ohm ± 1% and Rsource_max=0.19 Ohm ± 1% for all PD operating conditions as shown in Figure 33-18a. These resistances may be different from each other and the worst case happens when one resistance value is minimum while the other is maximum.

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.3.7.10** *P* **137** *L* **9** # 89

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **D** *PD Power*

"All Class 5 and higher PDs shall not exceed I con-2P-unb as defined in Table 33-11 on any pair."

Does not specify timing. This only applies for t>Tcut-2P min

SuggestedRemedy

"All Class 5 and higher PDs shall not exceed I con-2P-unb for longer than T_cut-2P min as defined in Table 33-11 on any pair."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.7.10** *P* **137** *L* **17** # 13

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *Pres: Darshan3*

To adress Editors note in line 17: "Editor's Note: Longer channel resistances need to be added."

D1.4 requires in its Editor Note in page 137 line 17 to address longer channel as well due to the fact that it looks that meeting Icon-2P_unb is restricted to short channel only per the old text rather than Icon-2P_unb has to be met at any case. However Icon-2P_unb should be measured at worst case conditions i.e. short cable . The following changes fix the problem.

SuggestedRemedy

1. Remove Editor Note in line 17.
2. Change the text per darshan_03_1115.pdf.

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33.6** *P* **159** *L* **36** # 94

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *Editorial*

"Type 2, Type 3 and Type 4 PDs that require more than Class 3 power levels, or Type 3/DS and Type 4/DS PDs support Data Link Layer classification (see 33.3.5)."

Signature and Type are separate entities. The abbreviation Type x/DS should not be used.

SuggestedRemedy

"Type 2, Type 3 and Type 4 PDs that require more than Class 3 power levels, or dual-signature PDs support Data Link Layer classification (see 33.3.5)."

Proposed Response *Response Status* **W**

TFTD

How does this affect Type 1/2?

Cl **33** *SC* **33.6.1** *P* **159** *L* **23** # 93

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *TLV*

original text: "Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009 shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and shall support the control state diagrams defined in 33.6.3."

We decided to have two different subtype TLVs.
See presentation "wendt_1_1115_LLDP_Extensions_vxxx.pdf" and related baseline proposal.

SuggestedRemedy

"Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009 shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and the Power via MDI Measurements TLV defined in 79.3.7 and shall support the control state diagrams defined in 33.6.3."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

"Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and the Power via MDI Measurements TLV defined in 79.3.7; and shall support the control state diagrams defined in 33.6.3."

Cl **33** *SC* **33.6.3.2** *P* **160** *L* **32** # 161

Tremblay, David Hewlett Packard Enter

Comment Type **ER** *Comment Status* **X** *DLL*

PD_DLLMAX_VALUE of 999 for pd_max_power 8 is inconsistent with Pclass_pd in Table 33–16a.

pd_max_power	PD_DLLMAX_VALUE
8	999

SuggestedRemedy

Change 999 to 710 on line 32.

pd_max_power	PD_DLLMAX_VALUE
8	710

Proposed Response *Response Status* **W**

TFTD.

This was done to allow a class 8 PD request up to the maximum power capable of being sourced.

Cl **33** *SC* **33.6.3.2** *P* **160** *L* **46** # 162

Tremblay, David — Hewlett Packard Enter

Comment Type **ER** *Comment Status* **D** *DLL*

PD_INITIAL_VALUE of 900 for pd_max_power 8 is inconsistent with Pclass_pd in Table 33–16a.

pd_max_power	PD_INITIAL_VALUE
8	900

SuggestedRemedy

Change 900 to 710 on line 46.

pd_max_power	PD_INITIAL_VALUE
8	710

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 158

Cl **33** *SC* **33.6.3.2** *P* **161** *L* **6** # 158

Bennett, Ken — Sifos Technologies, In

Comment Type **TR** *Comment Status* **X**

PSE_INITIAL_VALUE is used to initialize the PSE allocated and PD requested values in the DLL Classification state diagram. For Class 6 and Class 8, these values are currently 600 and 900 respectively.

Values of 600 and 900 are only valid for extended power, where "additional information is known about actual channel resistance" (from 33.3.7.2). Under normal operation, these values should be initialized at 510 and 710, which is correct when no additional information is available.

SuggestedRemedy

Change PSE_INITIAL_VALUEs for Class 6 and Class 8 values to 510 and 710 respectively.

Could consider adding a footnote to these values, stating:
1. If there is a priori knowledge of channel resistance, the PSE_INITIAL_VALUE settings for class 6 and class 8 may be increased up to a maximum of 600 and 900 respectively.

Proposed Response *Response Status* **W**

TFTD.

See 162.

Cl **33** *SC* **33.6.3.2** *P* **161** *L* **8** # 163

Tremblay, David — Hewlett Packard Enter

Comment Type **ER** *Comment Status* **D** *DLL*

PSE_INITIAL_VALUE of 900 for parameter_type 4 with mr_pd_class_detected 8 is inconsistent with Pclass_pd in Table 33–16a.

parameter_type	mr_pd_class_detected	PSE_INITIAL_VALUE
4	8	900

SuggestedRemedy

Change 900 to 710 on line 8.

parameter_type	mr_pd_class_detected	PSE_INITIAL_VALUE
4	8	710

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.6.3.3** *P* **161** *L* **28** # 164

Tremblay, David — Hewlett Packard Enter

Comment Type **ER** *Comment Status* **X** *DLL*

The following variables contain ending values which are inconsistent with Pclass_pd in Table 33–16a.

MirroredPDRequestedPowerValue - page 161, line 28
MirroredPSEAllocatedPowerValue - Page 161, line 37
PDRequestedPowerValueEcho - Page 161, line 44
PSEAllocatedPowerValue - Page 162, line 8
PSEAllocatedPowerValueEcho - Page 162, line 12

Values: 0 through 999

SuggestedRemedy

Change the ending value to 710 for all five variables.

Values: 1 through 710

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.6.3.3** *P* **161** *L* **28** # 160

Tremblay, David — Hewlett Packard Enter

Comment Type **ER** *Comment Status* **D** *DLL*

The following variables contain a starting value of 0 which is invalid per clause 79:

MirroredPDRequestedPowerValue - page 161, line 28
MirroredPSEAllocatedPowerValue - Page 161, line 37
PDRequestedPowerValueEcho - Page 161, line 44
PDRequestedPowerValue - Page 162, line 1
PSEAllocatedPowerValue - Page 162, line 8
PSEAllocatedPowerValueEcho - Page 162, line 12

Values: 0 through 999

SuggestedRemedy

Change the starting value to 1 for all six variables.

Values: 1 through 999

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.6.3.3** *P* **162** *L* **2** # 204

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **X** *DLL*

The text in this section may not provide enough information to avoid interoperability issues when Type-3 and Type-4 PSEs receive a DLL PD requests for power that exceed Pclass_PD shown in Table 33-16a.

Existing text:
PSEAllocatedPowerValue Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.7.2) the PD ever draws. The power value for a PSE is the maximum input average power the PD may ever draw. This power value is encoded according to Equation (79-2), where X is the decimal value of PSEAllocatedPowerValue. This variable is mapped from the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).
Values:0 through 999

SuggestedRemedy

After "…attribute (30.12.2.1.18)." add,
"If the PDRequestedPowerValue exceeds Pclass_PD shown in Table 33-26a, the PSE may assume that the PD has determined the power request made will not lead to more than PClass to be drawn from the PSE. Additional information on power levels for classes 6 and 8 may be found in 33.3.7.2."

Please also correct the grammar in the existing text by replacing "…power value in the PSE." with "… power values by the PSE."

Proposed Response *Response Status* **W**

TFTD

Cl **33** *SC* **33.8.3.5** *P* **183** *L* **19** # 169

Maguire, Valerie — Siemon

Comment Type **T** *Comment Status* **D** *Cabling*

Align PSEEL13 with clause 33.4.9.1.4 and resolution of #22 against draft 1.3. Category 5 jumper performance is specified in ANSI/TIA/EIA-568-A:1995.

SuggestedRemedy

Replace, "ANSI/TIA-568-C.2" with "ANSI/TIA/EIA-568-A:1995"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33A.5** *P* **172** *L* **31** # 222

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *Pres: Darshan1*

NEW D1.4
Updating comment sent at the first round.
Requested by remedy of comment #5 from D1.3:
In Annex 33A.5 to define Rpair_max_PD, Rpair_min_PD.

SuggestedRemedy

1.Add the following text after line 31
RPair_PD_max and RPair_ PD_min represent PD common mode input effective impedance of pairs of the same polarity.
The effective resistance Zi is the measured voltage Veff_pd_i, divided by the current through the path as described below and as shown in the example in Figure 33A-1.
Positive pairs:
Z1= RPair_ PD_min =Veff_pd1/i1
Z3= RPair_PD_max =Veff_pd3/i3
Negative pairs:
Z2= RPair_ PD_min =Veff_pd2/i2
Z4= RPair_PD_max =Veff_pd4/i4

2.Add figure 33A-1 after the above text as described in page 3 of darshan_01_1115.pdf3.

3. Lines 20-31: Change from RPair_max_PD to RPair_PD_max and from RPair_min_PD to RPair_PD_min. 10 occurrences.

4. In the equations in lines 21-27, add "[ohm]" after RPair_PD_max. 4 occurrences.

5. Delete Editor Note in lines 32-36.

Proposed Response *Response Status* **W**

wfp

Cl **33** *SC* **33A.5** *P* **172** *L* **35** # 10

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *Pres: Darshan1*

Requested by remedy of comment #5 from D1.3:
In Annex 33A.5 to define Rpair_max_PD, Rpair_min_PD.

SuggestedRemedy

1. Add the following text after line 35:
"Rpair_max_PD and Rpair_min_PD represents PD common mode input effective impedance.
The effective resistance is the measured voltage Veff_pd_i, divided by the current through the path e.g. the effective value of Rpair_max_PD =Veff_pd1/i1 and Rpair_min_PD =Veff_pd3/i3 as shown in Figure 33A-1."
2. Add figure 33A-1 after the above text as described in darshan_01_1115.pdf

Proposed Response *Response Status* **W**

wfp

Cl **33B** *SC* **33B** *P* **191** *L* **1** # 144

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X**

Annex 33B contains:
2 shalls
2 musts

Do we need a normative annex for 2 shalls ?
Also, the shalls are very similar to each other.

SuggestedRemedy

Consider to move the requirement into the appropriate section in 33.2.
33.2.7.4.1 seems like a good candidate.

TF to discuss the 'musts' and either reword or turn into 'shalls'.

Proposed Response *Response Status* **W**

TFTD

Cl **33B** *SC* **33B** *P* **191** *L* **23** # 146

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Pres: Lennart8*

Figure 33B-1.
According to 33.1.3: "The PI is the electrical interface between the PSE or PD and the transmission medium."
In my understanding: the PI is right between where the jack and plug contacts meet.

- Figure 33B-1 shows Vport_pse behind the R_pair resistance from the dotted line which I presume is the PI ?
- Why is the PSE internal resistance called R_pair ?
- Later section refers to Rpse but is isn`t defined ?

SuggestedRemedy

See yseboodt_8_1115_Fig_33B_1.pdf which:
- Does not refer to Vport_pse
- Renames Rpair to Rpse

Proposed Response *Response Status* **W**

TFTD (show figure)

Cl **33B** *SC* **33B** *P* **191** *L* **23** # 147

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Editorial*

Figure 33B-1.
The figure seems to suggest that the PD is drawing PClass.
When it does that, with a non zero ohm channel, the PSE delivers more than Pclass. This is a non-compliant PD at this point.

SuggestedRemedy

Change PClass to Pclass_PD ?

Proposed Response *Response Status* **W**

TFTD

Cl **33B** *SC* **33B** *P* **192** *L* **36** # 148

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **X** *Editorial*

Section 33B.2 is titled: "Effective resistance measurement method by measurement of current unbalance under worst case pair-to-pair load conditions"
Which is somewhat long for a section title.

SuggestedRemedy

It seems that 33B.1 through 33B.3 are different methods to measure R_pse max and R_pse min.

- Add sentence to 33B: "Measurement methods to determine R_pse min and R_pse max are defined in 33B.1, 33B.2 and 33B.3"
- Rename 33B.1 to "Direct R_pse measurement"
- Rename 33B.2 to "Effective resistance R_pse measurement"
- Rename 33B.3 to "Current unbalance R_pse measurement"

Proposed Response *Response Status* **W**

TFTD

Cl **33B** *SC* **33B.2** *P* **193** *L* **29** # 181

Stover, David Linear Technology Cor

Comment Type **E** *Comment Status* **D** *Editorial*

Equations are written in a mixed style that is inconsistent with the document and, in some cases, difficult to parse. For example, I1 is Written as I1 in Step 1b (error) and the equations for I1 and Reff1 are not written as proper quotients.

SuggestedRemedy

Revise the subscripts and mathetmatical formulae in this section to reflect the style of other equations and variables in the document.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Editor to have license

Cl **79** *SC* **79.3.2** *P* **207** *L* **35** # 153

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Pres: Wendt1*

We decided to have two TLV figures one for the old types and one for the new Type 3 and Type 4 fields.
See presentation "wendt_1_1115_LLDP_Extensions_vxxx.pdf" and related baseline proposal

SuggestedRemedy

Implement wendt_1_1115_LLDP_Baseline_vvxxx.pdf

Proposed Response *Response Status* **W**

wfp

Cl **79** *SC* **79.3.2.6b.** *P* **212** *L* **28** # 205

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **X** *LLDP*

System using LLDP would benefit from communicating whether a DS PD has, isolated loads, or nonisolated loads. The data is reported for all PD types whether SS or DS.

SuggestedRemedy

Replace "Reserved" field, Bit 1, in Table 79-6b, with, "PD Load". For this row replace the Value/meaning with, "1 = PD power demand on Modes A and B are electrically isolated. 0 = PD power demand on Modes A and B are not electrically isolated."

On page 211, line 48, replace the existing sentence,
"The System setup value field shall contain the device bit-map of the Power type, PD 4P-ID, and PD PI defined in Table 79-6b and is reported for the device generating the TLV."

With "The System setup value field shall contain the device bit-map of the Power type, PD 4P-ID, PD PI, and PD Load defined in Table 79-6b and is reported for the device generating the TLV."

Add "79.3.2.6b.4 PD Load
This field shall be set according to Table 79-6b when the power type is PD. Electrically isolated for this Bit filed shall mean greater than or equal to 50 k-ohm resistance between any one connection of Mode A and any one connection on Mode B, when measured using at least VPort_PSE-2P minimum for Type-4 PSEs. This field shall be set to 0 when the power type is PSE."

Proposed Response *Response Status* **W**

TFTD

Cl **79** *SC* **79.3.2.6c** *P* **212** *L* **46** # 155

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Pres: Wendt1*

We agreed to change measurements to the verbose system as proposed in "yseboodt_3_0915_v120.pdf" and move these into a new optional TLV subtype.
See presentation "wendt_1_1115_LLDP_Extensions_vxxx.pdf" and related baseline proposal

SuggestedRemedy

Implement wendt_1_1115_LLDP_Baseline_vvxxx.pdf

Proposed Response *Response Status* **W**

wfp