Cl **1** *SC* **1.4.289** *P* **24** *L* **29** # r02-85

Thompson, Geoffrey — Individual

Comment Type **TR** *Comment Status* **X** *Definitions*

The definition for "link section" has been updated in the revision of 802.3 (Ref: P802.3cj, cl. 1.4.289 quoted below) therefore the change to the base standard requested on page 24, line 29 (1.4.254) is not needed.

1.4.289 link section: The point-to-point medium connection between the active PSE Power Interface (PI) and the PD PI.

SuggestedRemedy

Remove the change to the base standard detailed on page 24, lines 28 through 31 (labeled as cl. 1.4.254) from the draft for P802.3bt.

Proposed Response *Response Status* **W**

TFTD

TFTF CJ
D3.2
1.4.254 link section: The portion of the link segment from the PSE to the PD.

802.3cj:
1.4.289 link section: The point-to-point medium connection between the active PSE Power Interface (PI) and the PD PI.

802.3:
1.4.255 link segment: The point-to-point full-duplex medium connection between two and only two Medium Dependent Interfaces (MDIs).

TFTD LY
This new definition no longer indicates the relation between the link section and the link segment. A merged version:
"1.4.254 link section: The part of the link segment between the active PSE PI and the PD PI."

Cl **1** *SC* **1.4.338** *P* **24** *L* **40** # r02-10

Jones, Chad — Cisco Systems, Inc.

Comment Type **ER** *Comment Status* **D** *Definitions*

here is this definition without the editing instructions (so, as it will be published):
1.4.338 Power Sourcing Equipment (PSE): A DTE or midspan device that provides the power to a single link section. PSEs are defined for use with two different types of balanced twisted-pair PHYs. When used with 2 or 4 pair balanced twisted-pair (BASE-T) PHYs, see IEEE Std 802.3, Clause 33 and Clause 145, Power over Ethernet is intended to provide a single 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a unified interface for both the data it requires and the power to process these data. When used with single balanced twisted-pair (BASE-T1) PHYs (see IEEE Std 802.3, Clause 104), Power over Data Lines is intended to provide a single 100BASE- T1 or 1000BASE-T1 device with a unified interface for both the data it requires and the power to process these data. A PSE used with balanced single twisted-pair PHYs is also referred to as a PoDL PSE.

Not sure why we chose to use a different sentence construct for PoE than used for PoDL. The PoE sentence reads poorly. Restore the PoDL sentence construct to the PoE sentence. WIthout the parenthesis around the pointers to the clauses, it feels like this is a sentence that is missing a period after 'Clause 145'.

SuggestedRemedy

Change: When used with 2 or 4 pair balanced twisted-pair (BASE-T) PHYs, see IEEE Std 802.3, Clause 33 and Clause 145, Power over Ethernet is intended to provide a single 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a unified interface for both the data it requires and the power to process these data.

to: When used with 2 or 4 pair balanced twisted-pair (BASE-T) PHYs (see IEEE Std 802.3, Clause 33 and Clause 145), Power over Ethernet is intended to provide a single 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a unified interface for both the data it requires and the power to process these data.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
AAARGH Confusing.
Confirm that what you are asking is undoing the strikeout of the paranthesis around "(see IEEE Std 802.3 ...)".
Also, it will publish precisely the way you see it, with strikeouts and underlines.
Those only go away when our amendement gets pulled in to 802.3-2021 (or whatever year).

TFTD GT
Needs group discussion. What is there goes too far into being a specification instead of a definition.
I think it needs to be heavily pruned.

Cl **79** *SC* **79.3.2** *P* **86** *L* **15** # r02-25

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *Maintenance*

OOS

"The DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79-3 can be used by the PSE only when it is supplying power to a PI encompassed within an MDI and by the PD only when it is drawing power from the PI."

Imagine a PD connected through a Midspan (supplying power) to a PSE (not supplying power, because midspan in the way).
If that PSE sends out PoE TLVs, whatever value it puts in the PSEAllocatedPowerValue would be wrong.
Hence the quoted statement, saying this is not allowed.

However, the word "can" is used, when it needs to be a "shall".
Because this suggested remedy would create a new requirement on legacy devices, an MR has been filed in support.

SuggestedRemedy

Change sentence to say:
"The DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79-3 shall not be sent by the PSE unless it is supplying power to a PI encompassed within an MDI and by the PD unless it is drawing power from the PI."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

As the commentor states, this needs to be handled through the maintenance process.

TFTD LY
The maintenance request is against the base standard, which differs substantially from what we currently have in our draft. We need this remedy against our draft, not the remedy from the MR.

TFTD GT
Not sure that I agree that it needs to be handled through maintenance.
Seems like a basic flaw that, at a minimum, needs more discussion.

Cl **79** *SC* **79.3.2.6d** *P* **93** *L* **51** # r02-26

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *LLDP*

OOS

"The 'System setup' field shall contain the device bit-map of the Power Type ext and PD Load defined in Table 79-6f and is reported for the device generating the TLV. The value of the 'System setup' field transmitted by a PSE is undefined."

That last sentence is utter nonsense.

SuggestedRemedy

Strike "The value of the 'System setup' field transmitted by a PSE is undefined."

Proposed Response *Response Status* **W**

TFTD

How is the PSE supposed to fill out the device bit-map of Power Type ext and PD Load for the itself? (The sentence before says it is for the device generating the TLV.)

TFTD LY
The PSE fills out its own Type ('for the device generating the TLV') and '0' for PD load as required by 79.3.2.6d.2.

TFTD YD
"Yair: The commenter is correct. The text ""System setup' field transmitted by a PSE is undefined"" need to be deleted or defined but can't stay as undefined. In addition, the previous text already said that the field is filled by the device generating the TLV which means that for Power Type Ext the field can be filled by Yair: the PSE or by the PD (both may have the info). Regarding PD load field, the PD knows itself so the PD will fill up the field. "

Cl **145** *SC* **145.2.5.4** *P* **127** *L* **20** # r02-108

Darshan, Yair

Comment Type **T** *Comment Status* **D** *PSE SD*

The text "This variable is set per this description." that we add to several variables looks that it doesn't add any value.
See http://www.ieee802.org/3/bt/public/nov17/yseboodt_06_1117_final.pdf

SuggestedRemedy

Delete the text in this variable and all others where it is used or explain why we need it.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This text was added to make it clear which variables were allowed to be set by the PSE at any time and which variables need to follow the definition.

For example the variable you pointed out:

iclass_lim_det
A variable indicating if any IClass measured by the PSE during do_classification is invalid or equal
to or greater than IClass_LIM min as defined in Table 145–14. This variable is set per this description.
Values:
FALSE: Measured IClass is not invalid or is less than IClass_LIM min during do_classification
or this function is not active.
TRUE: Measured IClass is invalid or equal to or greater than IClass_LIM min during do_-classification.

Must be set by the definition (the PSE can't choose what to set this to).

TFTD YD
Why you reject my comment if you have accepted the 2nd option of the remedy (to explain it..)?

Response DNA: Ok, I have explained it. If you are happy with my explanation, I would suggest that you withdraw the comment.

Cl **145** *SC* **145.2.5.4** *P* **127** *L* **51** # r02-107

Darshan, Yair

Comment Type **E** *Comment Status* **X** *Pres: Yseboodt2*

The link to MirroredPDAutoclassRequest is Table 145-39 and not Table 145-38.

SuggestedRemedy

Change from Table 145-38 to Table 145-39

Proposed Response *Response Status* **W**

TFTD

Table 145-38 is for PSEs (thus I would expect to find it here). Table 145-39 is for SS PDs. This variable is output by the PSE SD so I would think Table 145-38 is correct, do we need to move it?

TFTD LY
See yseboodt_0118_02_dllmappings.pdf. There are multiple goofs in Table 145-38 and 145-39.

TFTD YD
Yair: MirroredPDAutoclassRequest is used by the PSE autoclass state machine in page 147 and then in PSE LLDP variable list in page 231 and then in Fig 145-39 PSE DLL state machine and then in Table 145-39 page 244 which is cross ref Table for single-signature PDs so the link is Table 145-39 where this variable is there and not Table 145-38 where it is not there. (The variable is a Mirror to something which is what PSE expect to have from the remote device which is the PD in this case)

Cl **145** *SC* **145.2.5.4** *P* **130** *L* **49** # r02-101

Johnson, Peter

Comment Type **T** *Comment Status* **X** *PSE SD*

The state variables 'power_available', 'power_available_pri', and 'power_available_sec' are described as "This variable may be set by the PSE at any time." This does not seem to be true in the state machine as this variable only appears in the POWER_ON state. It is not a pre-condition of powering a PD.

SuggestedRemedy

Alter the description in each of these three variables to be "This variable is set per this description." Perhaps expand the variable description to include "during normal operating state" or something to that effect.

Proposed Response *Response Status* **W**

TFTD

I think the answer is that the PSE can set this variable at any time, but it is only checked in the PowerON states.

TFTD YD
Yair: A variable may be specified at any time such as power_available, power_available_pri/sec regardless when it is the first time it is being used however in this case to use "This variable is set per its description." is more suitable.

Cl **145** *SC* **145.2.5.4** *P* **133** *L* **14** # r02-102

Johnson, Peter

Comment Type **T** *Comment Status* **D** *PSE SD*

The state variables 'pse_reset', 'pse_reset_pri', and 'pse_reset_sec' include the description "This variable is set per this description". However, it's not clear why these variables cannot be manipulated at any time the by the PSE.

SuggestedRemedy

Change description to "This variable may be set by the PSE at any time."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

While it does say that it is set according to the description, the description includes "It is also TRUE when implementation-specific reasons require reset of PSE functionality."

TFTD YD
Yair: Pete is correct. This variable should be set at any time. We always agree the we can set PSE reset at any time. We discuss it many times whenever we wanted to add exit to IDLE/IDLE_PRI/SEC to allow some features. Propose to ACCEPT.

Cl **145** *SC* **145.2.5.4** *P* **133** *L* **39** # r02-109

Darshan, Yair

Comment Type **T** *Comment Status* **D** *PSE SD*

In the following text Class 0 should be adressed as well:
"pse_ss_mode
A variable that controls whether the PSE provides power over 2 pair or 4 pair to a single-signature
PD assigned to Class 1 through Class 4. This variable may be set by the PSE at any time.
0: Single-signature PD is powered over 2 pair.
1: Single-signature PD is powered over 4 pair."

Type 3 or 4 PSEs that detects PD with class 0 which they have to support over 2-pairs and allowed to support it over 4-pairs as well are not covered by the above variable description.

In adition, it is not sufficient that in Table 145-11 class 0 is adressed i.e. the rest of the spec in the PSE section need to be sync to it by simply change all ocurences of "class 3 = Class 3" to "Class 0, Class 3" and from "Class 1 to Class X" to "Class 0 to Class X". These are covered by seperate comments.

SuggestedRemedy

Change the text to:
"pse_ss_mode
A variable that controls whether the PSE provides power over 2 pair or 4 pair to a single-signature
PD assigned to Class 1 through Class 4. Class 0 PD is treated as Class 3 PD.This variable may be set by the PSE at any time.
0: Single-signature PD is powered over 2 pair.
1: Single-signature PD is powered over 4 pair."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The description clearly says "asigned to Class 1 through Class 4". PDs that request Class 0 get assigned to Class 3, thus the current description is correct and does not need to be changed.

TFTD YD
Yair: Where we have explicit text that says PDs that request class 0 get assigned to class 3 with a shall ? IF there is such a text then ACCEPT IN PRINCIPLE this comment and show where the text is with no further changes to the draft.

Response DNA: While looking for this I did notice that the reference to table 145-11 in the definition of pd_class_sig on page 138, line 11 is wrong. It should be 145-13, right? Also, I don't think there is a "shall" in text that says this, although table 145-11 does show it. It is covered by the shall for the SD and the behavior is shown in the MARK_EV_LAST state where it says "If pd_class_sig = 0 then pse_allocated_pwr <= 3)"

Cl **145** *SC* **145.2.5.6** *P* **138** *L* **20** # r02-98

Johnson, Peter

Comment Type **T** *Comment Status* **X** *PSE SD*

The Functions 'do_classification_pri' and 'do_classification_sec' seem highly unconventional as they seem to operate at two levels of the Primary and Secondary PSE state machines. On a per class event level, they (presumably) produce class signatures. But additionally, they return the variables pd_req_pwr_pri (sec) and pd_allocated_pwr_pri (sec) that really should come from CLASS_EVAL_PRI and CLASS_EVAL_SEC, as seems to be the case in the top level (single signature) state machine where the Function 'do_classification' simply returns the class signature from a single event as shown in the state diagrams.

SuggestedRemedy

If this is truly seen to be an issue, then 'do_classification_pri' (and sec) should just return class signatures per class event and the variables pd_req_pwr_pri (sec) and pd_allocated_pwr_pri (sec) should be defined along with pd_req_pwr in 145.2.5.4.

Proposed Response *Response Status* **W**

TFTD

I don't believe this is seen to be an issue.

TFTD YD
Yair: The commenter arguments seems incorrect. All the arguments are covered by the description of pd_req_pri. I don’t see any issue here so no changes are needed.

Cl **145** *SC* **145.2.5.6** *P* **140** *L* **26** # r02-100

Johnson, Peter

Comment Type **T** *Comment Status* **D** *PSE SD*

The state variable 'option_vport_lim' (and ..._pri , ... _sec) are shown as being returned by the Function 'do_initialize'. This does not seem to be consistent with the purpose of these variables that are defined to report an operating condition during the POWER_ON state, albeit the purpose of 'do_initialize' is not clear in the PSE state machine. First problem is that the variable 'option_vport_lim' is not used anywhere in state processing. Further, the 'pri' and 'sec' versions of these variables are processed identically to 'short_det_pri', 'short_det_sec', 'overld_det_pri' and 'overld_det_sec'. They all have meaning only during the POWER_ON state.

SuggestedRemedy

Remedies: 1) Remove from 'do_initialization' 2) Remove 'option_vport_lim' altogether 3) Specify in the definitions of 'option_vport_lim_pri' and 'option_vport_lim_sec' that "This variable is set per this description" much like the write-ups for 'overld_det_pri' and 'short_det_pri'.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
"There are two problems here:1. option_vort_lim is not used by the state machine. It is covered by option_vort_lim_pri/sec that are embedder in the error_pri/sec variable.2. option_vort_lim_pri/sec need to be set per its description (and also can be set at any time- To discuss what is best).Update the proposed remedy to be with more explicit instructions: 1. Delete option_vport_lim variable from the spec (variable list).2. Remove option_vort_lim and option_vort_lim_pri/sec from do_initialization3. Add the following text to option_vort_lim_pri and to option_vort_lim_sec: ""This variable is set per its description."""

Cl **145** *SC* **145.2.7** *P* **142** *L* **1** # r02-141

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan3*

PSE state machine need to be updated per the updated simulation results

SuggestedRemedy

Adopt darshan_03_0118.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.7** *P* **142** *L* **9** # r02-138

Darshan, Yair

Comment Type **T** *Comment Status* **D** *PSE SD*

pse_allocated_pwr is set to zero in the IDLE state although in CLASSIFICATION state (page 144) we have the same initialization. The proper place is to use it in CLASSIFICATION which is the first time we need it and we have it there.

SuggestedRemedy

Remove pse_allocated_pwr from IDLE.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
There are all kinds of ways to get to IDLE with this variable set to a previous result. It is cleaner to also reset it to zero in IDLE.
Propose to leave it.

Cl **145** *SC* **145.2.7** *P* **142** *L* **14** # r02-136

Darshan, Yair

Comment Type **T** *Comment Status* **X** *PSE SD*

In the IDLE state, the do_initialize function return the variable alt_pri (in which "a" or "b" is set) and also pse_alternative is set (which Pinouts Alternative PSE uses A, B or both))".
Later, still in IDLE state, we have the following IF statement:
IF (pse_alternative != both) THEN
alt_pri <== pse_alternative
END
The problem is that to initialize alt_pri in two locations in the same state is redundant and confusing.
Proposal
1. To delete alt_pri from the function do_initialize on page 140 line 17.
2. To restore what we had in D3.1:
IF (pse_alternative != both) THEN
alt_pri <== pse_alternative
ELSE alt_pri <== user defined
END.

SuggestedRemedy

1. To delete alt_pri from the function do_initialize on page 140 line 17.
2. To restore what we had in D3.1:
IF (pse_alternative != both) THEN
alt_pri <== pse_alternative
ELSE alt_pri <== user defined
END

Proposed Response *Response Status* **W**

TFTD

TFTD LY
"user defined" is not valid state diagram syntax.
alt_pri is a choice of a 4-pair PSE, but is mandated for a 2-pair PSE.
That is precisely what the current assignments do.
While it IS being double-assigned here (in case of 2P), it does provide correct behavior.

Cl **145** *SC* **145.2.7** *P* **144** *L* **33** # r02-137

Darshan, Yair

Comment Type **T** *Comment Status* **D** *PSE SD*

In comment r01-174 (D3.1) we did some changes that are not required.
In the exit from CLASS_EV2 to MARK_EV2 we add the variable "*(pse_alternative=both)"
In the exit from CLASS_EV2 to MARK_EV_LAST we add the variable "*(pse_alternative != both)"
This is not required since the argument that was used to justify this change can't happen since pse_allocated_pwr is set to 4 in CLASS_EV2 and can't be higher then 4.

SuggestedRemedy

Restore to D3.1 all the changes done for comment r01-174.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This change was implemented to make sure that 2-pair PSEs don't give more than 2 class events (since they can't ever supply more than class 4).

TFTD YD
Yair:
(1) I disagree that this was the reason for the change i.e. that 2-pair PSE don't give more than 2-class events if pse_avail_pwr=4. If pse_avail_pwr>4 it can issue 3 class events for 4-pairs but the 4-pair test should not be done here at the exit from CLASS_EV2. It is already done at the exits of CLASS_EV3.
The facts are:
a) When pse_avail_pwr=4, PSE working over 2-pais OR 4-pairs, can issue 3 class events if option_2ev=FALSE. It has the same meaning for the PD in terms of available power.
b) Lennart in his corner case presented in r01-174, explained that in the exit from CLASS_EV2 to MARK_EV2 the reason for his proposed changes was to address the corner case when option_2ev=TRUE and yet we issue 3 class events in the exit from CLASS_EV2 to MARK_EV2 which is the wrong way to address it.
-We issue 3 class events because pse_avail_power>4 and !option_2ev=0 which is still the correct logic in this exit. The correct way to fix his is shown below in (3).
(2) The other problem that I had is that Lennart in his arguments to r01-175 mention pse_allocated_pwr>4 which can't be the reason for the proposed changed in D3.1 since pse_allocated_pwr=4 was already assigned in CLASS_EV2. I guess it was a typo and Lennart meant to say pse_avail_pwr>4. (Lennart confirmed it.)
(3) The logic of the exit from CLASS_EV2 to MARK_EV2 is incorrect because this exit is only about the conditions to permit 3 class events when the 2nd pd_class_sig=4 regardless if PSE is operated over 2-pairs or 4-pairs since this condition is tested already at the exits of CLASS_EV3 and should not be tested now. The only ways to exit from CLASS_EV2 to MARK_EV2 are:
a) tcev_timer_done *(pd_class_sig = 4) * !option_2ev * (pse_avail_pwr = 4) [This solve Lennart problem in r01-174]
OR
b) tcev_timer_done *(pd_class_sig = 4) * (pse_avail_pwr > 4) [this allows 3 class events for the normal path when pse_avail_power>4 regardless of option_2ev] which results with:
tcev_timer_done * (pd_class_sig = 4) * ((pse_avail_pwr > 4) +)(pse_avail_pwr = 4) * !option_2ev( )
(4) The logic of the exit from CLASS_EV2 to MARK_EV_LAST done to prevent multiple true due the changes made for CLASS_EV2 to MARK_EV2 and is not required due to the above discussion i.e.:
tcev_timer_done *(pd_class_sig = 4) * option_2ev * ((pse_avail_pwr = 4) + (pse_alternative!=BOTH)) as it was in D3.1.
Proposed Remedy:
1. Change the exit from CLASS_EV2 to MARK_EV_LAST from:
tcev_timer_done *option_2ev *((pse_avail_pwr = 4) +(pse_alternative ≠ both)) *(pd_class_sig = 4)
To:
tcev_timer_done *option_2ev *(pse_avail_pwr = 4) * (pd_class_sig = 4)
2. Change the exit from CLASS_EV2 to MARK_EV2 from:
tcev_timer_done * (pd_class_sig = 4) * (((pse_avail_pwr > 4) * (pse_alternative = both)) + !option_2ev)
To:
tcev_timer_done * (pd_class_sig = 4) * ((pse_avail_pwr > 4) +)(pse_avail_pwr = 4) * !option_2ev( )

Cl **145** *SC* **145.2.5.7** *P* **147** *L* **42** # r02-91

Law, David Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *PSE SD*

The variable pse_dll_ready is not defined in subclause 145.2.5.4 'Variables', but used in Figure 145-14.

SuggestedRemedy

Suggest that the following is added to subclause 145.2.5.4 'Variables':

pse_dll_ready: See pse_dll_ready in 145.5.3.2.2.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
Yair: The remedy is OK but it is better that the full definition of pse_dll_ready (from 145.5.3.2.2) will be in 145.2.5.4 and in 145.5.3.2.2 we will have "See pse_dll_ready in 145.2.5.4.".

Cl **145** *SC* **145.2.5.7** *P* **148** *L* **17** # r02-133

Darshan, Yair

Comment Type **T** *Comment Status* **X** *PSE SD*

This comment is marked AVI_22 in D3.1 COMMENT 433 and was not resolved fully by http://www.ieee802.org/3/bt/public/nov17/yseboodt_03_1117_final.pdf as indicated by the remedy for r01-433.
The variable det_start_pri is set to TRUE in INIT_PRI. In case CC_DET_SEQ=2 the variable det_start_pri is set to TRUE after detection is done and the purpose of this variable is to indicate when detection is start which is the primary tells the secondary that it is between START_DETECT and POWER_UP.
In addition, in all other CC_DET_SEQ sequences, det_start_pri is set to TRUE in INIT_PRI and then again in START_DETECT_PRI which is redundant.
The solution is to move "det_start_pri <== TRUE" from INIT_PRI to START_CXN_CHK_DETECT which is the correct place for CC_DET_SEQ=2.
The same problem applies to the secondary as well.

SuggestedRemedy

1. Move "det_start_pri <== TRUE" from INIT_PRI to START_CXN_CHK_DETECT on page 142.
2. Move "det_start_sec <== TRUE" from INIT_SEC to START_CXN_CHK_DETECT on page 142.

Proposed Response *Response Status* **W**

TFTD

Can a SD expert help me check this?

Cl **145** *SC* **145.2.6.1** *P* **157** *L* **17** # r02-34

Yseboodt, Lennart Philips Lighting

Comment Type **E** *Comment Status* **D** *Editorial*

OOS

Detection and connection check are two different things, operating at about the same level. And yet, the connection check subclause (145.2.6.1) is under the detection subclause (145.2.6).

It would make more sense to have connection check sit at the same level as detection. What do we do with the 4PID subclause, which has depencies on detection, cc, classification, and mutual ID.

If we structure things roughly in the same way as they happen, we should have all of them sit at the 145.X.Y level in this order:
145.2.6 Detection
145.2.6a Connection check
145.2.7 PSE classification of PDs and mutual ID
145.2.7a 4PID requirements
145.2.8 Power supply output

SuggestedRemedy

Reshuffle subclauses as follows:
145.2.6 PSE detection of PDs [NO CHANGE]
145.2.6a Connection check [Bump up 1 level, change subclause title, move here]
145.2.7 PSE classification of PDs and mutual ID [NO CHANGE]
145.2.7a 4PID requirements [Bump up 1 level, move here]
145.2.8 Power supply output [NO CHANGE]

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD

Cl **145** *SC* **145** *P* **157** *L* **45** # r02-1

Anslow, Peter — Ciena Corporation

Comment Type **TR** *Comment Status* **D** *Editorial*

The response to unsatisfied comment r01-30 against D3.1 was:
"REJECT.
The comment resolution group believes that the em-dash is technically inaccurate for these entries as it means there is "a lack of data". In Clause 145 the empty cells are due to openended ranges, not a lack of data."
In order to clarify the meaning of an em-dash in tables within 802.3, a comment has been submitted against the revision project with the following suggested remedy
Add a new subclause 1.2.8:
1.2.8 Em dash (--) in a table cell
A table cell containing an em-dash (--) indicates a lack of data for that cell, or:
- For a units cell, that there is no unit for that parameter
- For a maximum cell, that there is no requirement on the maximum value of that parameter
- For a minimum cell, that there is no requirement on the minimum value of that parameter

SuggestedRemedy

Make sure all tables have an entry of em-dash or pointer to the requirement in currently blank min or max columns in accordance with all other recent amendments to IEEE 802.3. In particular, Tables 145-7, 145-8, 145-9, 145-10, 145-14, 145-15, 145-16, 145-21, 145-25, 145-28, 145-29, 145-32, 145-33.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
Let's see what happens in the revision meeting to the comment that add the "em-dash" text and accept / revise accordingly.

Cl **145** *SC* **145.2.6.5** *P* **159** *L* **52** # r02-35

Yseboodt, Lennart — Philips Lighting

Comment Type **E** *Comment Status* **D** *PSE Detection*

OOS

"The PSE shall reject as an invalid detection signature, a pairset which exhibits any of the following characteristics as defined in Table 145-10."

Typical of AF-era text it refers to things by relative position. Problem is, what follows is Table 145-9, not the list that is being referred to.

SuggestedRemedy

Fix as follows:
"The PSE shall reject as an invalid detection signature, a pairset which exhibits any of the following characteristics:" [FRAME: keep with next]
" a) Resistance less than or equal to R bad min, or
b) Resistance greater than or equal to R bad max, or
c) Capacitance greater than or equal to C bad min. " [FRAME: keep with next]
"R bad min, R bad max, and C bad min are defined in Table 145-10."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD HS
r02.35 creates text that is redundant with a table and is OOS. It is also deemed moot by r02-14.

Response CJ:
Yes 2-14 and 2-35 both address the same problem and both are accepts. I don't think 2-35 adds any new text or changes anything. He simply includes the Frame commands needed to ensure the section stays together with the table.

Cl **145** *SC* **145.2.7** *P* **161** *L* **25** # r02-36

Yseboodt, Lennart — Philips Lighting

Comment Type **E** *Comment Status* **D** *Editorial*

OOS

"The PD responds to each class event with a current representing one of a limited number of class signatures. The class signatures generated by the PD indicate the PD requested Class. See Table 145-26 and Table 145-27 for a mapping of class signature to the PD requested Class."

This is the first attempt at defining the PD requested Class. Given that we have removed Class 0 (compared to Type 1), this seems a good place to mention that.

SuggestedRemedy

Add a note after this paragraph:
"NOTE --- For Type 3 PDs, a requested Class 0 is not defined. Type 1 PDs that did not implement Physical Layer classification requested Class 0, with a power level equivalent to Class 3."

Insert the same note in 145.3.6.1, on page 201, line 4.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
"Yair: The proposed note construct was not worded in a clear way. ""NOTE --- For Type 3 PDs, a requested Class 0 is not defined.[this part is OK]"" Type 1 PDs that did not implement Physical Layer classification requested Class 0, with a power level equivalent to

Class 3."" This part is not clear. Instead use: "" Type 1 PDs that did not implement Physical Layer classification has a requested Class 0, with a power level equivalent toClass 3""In addition, in the PSE section we need a shall statement ""PSE when connected to PD that requires class 0, shall be treated as class 3."" or equivalent."

Cl **145** *SC* **145.2.7** *P* **162** *L* **19** # r02-112

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Pres: Darshan2*

In D3.1 we had the text "PSEs that have additional information about the actual link section DC resistance or temperature conditions may choose to use a lower Autoclass margin than that defined by Equation (145-4)." and it was removed in D3.2. It is better if it will be restored since the difference between worst case margin Pac_margin and the actual margin required is not negligible.

SuggestedRemedy

Add the following text after line 21 in page 162:
"PSEs that have additional information about the actual link section DC resistance or temperature conditions may choose to use a lower Autoclass margin than that defined by Table 145-15."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This sentence was removed intentionally because the amount of margin required was drastically reduced.

TFTD YD
"Yair: The argument for rejection looks incorrect to me:-In the Pac_margin presented last time there are errors so they are not correct.-In addition, the Pac_margins per the new calculations are higher than in D3.2. See darshan_02_0118.pdf-Even with the current numbers in the spec for class 7 and 8, the margins are not negligible they are above 1W for class 8 and with thousands of ports we get several KW margins.-Normally the spec is defined at room temperature and it is the system vendor responsibility to add the correct margins for temperature as we do for all other parameters and as we do when we specified Pclass in the usual powering states. So now if we add Pac_margin, lets do it correctly with all the flexibility needed. -In addition, in principle, how we can justify that if the ""margin is low"" the text that ""if we know the actual temperature and resistance, we can use lower margin"" is redundant, this is in contradiction with what we are trying to do which is make efficient power management. I am proposing to ACCEPT my proposal."

Cl **145** *SC* **145.2.7** *P* **162** *L* **22** # r02-113

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Autoclass*

I don't see the justification to remove the text from D3.1: "PSEs that have additional information about the actual link section DC resistance or temperature conditions may choose to use a lower Autoclass margin than that defined by Equation (145-4)."

SuggestedRemedy

Append the following text after line 21: "PSEs that have additional information about the actual link section DC resistance or temperature conditions may choose to use a lower Autoclass margin than that defined by Equation (145-4)."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This sentence was removed intentionally because the amount of margin required was drastically reduced.

TFTD YD
Yair: Make this comment OBE to 113.

Response DNA: I assume you meant to OBE it to 112. I can't do that as this would be an AIP, but 112 is unresolved and may not be an accept. We will revisit this comment after 112 is resolved.

Cl **145** *SC* **145.2.7.1** *P* **165** *L* **23** # r02-39

Yseboodt, Lennart Philips Lighting

Comment Type **T** *Comment Status* **X** *Classification*

OOS

"PSEs shall issue no more class events than the Class they are capable of supporting between the most recent time V PSE was at V Reset for at least T Reset and a transition to any of the power up states."

Nothing wrong with this sentence, however it is incomplete.
A PSE is also not allowed to create 'redundant extra' class events (eg. 2 events for a PD that requests Class 3).

While this proposed shall is duplicate to the state diagram, it is important enough to warrant a PICS entry of its own.

SuggestedRemedy

Add the following after the quoted sentence.

"PSEs connected to a single-signature PD shall issue no more than:
- one class event when the PD requests Class 1 through 3
- three class events when the PD requests Class 4
- four class events when the PD requests Class 5 or 6
- five class events when the PD requests Class 7 or 8
between the most recent time V PSE was at V Reset for at least T Reset and a transition to any of the power up states.

PSEs connected to a dual-signature PD shall issue, for a given pairset, no more than:
- three class events when the PD requests Class 1 through 4
- four class events when the PD requests Class 5
between the most recent time V PSE was at V Reset for at least T Reset and a transition to any of the power up states."

Proposed Response *Response Status* **W**

TFTD

This new sentence includes a shall that seems to be a redundand, more specific shall than the sentence already there. Should we remove the shall from one of the sentences?

TFTD LY
The requirements are distinct: one is about not issuing more class events than the PSE has power for, the other is about not producing more class events than the requested Class calls for.
We could merge them however:
"PSEs connected to a single-signature PD shall issue no more class events than the Class they are able to support and no more than:
- one class event when the PD requests Class 1 through 3
- three class events when the PD requests Class 4

- four class events when the PD requests Class 5 or 6
- five class events when the PD requests Class 7 or 8
between the most recent time V PSE was at V Reset for at least T Reset and a transition to any of the power up states.
PSEs connected to a dual-signature PD shall issue, for a given pairset, no more class events than the Class they are able to support and no more than:
- three class events when the PD requests Class 1 through 4
- four class events when the PD requests Class 5
between the most recent time V PSE was at V Reset for at least T Reset and a transition to any of the power up states."

Response DNA: Ok, I get your point, but this is a shall that is redundant to the SD. Do we want it called out like this, or stated without a shall?

TFTD YD
"Yair: Definitely, we don't need two shalls for the same requirement.In addition, before we move on with this comment, to check with other PSE system vendors that we could in 802.3at to issues 2 class events constantly for any class between class 0 to 4. The reason that I am mentioning this is that if in the future we want to replace Type 2 PSEs with Type 3 PSEs that supports only 30W to variety of PDs in the range of class 0-4, we can still do it."

Cl **145** *SC* **145.2.7.2** *P* **167** *L* **7** # r02-41

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *Autoclass*

"If the PSE implements Autoclass it shall measure P Autoclass when it reaches the POWER_ON state and pd_autoclass is TRUE. P Autoclass is the power provided by the PSE measured throughout the period bounded by T AUTO_PSE1 and T AUTO_PSE2 , defined in Table 145-15."

For assigned Class 1-4, if the PSE measures Autoclass in 4P mode, and then switches to 2P mode, the channel losses will roughly double.
Given that the PSE does not know what the PD power is, it cannot guarantee interoperability.

Proposed solution is to require PSEs that plan to transition back into 2P mode, to also make the Autoclass measurement in 2P mode.

SuggestedRemedy

Append sentence at the end of the quoted text:

"Autoclass enabled PSEs that have assigned Class 1 through 4, and have measured PAutoclass in 4-pair mode, shall not transition to 2-pair mode".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Add "Note--PSEs that have measured Pautoclass in 4-pair mode should account for the increased channel resistance if transitioning to 2-pair mode."

after line 16

TFTD LY
A note is insufficient -- this presents an interoperability problem and needs to be a requirement.
Alternative requirement:
"Autoclass enabled PSEs that may transition from 4-pair to 2-pair mode shall perform the Autoclass measurement in 2-pair mode."

Response DNA: why not have a shall that requires PSEs to add the necessary margin in this case…

Cl **145** *SC* **145.2.7.2** *P* **167** *L* **22** # r02-42

Yseboodt, Lennart Philips Lighting

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt1*

OOS

The Autoclass timings T_AUTO_PSE1 and T_AUTO_PSE2 are referenced "from the transition of POWER_UP to POWER_ON".

This has two issues:
- it is not observable at the PSE PI when this happens, making it untestable
- the PSE and PD reference points can drift apart by as much as 75ms

While the timings do work out in any permutation, it makes it hard to comprehend.

SuggestedRemedy

Recommend to pick a new unified reference point, which is always the same for PSE and PD and possible adjust timings to compensate.
Adopt yseboodt_01_0118_autoclasstime.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.7** *P* **167** *L* **36** # r02-121

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan1*

Pac_margin calculations has some errors and need to be updated. See updates for Pac_margin value in darshan_01_0118.pdf.

SuggestedRemedy

Adopt darshan_01_0118.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8.1** *P* **168** *L* **25** # r02-129

Darshan, Yair

Comment Type **T** *Comment Status* **D**

Type 3 and 4 PSE when connected to class 0 PD need to support it as well. Table 145-16 items 5, 6 and 7: Class 1-4 need to be Class 0 to 4

SuggestedRemedy

In Table 145-16 items 5, 6 and 7:
Change "Class 1-4" to "Class 0 to 4"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Items 5, 6, and 7 are all dependent on "assigned class". Class 0 PDs are assigned to Class 3, thus they are included in the table already.

TFTD YD
Where we have explicit text that says PDs that request class 0 get assigned to class 3 with a shall ? IF there is such a text then show it in the response and REJECT. If there is no such text then add "IF PSE detects class 0 PD, it shall be treated as Class 3 PD."

Response DNA: See comment 109

Cl **145** *SC* **145.2.8.1** *P* **169** *L* **14** # r02-131

Darshan, Yair

Comment Type **T** *Comment Status* **D**

Type 3 and 4 PSE when connected to class 0 PD need to support it as well. Table 145-16 items 11: Class 1-3 need to be Class 0 to 3

SuggestedRemedy

In Table 145-16 items 11:
Change "Class 1-3" to "Class 0 to 3"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Item 11 is dependent on "assigned class". Class 0 PDs are assigned to Class 3, thus it is included in the table already.

TFTD YD
Where we have explicit text that says PDs that request class 0 get assigned to class 3 with a shall ? IF there is such a text then show it in the response and REJECT. If there is no such text then add "IF PSE detects class 0 PD, it shall be treated as Class 3 PD."

Response DNA: See comment 109

Cl **145** *SC* **145.2.8.1** *P* **169** *L* **45** # r02-132

Darshan, Yair

Comment Type **T** *Comment Status* **D**

Type 3 and 4 PSE when connected to class 0 PD need to support it as well. Table 145-16 items 18: Class 1-4 need to be Class 0 to 4 for 2-pair and 4-pair rows.

SuggestedRemedy

In Table 145-16 items 18 for 2-pair and 4-pair rows:
Change "Class 1-4" to "Class 0 to 4"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Item 18 is dependent on "assigned class". Class 0 PDs are assigned to Class 3, thus it is included in the table already.

TFTD YD
Where we have explicit text that says PDs that request class 0 get assigned to class 3 with a shall ? IF there is such a text then show it in the response and REJECT. If there is no such text then add "IF PSE detects class 0 PD, it shall be treated as Class 3 PD."

Response DNA: See comment 109

Cl **145** *SC* **145.2.8.6** *P* **175** *L* **54** # r02-122

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Inrush*

"Power up occurs on each pairset between the transition to a power up state on that pairset and the expiration of TInrush. PSEs that have assigned Class 5 to 8 to a single-signature PD shall reach POWER_UP on both pairsets within TInrush max, starting with the first pairset transitioning into the power up state, and where the second pairset transitions to a power up state anytime within this time period."
1. The above text doesn't cover single-signature PD class 1-4 operating only over 4-pairs regarding power up requirements. They should have the same requirements as for single-signature PD class 5-8.
2. The current text in page 175 lines 54 and page 176 lines 1-2 take care of the possibility to flip between 2P and 4P and is good however this text is also true for class 1-4 operating only over 4-pairs as well.
3. If we are working over 2-pairs only, no special requirements are needed for powerup because it is straight forward and explained in page 175 lines 52-53 as for when powerup occurs.

SuggestedRemedy

Change from: "Power up occurs on each pairset between the transition to a power up state on that pairset and the expiration of TInrush. PSEs that have assigned Class 5 to 8 to a single-signature PD shall reach POWER_UP on both pairsets within TInrush max, starting with the first pairset transitioning into the power up state, and where the second pairset transitions to a power up state anytime within this time period."
To: "Power up occurs on each pairset between the transition to a power up state on that pairset and the expiration of TInrush. PSEs connected to single-signature PD that operates over 4-pairs shall reach POWER_UP on both pairsets within TInrush max, starting with the first pairset transitioning into the power up state, and where the second pairset transitions to a power up state anytime within this time period."

Proposed Response *Response Status* **W**

TFTD

While I understand your point, the text and SD were designed this way intentionally. If I want to operate over 4-pairs for this class, I can start up in 2-pair (inrush over 2-pairs) and then switch to 4-pair whenever I like (assuming all the necessary detections were done before power up). We can add the option to inrush in 4-pairs (a may statement somewhere and a tweak to the SD), but I don't want to be required to inrush in 4-pairs for class 1-4 (particularly when the requirement is the same as 2-pair inrush).

TFTD YD
Yair: I agree that we should not force to inrush in 4-pairs class 0-4 however there is missing instructions how to handle this case which is impossible spec wise to leave it unspecified. I agree that text with "may" will be sufficient. I am not sure that we need to cover it in the state machine (but it will be nice to have).

Cl **145** *SC* **145.3.3.3.3** *P* **188** *L* **47** # r02-114

Darshan, Yair

Comment Type **T** *Comment Status* **D** *PD SD*

The definition of "tinrushpdmax_timer A timer used to prevent the PD from drawing more than IInrush_PD and IInrush_PD-2P from TInrush_PD to Tdelay; see TInrush_PD max in Table 145-29. " is incorrect this timer has nothing to do with Tdelay.

SuggestedRemedy

1. Change to:
"tinrushpdmax_timer A timer used to determine when the PD exits INRUSH; see TInrush_PD max in Table 145-29."
2. The same for dual-signature PD on page 195 clause 145.3.3.4.3:
Change to:
"tinrushpdmax_timer_mode(X) A timer used to determine when the PD exits INRUSH over Mode X; see TInrush_PD max in Table 145-29."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
exit INRUSH over Mode X... better make it:
"tinrushpdmax_timer_mode(X) A timer used to determine when the PD exits INRUSH for Mode X; see TInrush_PD max in Table 145-29."

Cl **145** *SC* **145.3.8.1** *P* **208** *L* **7** # r02-52

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **D** *Inrush*

"The PD shall turn off at a voltage in the range of V Off_PD."

Except when in the INRUSH state...

SuggestedRemedy

Replace by:
"The PD shall turn off at a voltage in the range of V Off_PD, except when in INRUSH."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

That seems really odd, how about "After reaching POWER_DELAY, the PD shall turn off at a voltage in the range of V Off_PD."

which actually matches what the SD does…

TFTD YD
Yair: The proposal "The PD shall turn off at a voltage in the range of V Off_PD, except when in INRUSH." is not good enough since it doesn't allow us to shut off the port in case the PD is short load and there is the voltage at the PD stuck below Voff_PD which is an error. The PD is required to successfully startup on the 1st trial i.e. it gets to POWER_DELAY. In this sense David A proposal seems better and doesn't add allowances to additional incompliant behavior.

Cl **145** *SC* **145.3.8.2** *P* **208** *L* **25** # r02-104

Bennett, Ken

Comment Type **T** *Comment Status* **D** *PD Power*

In table 145-29, the symbol for the parameter "input AVERAGE power" is defined as Pport_PD. Section 145.3.8.4.1, Peak Operating Power Exceptions, uses Pport_PD as an AVERAGE power for computations. (It's also described as an AVERAGE power in section 33.3.7.2.1 of the existing standard.)

The recent addition to 145.3.8.2 changes the Pport_PD definition to instantaneous power. This causes errors in 145.3.8.4.1 and it results in an ambiguity in table 145-29, where the symbol no longer matches the described parameter. The proposed solution changes Pport_PD and Pport_PD-2P back to an average power.

The Existing Text in Draft 3.2 is:

PPort_PD is the power drawn by a single-signature PD, defined in Equation (145-23). PPort_PD-2P is the
power drawn by a given Mode of a dual-signature PD, defined in Equation (145-24).
Pport_PD = VPD*Iport (145-23)
Pport_PD-2P = VPD*Iport-2P (145-24)
For single-signature PDs, the AVERAGE value of PPort_PD shall not exceed PClass_PD for the assigned class. For
a dual-signature PD, the AVERAGE value of PPort_PD-2P shall not exceed PClass_PD-2P for the assigned class.

SuggestedRemedy

Move the word "average" in lines 32 and 33 to lines 25 and 26, and modify the equations to represent the following:

PPort_PD is the AVERAGE power drawn by a single-signature PD, defined in Equation (145-23). PPort_PD-2P is the AVERAGE power drawn by a given Mode of a dual-signature PD, defined in Equation (145-24).

Pport_PD = the integral of VPD(t)*Iport(t) dt from t=n to (n+1) (145-23)
Pport_PD-2P = the integral of VPD(t)*Iport-2P(t) dt from t=n to (n+1) (145-24)

For single-signature PDs, the value of PPort_PD shall not exceed PClass_PD for the assigned class. For a dual-signature PD, the value of PPort_PD-2P shall not exceed PClass_PD-2P for the assigned class.

OPTION 1: Remove the equations:

PPort_PD is the AVERAGE power drawn by a single-signature PD. PPort_PD-2P is the AVERAGE power drawn by a given Mode of a dual-signature PD.
For single-signature PDs, the value of PPort_PD shall not exceed PClass_PD for the assigned class. For a dual-signature PD, the value of PPort_PD-2P shall not exceed PClass_PD-2P for the assigned class.

Proposed Response *Response Status* **W**

TFTD

TFTD YD
Yair: The proposed remedy is not sufficiently clear. Please copy the whole relevant text to a Word document and make the changes with editing marks so we can review it at the meeting.

Cl **145** *SC* **145.3.8.3** *P* **210** *L* **32** # r02-116

Darshan, Yair

Comment Type **T** *Comment Status* **D** *PD Power*

There is an error in the text "A dual-signature PD can also be implemented with a single load, resulting in a lower than Cx + Cy capacitance value as seen by the PSE.".
The value in this case generally will be lower than Cx+Cy but in this particular case of a single load it will be Cx.

SuggestedRemedy

Change from:
"A dual-signature PD can also be implemented with a single load, resulting in a lower than Cx + Cy capacitance value as seen by the PSE."
To: "A dual-signature PD can also be implemented with a single load, resulting in Cx capacitance value as seen by the PSE."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

As there is no picture to go with the single load, DS case, the suggested remedy would add confusion. What is in the current note is correct given that we don't show what the single load cap is called.

TFTD YD
Yair: Agree that if we want to make it clear, we need to add picture for dual-signature single-load. If the group is interested, I can supply the picture at the meeting.

Cl **145** *SC* **145.3.8.9** *P* **213** *L* **44** # r02-63

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *Unbalance*

"Single-signature PDs shall not exceed I Unbalance_PD-2P for longer than T CUT min and 5 % duty cycle, and shall not exceed I Unbalance_peak-2P , as defined in Table 145-31 on any pair when PD PI pairs of the same polarity are connected to any voltage in the range of V Port_PSE-2P min + 0.31 V to V Port_PSE-2P max through two common mode resistances, R source_min and R source_max, as defined in Equation (145-28) and shown in Figure 145-30."

... "when PD PI pairs of the same polarity are connected to any voltage in the range of" ... does not make sense.
We really want to indicate the PD is to be connected in 4-pair mode, with two positive pairs and two negative pairs.

Fortunately, we have a Table that lists all of those options!

SuggestedRemedy

"Single-signature PDs shall not exceed I Unbalance_PD-2P for longer than T CUT min and 5 % duty cycle, and shall not exceed I Unbalance_peak-2P , as defined in Table 145-31 on any pair when the PD is connected per any valid 4-pair configuration, as defined in Table 145-20, to any voltage in the range of V Port_PSE-2P min + 0.31 V to V Port_PSE-2P max through two common mode resistances, R source_min and R source_max, as defined in Equation (145-28) and shown in Figure 145-30."

Same change for dual.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
"Yair: The commenter says that the requirement is valid when working over 4-pairs but this is what the current text says by specifying for the current of ""pairs of the same polarity"" which is only 4-pairs since in two pairs you don't have pairs of the same polarity..so the commenter argument that the text current text doesn't make sense…doesn't make sense.The main point of the current spec is about Iunbalance between pairs of the same polarity AND NOT NOTHING ELSE. Furthermore, replacing ""pairs of the same polarity"" by the link to Table 145-31 doesn't tell the reader that we are addressing only the 4-pairs case which the current text does.In addition, the text is page 212 lines 40-43 also say that we are addressing 4-pairs operation but it is a description of the use case but not include in the requirements of the called out text to make it explicit. Suggest rejecting this comment since it doesn't add clarity or accuracy. The remedy the proposed remedy doesn't answer the commenter worries and the commenter worries already addressed in the current text."

Cl **145** *SC* **145.3.9** *P* **215** *L* **31** # r02-64

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *MPS*

"A single-signature PD shall use the I Port_MPS value associated with assigned Class 5 to 8 when pse_assigned_class is 5, 6, 7, or 8, or when PDRequestedPowerValue is greater than 255."

We need to weave in an exception for when PDRequestedPowerValue == 0xACAC, because in that case, assigned Class is leading.

SuggestedRemedy

Change as follows:
"A single-signature PD shall use the I Port_MPS value associated with assigned Class 5 to 8 when pse_assigned_class is 5, 6, 7, or 8, or when PDRequestedPowerValue is greater than 255, but not equal to 0xACAC."

This has become very ugly --- any better way to specify this ?

Proposed Response *Response Status* **W**

TFTD

I hate this….

TFTD CJ
Suggest leaving the sentence as is and adding after: "The only exception is when PDRequestedPowerValue equals 0xACAC which signifies an Autoclass PD."

Yair : looks that this is a good example of more is less. If I understand correctly, you want the requirement to be valid for PDRequestedValue>255 ONLY. In this case you don't need to add but not equal to 0xACAC since the text already says that it is valid only for PDRequestedValue>255 ONLY. Not clear what is the added value of adding the text you want. Let's take this to the extreme: Do we need when ever something is valid for X>Y to add text that says "but it is not valid for X=Y" ? looks to me that we don't need it...unless I miss something here.

Cl **145** *SC* **145.3.9** *P* **215** *L* **44** # r02-65

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *MPS*

"A PD shall meet the T MPS_PD requirement with a series resistance of R Ch , which represents the worst case cable resistance between the measurement point and the PD PI."

Once again we have a requirement that only applies at a single point (RChan=RCh). Also, there is no reason to imply the measurement must be made at the far end of the

SuggestedRemedy

Replace by:
"A PD shall meet the T MPS_PD requirement with a series resistance in the range of 0 Ohm to R Ch between the PD PI and the source."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 84

TFTD YD
See my response to #84.

Cl **145** *SC* **145.3.9** *P* **215** *L* **44** # r02-84

Abramson, David — Texas Instruments Inc

Comment Type **TR** *Comment Status* **D** *MPS*

When combining all of the PD MPS requirements into a table, we inadvertantly caused Type 3 and Type 4 PDs to draw more power (than Type 1 and 2) when connected to Type 1 and Type 2 PSEs.

This is because the 75ms for Tmps_pd number already accounted for the effect of the cable impedance and PD capacitance as the PSE limit was 60ms. For Type 3 and 4, we reduced the margin from 15ms to 1ms, but required the PD Tmps_pd to be measured with the cable impedance there (meaning that the PD designer had to account for the effect of the cap and impedance). However, the sentences (which were separate) got combined into a single sentence when all the numbers were moved to a table, adding the cap/impedance requirement on top of the 15ms margin for the 75ms requirement.

Also, we should make sure Tmpdo_pd is met with the cable impedance present.

SuggestedRemedy

Change: "A PD shall meet the TMPS_PD requirement with a series resistance of RCh, which represents the worst case cable resistance between the measurement point and the PD PI."

To: "A PD shall meet the TMPS_PD and TMPDO_PD requirements with any series resistance between 0 Ohms and RCh between the PD PI and the source when long_class_event = TRUE."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD

Note: I know that this makes it sound like these requirements don't exist if lce=false, but they are covered by the shall on line 21 combined with the shall on line 26. I would welcome better text that clarifies this.

TFTD YD
"Yair: The only issue I see is that the timing values need to be met in the range from Rchan=0 to Rch. We don't need to define if the requirement is to be met if long_class_event=TRUE only because it need to be met with TRUE or FALSE case as well.In PSE/PD Type 1 and 2, the 75msec requirement from the PD was set regardless of Rch. This is minimum value. The value of 60msec in the PSE was set to be way below 75msec NOT BECAUSE Rch and capacitance effect since time constant effect is negligible at 5uF and 180uF (75msec compared to 0.0625msec and 2.25msec time constants for 5uF and 180uF). For Type 3 and 4 PD this is not the case (7msec vs.. same numbers) at the PD input including Rch effect so PSE sees real 7msec min but has 6msec which is just 1msec margin which is OK for the spec. Based on the above data, I wonder if the new text is better. As it is, you need the PD to show 7msec or 75msec at the PD PI with Rchan from 0 to Rch. As a result, we just need to change to:""A PD shall meet the

TMPS_PD and TMPDO_PD requirements with any series resistance between 0 Ohms and RCh between the PD PI and the source."" OR ACCEPT r02-65 and make r02-84 OBE to r02-65."

Cl **145** *SC* **145.4.1** *P* **217** *L* **39** # r02-70

Peker, Arkadiy
Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Darshan2*

The requirement in "Dual-signature PDs shall have less than or equal to 10 uA of current between any one conductor of Mode A and any one conductor of Mode B when VPD, as defined in 145.1.3, of either Mode is less than VOff_PD min, as defined in Table 145-29. See Table 79-6f." is impossible to meet due to the following reasons:
There are diodes between some of the pins that are low impedance. It should be isolated between pairs of the same polarity that the PSE is required to support only i.e. the requirement should be the minimum requirement to keep interoperability.

SuggestedRemedy

Change from: "Dual-signature PDs shall have less than or equal to 10 uA of current between any one conductor of Mode A and any one conductor of Mode B when VPD, as defined in 145.1.3, of either Mode is less than VOff_PD min, as defined in Table 145-29. See Table 79-6f."
To: "Dual-signature PDs shall have less than or equal to 10 uA of current between any negative pairs when VPD, as defined in 145.1.3, of either Mode is less than VOff_PD min, as defined in Table 145-29. See Table 79-6f."

Proposed Response *Response Status* **W**

TFTD

1) I can't come up with a Mode A to Mode B (or vice versa) connection that is low impedance. There is always at least one reversed bias diode in the path.

2) In the suggested remedy, you add "on the negative pairs", but there is no requirement on the PSE to measure current on the negative pairs. The only requirement that I am aware of is for PSEs to control the inrush current on the negative pairs.

TFTD YD
"Yair:
(1) We can't ask for 10uA leakage current between any one conductor of Mode A and any one conductor of Mode B since there are pins that connected to Transformers (not diodes as mentioned by the comment) that forms very low resistance. The original intent of dual-signature PD vendors was to have isolation between pairs of the same polarity at the polarity where the PSE guarantee switching and measuring the current/voltage when doing connection check and/or detection. This is the minimum spec required to guarantee interoperability.
(2) Requiring isolation on the positive pairs at the PD side has no value and technically is not needed by the PD nor by the PSE due to the following reasons:
a) Only the negative pairs at the PD are guaranteed to be supported by the PSE negative pairs. There is no guarantee or mandatory PSE requirement to control the current (switch it ON/OFF) and measure it (implicit requirement) on the positive pairs. There is only mandatory requirement to switch the negative pairs.The only way to support switches on the PSE positive/negative pairs is to measure the current on the pairs where the switches are located so it will meet the controllability criteria i.e. current can be controlled and monitored on the pairs where the switching elements are located since the current i1 in the

positive pairs is not equal to its return current i3 in the negative pairs (see drawings in the Annexes in darshan_02_0118.pdf) and the same applies for i2 and i4. As a result, even if there is no explicit requirement to measure the current in the negative pairs of the PSE, it is implicitly defined. If we want, we can require explicitly to measure the current at least at the negative pairs too but I believe it is not necessary due to the above discussion.
(b) Even if we require isolation on the positive pairs at the PD it is not guaranteed that it will be supported by the PSE since at the PSE side we will have short between the positive pairs if PSE switches only at the negative pairs. There is no technical reason or need to switch on the positive pairs at the PSE if it is mandatory to switch on the negative pairs.
(c) there is no point to mandate in the PD isolation on the positive pairs knowing that nobody will follow this requirement due to no technical need and no violation of interoperability criteria.
(d) In a dual-signature PD with a single load, you must short the positive pairs (if the negative pairs in the PD are not the common point) at the PD side to form close circuit. In dual-signature PD dual load it is much simpler case. We have inherent isolation on both negative and positive pairs HOWEVER, the PSE shorts its positive pairs effectively make the PD positive pairs not isolated so bottom line, in both cases of dual-signature PD the requirement for isolation on positive pairs is technically not required and doesn't bring any value in addition to the fact that PSE is not required to support it.
(e) Due to the above arguments, the minimum spec requirements to guarantee interoperability is to require isolation at least between the negative pairs at the PD.
(f) There is other problem not connected to David A questions that the 10uA isolation requirement value is correct up to 10.1V but need to be higher than 10uA between 10.1V and 30V since the source of the leakage is voltage depended and leakage current is increased as voltage increased (See darshan_02_0118.pdf."

Cl **145** *SC* **145.4.1** *P* **217** *L* **39** # r02-119

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan2*

There are few errors in the text "Dual-signature PDs shall have less than or equal to 10 uA of current between any one conductor of Mode A and any one conductor of Mode B when VPD, as defined in 145.1.3, of either Mode is less than VOff_PD min, as defined in Table 145-29. See Table 79-6f.".
a) we can't ask for 10uA leakage current between any one conductor of Mode A and any one conductor of Mode B since there are pins that connected to diodes in forward bias conduction. The intent was to have isolation between pairs of the same polarity at polarity where the PSE guaranteed switching and measures the current/voltage when doing connection check and/or detection.
b) The requirement should apply to the negative pairs while for the positive pairs it should be optional and the reason is that the PSE has a mandatory requirement to switch on the negative pairs hence PD is guaranteed to be supported in terms of isolation on the negative pairs but there is not guaranteed for the positive pairs to be supported.
c) in addition to (b) there is no technical need to require both sides isolated in the PD since it is not cost effective and it doesn't give any technical value to do it. It actually limits the use of TVS connected to a common point.
d) The 10uA isolation requirement value is correct up to 10.1V but need to be higher than 10uA between 10.1V and 30V since the source of the leakage is voltage depended and leakage current is increased as voltage increased.

SuggestedRemedy

Adopt darshan_02_0118.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

TFTD YD
See updated comment details in darshan_02_0118.pdf and adopt its proposed remedy.

Cl **145** *SC* **145.4.9.4.1** *P* **229** *L* **50** # r02-66

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *AES*

"Calculations that result in PSANEXT loss values greater than 67 dB shall revert to a requirement of 67 dB minimum."

We can shave off a separate shall by incorporating this into the equation.

SuggestedRemedy

Replace Equation (145-36) as follows:

PSANEXT loss - min(67, 70.5 - 20 * log10(f/100))

and delete quoted text.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD CJ
AIP: make the change to the equation and only delete the shall, leaving the explanatory text. Need to change 'revert' to 'reverts'.

Response DNA: No revert is correct (the noun is plural).

TFTD YD
Yair: There is error in the equation the "-" need to be "="

Cl **145** *SC* **145.4.9.4.2** *P* **230** *L* **9** # r02-67

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *AES*

"Calculations that result in PSAFEXT loss values greater than 67 dB shall revert to a requirement of 67 dB minimum."

We can shave off a separate shall by incorporating this into the equation.

SuggestedRemedy

Replace Equation (145-37) as follows:

PSAFEXT loss - min(67, 67 - 20 * log10(f/100))

and delete quoted text.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD CJ
AIP: make the change to the equation and only delete the shall, leaving the explanatory text. Need to change 'revert' to 'reverts'.

Response DNA: No revert is correct (the noun is plural).

TFTD YD
Yair: There is error in the equation the "-" need to be "="

Cl **145C** *SC* **145C** *P* **295** *L* **11** # r02-120

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Annex*

It will be advantageous to mention that the current calculations done at 100% balanced system while in actual system the unbalance as specified by 145.2.8.1 and 145.3.8.9, reduces the current resulting with lower cable power dissipation .

SuggestedRemedy

Add the following text after line 11 page 295:
"The following models and calculations are derived for 100% balanced system (zero unbalance) while in all systems the actual resistance unbalance is greater than zero as specified by 145.2.8.1 and 145.3.8.9 which reduces the current and resulting with lower cable power dissipation."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This Annex is meant to simplify the reader's understanding. The difference in power loss due to unbalance is negligible enough that it does not warrant putting this note into the draft.

TFTD YD
Yair: at 9% unbalance with class 8 which happens at 100m the difference in power loss between 0% unbalance and 9% unbalance is about 1.65W (18.7W in perfect balanced system vs.. 17 with 9% unbalance) which is ~ 10% less power. This is not negligible. In addition the proposed added text doesn't add complexity it just adds important fact that the balance system is the worst case power loss and in reality due to unbalance, the power loss is lower. It is like stating that at shorter cable than 100m the power loss is lower…