Cl **1** *SC* **1.4.254** *P* **24** *L* **30** # r03-98

Thompson, Geoffrey — Individual

Comment Type **TR** *Comment Status* **X** *Definitions*

The resolution of Thompson comment put into D3.3 is essentially a REJECT of D3.2 Comment r02-85.
The text in D3.3 cl. 1.4.309 is not a satisfactory resolution of Comment r02-85.
The text in D3.3 cl. 1.4.309 is not technically correct in the full context of IEEE Std 802.3 which is the scope of the proposed definition.

Your definition
"link section: The portion of the link segment from the PSE to the PD"
is dependent on being a subset of the following definition
"1.4.290 link segment: The point-to-point full-duplex medium connection between two and only two Medium Dependent Interfaces (MDIs)."

In a clause 33 Type 1/2 instance with a midspan PSE, the link section is entirely separate from the link segment.
Reference: P802.3cj/D3.0, Figure 33-6--10BASE-T/100BASE-TX Midspan PSE location overview, Alternative B

SuggestedRemedy

Delete the change to the definition of "link section" from the P802.3bt draft and leave the definition of "link section" in P802.3Rev (P802.3cj)/D3 unchanged.

Proposed Response *Response Status* **W**

TFTD

Cl **30** *SC* **30.12.2.1.17b** *P* **47** *L* **18** # r03-81

Law, David — Hewlett Packard Enter

Comment Type **T** *Comment Status* **X** *Pres: Law1*

A PSE that supports DLL classification contains an instance of both the Local System Group (oLldpXdot3LocSystemsGroup) managed object class and the Remote System Group (oLldpXdot3RemSystemsGroup) managed object class. Similarly a PD that supports DLL classification contains an instance of both the Local System Group managed object class and the Remote System Group managed object. The information in the Local System Group managed object class is used to populate the fields in transmitted TLVs, the Remote System Group managed object class is populated from the received TLVs. This the case for both a PD and a PSE. See <http://www.ieee802.org/3/bt/public/jan17/802d3bt_law_01_0117.pdf> for more details.

Based on this every attribute in these two managed object classes needs to have a defined behaviour for both a PSE and a PD. At the moment some do, for example 30.12.2.1.17b aLldpXdot3LocPDRequestedPowerValueB includes the text 'For a PD, it is the power value that the PD has currently requested from the remote system for the Mode B pairset. For a PSE, it is the power value for the Alternative B pairset that the PSE mirrors back to the remote system.'.

But others do not, for example 30.12.2.1.18n aLldpXdot3LocAutoclassCompleted just states 'A read-only attribute that returns a bit string indicating whether the local PSE system has completed the Autoclass measurement.'. Taking this as an example Table 79-9 'IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references' states that the 'Autoclass completed' bit is mapped from the attribute aLldpXdot3LocAutoclassCompleted. Further, subclause 79.3.2.6f.2 'Autoclass completed' states that 'When the Power type is PD this field shall be set to 0.'. Based on this the behaviour of the aLldpXdot3LocAutoclassCompleted attribute should really state that 'For a PD this bit is set to zero.'.

Also there seems to be cases where the description in Clause 30 is not aligned with Clause 79. As an example subclause 30.12.2.1.18e aLldpXdot3LocPowerPairsExt states that '... for a PD the contents of this attribute are undefined.'. Table 79-9 states that the PSE power pair ext is mapped from the aLldpXdot3LocPowerPairsExt attribute yet subclause 79.3.2.6c.3 'PSE power pairs ext' states that 'A TLV generated by a PD shall set the field to 0.'.

SuggestedRemedy

Ensure that (a) Clause 30 Local System Group and Remote System Group managed object class attributes have defined behaviours for both a PD and a PSE instance and (b) Clause 30 Local System Group and Remote System Group managed object class attributes behaviours match the behaviours defined for the TPV fields they are mapped from or to.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **30** *SC* **30.12.2.1.18d** *P* **48** *L* **35** # r03-21

Yseboodt, Lennart — Philips Lighting

Comment Type **E** *Comment Status* **D** *Management*

OOS

Management object "aLldpXdot3LocPDPoweringStatus" name does not match with corresponding LLDP field,
which is called 'PD Powered Status field'.

SuggestedRemedy

Change to "aLldpXdot3LocPDPoweringStatus" to "aLldpXdot3LocPDPoweredStatus" in the draft.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Do they need to match? The current text makes sense as the PSE is powering and the PD is powered…

TFTD

Cl **33** *SC* **33.4.3** *P* **70** *L* **54** # r03-8

Anslow, Peter — Ciena Corporation

Comment Type **T** *Comment Status* **D** *Editorial*

The editing instruction is "Change 33.4.3 as follows:". However, the content of 33.4.3 in the base standard below Equation (33-16) is missing, so it is unclear what should be done with it.

SuggestedRemedy

Bring Equation (33-17) and Figure 33-20 in to the draft to clarify whether they should be removed or not.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
Double check with George to see what we need to do

Cl **79** *SC* **79.3.8.1** *P* **96** *L* **31** # r03-15

Anslow, Peter — Ciena Corporation

Comment Type **E** *Comment Status* **D** *Editorial*

The table being inserted in 79.3.8.1 comes after Table 79-8 in 79.3.7.2 of the base standard, so it should be Table 79-8a.

SuggestedRemedy

Change the table number to be Table 79-8a

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
Change Table 79-7b to 79-8a
Change Table 79-7c to 79-8b

Cl **145** *SC* **145.1.3** *P* **113** *L* **47** # r03-28

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *Cabling*

OOS

"For 2-pair systems that provide Class 4 power or less, two twisted pairs are required to source I Cable --one carrying (+ I Cable) and one carrying (- I Cable), from the perspective of the PI."

Implies that there are 2-pair systems that provide more than Class 4.

The proposed change links nicely to the next sentence in the paragraph which reads:

"All four twisted pairs, connected from PSE PI to PD PI are required in order for the PSE to source greater than Class 4 power at the PSE PI"

SuggestedRemedy

Change to:
"In a 2-pair system two twisted pairs are required to source I Cable --one carrying (+ I Cable) and one carrying (- I Cable), from the perspective of the PI.
Such systems are restricted to Class 4 power."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Note that the 4-pair equivalent sentence doesn't mention 4-pair systems, thus this sentence doesn't need to and it only confusing things…

Change to:
"Two twisted pairs are required to source I Cable --one carrying (+ I Cable) and one carrying (- I Cable), from the perspective of the PI. Such systems are restricted to Class 4 power."

TFTD LY
But now the second sentence "Such systems are..." refers back to nothing.
This paragraph has become unwieldy, trying to explain things that really ought to come later.

Propose to replace lines 47 through 54 by:
I Cable , specified in Table 145-1, is the current on one twisted pair in the balanced twisted-pair cable. When power is delivered over 2 pairs, two twisted pairs are required to source I Cable, one carrying (+ I Cable) and one carrying (â€“ I Cable), from the perspective of the PI.
When power is delivered over 4 pairs, four twisted pairs are required to source 2xICable, two each carrying a nominal current (+ I Cable) and two each carrying a nominal current (- I Cable), from the perspective of the PI.

OPTIONALLY add:
Greater than Class 4 power delivery requires 4 pairs.

TFTD HS
Maintain the original suggested remedy.

The "such systems" term no longer refers to anything in previous sentence as that "system" was deleted…

Cl **145** *SC* **145.1.4** *P* **115** *L* **14** # r03-69

Brillhart, Theodore — Fluke Corporation

Comment Type **TR** *Comment Status* **X** *Cabling*

While the ISO/IEC TS 29125 Technical Specification 'Information technology -- Telecommunications cabling requirements for remote powering of terminal equipment' provides guidance for remote powering on new cabling installations and renovations ISO/IEC JTC1 SC25 WG3 is working on a revision of the ISO/IEC 14763-2 standard 'Information technology -- Implementation and operation of customer premises cabling -- Part 2: Planning and installation' which is currently in the committee draft balloting stage.

This revision to the standard will add the requirements and recommendations for the specification, planning, installation and administration of cabling intended to support currents per conductor of up to 500 mA. It mandates those requirements for all installations of cabling into new buildings and refurbishment of existing infrastructure.

Subclause 145.1.4 Cabling requirements states 'Under worst-case conditions, Type 3 operation requires a 10 degree C reduction in the maximum ambient temperature when all cable pairs are energized at ICable (see Table 145-1), or a 5 degree C reduction in the maximum ambient temperature when half of the cable pairs are energized at ICable.'

This statement is not correct since the 10 degree C reduction covers a 100 cables bundle in air (ventilated) and therefore does not correspond to worse case conditions. Instead a reference to ISO/IEC 14763-2 should be made as this provides guidance on installations in all configurations.

SuggestedRemedy

Change the second paragraph of 145.1.4 to read 'Requirements for the planning of all types of PSEs are provided in ISO/IEC CD 14763-2 supported by the information in ISO/IEC TS 29125 and TIA TSB-184-A, as well as applicable local codes and regulations, e.g., ANSI/NFPA 70 - National Electric Code(R) (NEC(R)) for more information.'

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.1.4** *P* **115** *L* **19** # r03-99

Diminico, Christopher

Comment Type **G** *Comment Status* **X** *Pres: Diminico1*

The cautionary note on the use of cables with conductors smaller than 26 AWG should be replaced with reference to TIA-TSB-184-A Annex E. which is to provide installation guidelines to support the delivery of power over installations with 28 AWG cord cable.

SuggestedRemedy

Replace cautionary note with reference to TIA-TSB-184-A Annex E in development under TR42.7 which is to provide installation guidelines to support the delivery of power over installations with 28 AWG cord cable.

Presentation to be provided.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.4** *P* **125** *L* **5** # r03-30

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt1*

"The PSE shall meet all specifications related to current on the negative pair or pairs unless otherwise noted."

We need to review all references to current, specifically to 'pairset current'.

SuggestedRemedy

Adopt yseboodt_01_0318_current.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.5.6** *P* **139** *L* **32** # r03-78

Law, David Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *PSE SD*

In the definition of the variables returned by the do_class_probe_pri function, for the pd_req_pwr_pri variable it is stated 'See pd_req_pwr_pri in 145.2.5.4.'. The pd_req_pwr_pri isn't defined in subclause 145.2.5.4, instead it's defined in the do_classification_pri function below. A similar issue exists for the pd_req_pwr_sec returned by the do_class_probe_sec function.

SuggestedRemedy

Change 'pd_req_pwr_pri: See pd_req_pwr_pri in 145.2.5.4.' to read 'pd_req_pwr_pri: See do_classification_pri function.'.
Change 'pd_req_pwr_sec: See pd_req_pwr_sec in 145.2.5.4.' to read 'pd_req_pwr_sec: See do_classification_sec function.'.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

pd_req_pwr is defined in 145.2.5.4 on page 132, line 23. All of the commented instances refer back to the original defintion so that there are not multiple definitons of the same variable.

TFTD LY
Clarification: this situation exists because the variable pd_req_pwr is assigned both directly by the state diagram, as well as being returned by a call to the do_class_probe function.

TFTD HS
David Law is correct. David A incorrectly references pd_req_pwr in his reject.

Cl **145** *SC* **145.2.5.6** *P* **140** *L* **37** # r03-34

Yseboodt, Lennart — Philips Lighting

Comment Type **E** *Comment Status* **D** *Editorial*

"pd_class_sig_pri: The PD class signature seen during the most recent class event; see Table 145-11 and 145.2.8."

This is about the class signature and should point to Table 145-13 in stead.

SuggestedRemedy

Change link from Table 145-11 to 145-13 and make the same change for pd_class_sig_sec.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
The remedy for the secondary is not complete

TFTD CJ
can't be an accept. The suggested remedy incomplete. Need to be AIP and have Lennart finish the remedy

TFTD HS
Incomplete remedy.
Also fix in pd_class_sig_sec p 141 line 10.

Response DNA: the suggested remedy says "make the same change for pd_class_sig_sec."

Cl **145** *SC* **145.2.5.6** *P* **142** *L* **44** # r03-104

Darshan, Yair

Comment Type **E** *Comment Status* **D** *Editorial*

pse_allocated_pwr line need to be aligned to the other variables and need to be with one line space from the next line.

SuggestedRemedy

1. Move pse_allocated_pwr line to the left to align with do_update_pse_allocated_pwr.
2. keep one line space between pse_allocated_pwr to do_update_pse_allocated_pwr_pri

Proposed Response *Response Status* **W**

PROPOSED REJECT.

pse_allocated_pwr is a variable returned by the function do_update_pse_allocated_pwr and thus needs to be indented as it currently is. The current formatting is correct.

TFTD YD
There are two issues in the comment. The 2nd issue is missing space to the next line that was not addressed by the comment editor/Lennart.

Respose DNA: The spacing is correct. There are blank line between a function description and the variables it returns, but no blank space between the variables and the

Cl **145** *SC* **145.2.5.6** *P* **142** *L* **49** # r03-105

Darshan, Yair

Comment Type **E** *Comment Status* **D** *Editorial*

pse_allocated_pwr_pri line need to be aligned to the other variables and need to be with one line space from the next line.

SuggestedRemedy

1. Move pse_allocated_pwr_pri line to the left to align with do_update_pse_allocated_pwr_pri.
2. keep one line space between pse_allocated_pwr_pri to do_update_pse_allocated_pwr_sec"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

pse_allocated_pwr is a variable returned by the function do_update_pse_allocated_pwr_pri and thus needs to be indented as it currently is. The current formatting is correct.

TFTD YD
Same as 104

Response DNA: See 104

Cl **145** *SC* **145.2.5.7** *P* **149** *L* **17** # r03-100

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan1*

There is PSE state machine issue regarding the location "det_start_pri <== TRUE" from INIT_PRI to START_CXN_CHK_DETECT that need to be resolved. See darshan_01_0318.pdf for comment and remedy.

SuggestedRemedy

Adopt darshan_01_0318.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.7** *P* **161** *L* **7** # r03-36

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **D** *Connection Check*

OOS

Connection check PSE PI voltage requirements differ from those of detection.

Detection:
1. Voc applies for an open circuit
2. Isc applies for a short circuit
3. Vvalid applies when a valid detection signature is connected
4. Anything outside of these conditions is not specified, so falls back to Voc and Isc

Connection check repeats requirements 1 and 2, but omits 3.
Why would we permit the voltage to rise above Vvalid max when a valid detection signature is present ?
The whole point of detection was to prevent just that from happening.

Note that since CC and detection cannot be told apart at the PI, these requirement really must be the same in order to be testable.

SuggestedRemedy

Change sentence p161, line 17 from:
"During connection check the PSE shall meet the specifications for open circuit voltage, V oc , and short circuit current, I sc , in Table 145-7."
to read:
"During connection check the PSE shall meet the specifications for open circuit voltage, Voc, short circuit current, Isc, and valid test voltage Vvalid, defined in Table 145-7."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change
from:
During connection check the PSE shall meet the specifications for open circuit voltage, Voc, and short circuit current, Isc, in Table 145-7. In addition, only tests that result in a voltage at the PSE PI that is below Vvalid max as defined in Table 145-7 shall be used to determine whether a single-signature PD or dual-signature PD is attached to the two pairsets.

To:
During connection check the PSE shall meet the specifications for open circuit voltage, Voc, and short circuit current, Isc, in Table 145-7. The connection check voltage at the PSE PI shall be within the Vvalid voltage range, as defined in Table 145-7, with a valid PD connection check signature connected, as defined in (PD signature configuration).

TFTD YD

The comment is not clear. OBE it to #93 which is the same subject and is good.

Response DNA: This is the exact same resolution as 93. I can't OBE it because the comments need different explanations.

TFTD LY
Let's not accept two comments that change the same text. OBE r03-93 to r03-36 (or the other way around).

Cl **145** *SC* **145.2.7** *P* **161** *L* **17** # r03-93

Stover, David — Analog Devices Inc.

Comment Type **TR** *Comment Status* **D** *Connection Check*

PSE connection check criteria specifies vvalid as voltage range for determining single/dual signature but does not prohibit PSE from using voltage greater than vvalid when a valid PD is connected. This behavior is inconsistent with detection requirements, so let's borrow the same text from PSE detection and apply to PSE connection check.

Also by prohibiting PSE from exceeding vvalid when connected to a valid PD, we do not need to specify PSE behavior above vvalid (voltage below Voff for at least TReset).

SuggestedRemedy

Change
from:
During connection check the PSE shall meet the specifications for open circuit voltage, Voc, and short circuit current, Isc, in Table 145-7. In addition, only tests that result in a voltage at the PSE PI that is below Vvalid max as defined in Table 145-7 shall be used to determine whether a single-signature PD or dual-signature PD is attached to the two pairsets.

to:
During connection check the PSE shall meet the specifications for open circuit voltage, Voc, and short circuit current, Isc, in Table 145-7. The connection check voltage at the PSE PI shall be within the Vvalid voltage range, as defined in Table 145-7, with a valid PD connection check signature connected, as defined in (PD signature configuration).

Delete "If the voltage on either pairset rises above Vvalid max, as defined in Table 145-7, during connection check,
the PSE shall reset the PD by bringing the voltage at the PI below Voff max, as defined in Table 145-16, for
at least TReset, as defined in Table 145-14, before performing classification."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We can't delete the reset text as we still have the possibility of a PD getting plugged in during connection check. Not sure if CC will work as the PD may be in mark as the PI will start at Voc and then come down, but we still need to account for it.

Change
from:
During connection check the PSE shall meet the specifications for open circuit voltage, Voc, and short circuit current, Isc, in Table 145-7. In addition, only tests that result in a voltage at the PSE PI that is below Vvalid max as defined in Table 145-7 shall be used to determine whether a single-signature PD or dual-signature PD is attached to the two pairsets.

To:

During connection check the PSE shall meet the specifications for open circuit voltage, Voc, and short circuit current, Isc, in Table 145-7. The connection check voltage at the PSE PI shall be within the Vvalid voltage range, as defined in Table 145-7, with a valid PD connection check signature connected, as defined in (PD signature configuration).

TFTD LY
Let's not accept two comments that change the same text. OBE r03-93 to r03-36 (or the other way around).

Cl **145** *SC* **145.2.8** *P* **163** *L* **11** # r03-40

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *PSE Power*

OOS

There is no guidance on what to do in case when a fault occurs that causes the PSE to flip to two-pair (*_SEMI_PWRON state).
Would suggest to revert back to PClass in this case.

This provides guidance both for a case where power is managed through DLL or through Autoclass.
This is only required for Class 5-8.

SuggestedRemedy

Insert new sentence on line 12:
"When the PSE assigned Class 5 through 8 prior to a fault and then transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it shall revert the allocation of power to PClass per the assigned Class."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is a fault mode and the worst that happens is that the PD gets shut down. There is no justification for inserting a new "shall" at this point in the process. Furthermore, any Class 5-8 PD that gets powered from SEMI_PWRON is almost guarenteed to get shut down immediately.

TFTD LY
It was passionately argued that allowing SEMI_PWR_ON modes was a great feature for PDs that could make use of it. I imagine that would entail detecting a flip to 2-pair or 3-pair mode and changing the power consumption to a lower level, all within 6ms.

Anyway, for such PDs, it seems useful that it is defined what power is guaranteed in this (unlikely) scenario. We have done that by re-assigning the PD to the min(class 4, assigned class)
in the state diagram. The proposed new shall simply removes ambiguity as what to do with any open
DLL or Autoclass power assignment.

Cl **145** *SC* **145.2.8** *P* **163** *L* **14** # r03-96

Stover, David — Analog Devices Inc.

Comment Type **T** *Comment Status* **D** *Autoclass*

Pac_extra seems to address the case where PSE asynchronously transitions from 4-pair to 2-pair power, ensuring PD still gets full power allocation. However, we say "A PSE that measured PAutoclass while providing power over 4 pairs, shall increase ... during any time it provides power over 2 pairs thereafter." How does this work in the case where a new LLDP-based PD Autoclass measurement is performed AFTER the transition to 2-pair power? Such measurements would already account for RCh/2.

SuggestedRemedy

TFTD clarifying in this conformance statement that Pac_extra needn't be added if Autoclass measurement is performed after transition to 2 pair power.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

It says in that very sentence "A PSE that measured Pautoclass while providnig power over 4 pairs….". Thus, this does not apply if the autoclass measurement was done over 2 pairs.

TFTD DS
Consider the case where a PSE powers a PD and first measures Autoclass power over 4-pair connection. Later, PSE transitions to 2-pair and is forced to use Pac_extra (this is what you want). However, now at any time when the PSE measures Autoclass power again (over 2-pair connection, now) it must apply Pac_extra on top of Pautoclass , rather than Pac_margin. This results in a different behavior from a PSE initially measuring Autoclass over 2 pair. I do not believe this is what you want.

Change “A PSE that measured PAutoclass while providing power over 4 pairs” to “A PSE currently applying PAutoclass measured over 4 pairs”

Response DNA: So, if a PSE measures Autoclass power through DLL, it is not called Pautoclass?

Cl **145** *SC* **145.2.9** *P* **168** *L* **50** # r03-41

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *4PID*

OOS (it has a change bar, but that is because it was moved)

The 4PID requirements subitem b) does not take 3-pair into account.
"The PSE detects a valid detection signature on the unpowered pairset when power is provided over a single pairset"

This would require a true 2-pair mode to exist in order to use this method.
We'll change this to say '2-pair mode' and use yseboodt_01_0318_current.pdf to make clear that includes 3-pair mode for PSEs.

SuggestedRemedy

Change to:
"The PSE detects a valid detection signature on the unpowered pairset when power is provided in 2-pair mode."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
"I don't understand why the 4PID requirement in subitem b care if it is 3 pair (which is 2-pair operation)?I believe that it is not a problem for 4PID since all the measurements (current) are done at the negative pairs so if we have 3 pairs it doesn't matter since it is actually 2-pair operation.Just change the text from """The PSE detects a valid detection signature on the unpowered pairset whenpower is provided over a single pairset""To: ""The PSE detects a valid detection signature on the unpowered **negative pair** whenpower is provided over a single pairset""It addition, this comment is probably addressed in yseboodt_01_0318_current.pdf per comment 30 and may create a conflict with this comment."

Cl **145** *SC* **145.2.8.2** *P* **169** *L* **1** # r03-86

Stewart, Heath — Analog Devices Inc.

Comment Type **E** *Comment Status* **D** *Editorial*

Table has moved out of the section to which it relates.

SuggestedRemedy

Move 145.2.8.3 so it is below Table 145-15.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

There is no 145.2.8.3.

Move 145.2.9 so it is below Table 145-15.

TFTD LY
Frame automatically places Tables and other objects 'optimally', aimed at creating the best output.
Putting in overrides is a bit pointless, as changes to text will make those overrides suboptimal.
Propose to leave this to staff at publication time to change if needed.
Even if it stays as-is, it is preferred to creating a lot of whitespace to force that table in the previous section.

Cl **145** *SC* **145.2.10** *P* **170** *L* **10** # r03-117

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan1*

This comment is marked UNB_REQ.
1. In our spec, we concluded that Icon-2P_unb need to be split to two parameters:
a) Iunbalance-2P which is the max pair current due to unbalance when connected to the test verification model.
b) Icon-2P_unb which is the minimum pair current that the PSE will be able to support under unbalance condition.
c) It is obvious that Icon-2P_unb need to be higher than Iunbalance-2P.
d) In D3.2 we set the numbers of Iunbalance-2P and Icon-2P_unb per the following principles:
We took the simulation results (without the test verification +/-1% accuracy effect) and add to it 5mA and set it as Icon-2P_unb (the actual contribution of the +/-1% is 7mA to 11mA pending the class and not 5%).
And then we set Iunbalance-2P as Icon-2P_unb - 10mA.
3. When I test by calculations if we meet the Iunbalance-2P spec by connecting the PSE to the test verification model, I saw that we fail in Class 5,6 and 7, Class 8 passes but with very small margin. The reason is that in D3.2 we did the procedure to define Iunbalance-2P wrongly.
The reason for the failure is:
Eq-1: Icon-2P_unb=sim_results + 5mA
Eq-2: Iunbalance-2P = Icon-2P_unb -10mA = sim_results + 5mA -10mA =sim_results - 5mA so it clear why we will fail the test when we connect the PSE to the test verification model that was based on the worst case of the sim/calculation results. The sim/calculation results are the minimum value for Iunbalance-2P! (and to add to it the test verification model accuracy effect on Iunbalance-2P and to add the margin to handle Rpse_min, Rpd_min range which is couple of few mA as shown in my previous work on the subject).

SuggestedRemedy

Make the following changes for Icon-2P_unb:
Change Icon-2P_unb for Class 5,6,7,8 from:
0.555, 0.687, 0.789, 0.943
To: 0.570, 0.703, 0.818, 0.950

[As explained, the new values of Icon-2P_unb, when we decrease 10mA from it to determine Iunbalance-2P, will give us the worst case of Iunbalance-2P under +/1% accuracy and Rpse_min, Rpd_min range]
See darshan_01_0318.pdf for details.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.10** *P* **171** *L* **12** # r03-118

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan1*

If comment UNB_REQ will be accepted, ILIM-2P for class 5, 6 and 7 need to slightly modified to sync with Ipeak_2P_unb that has to be higher due to higher Iunbalance-2P.

SuggestedRemedy

Change ILIM-2P for class 5, 6 and 7 from:
0.578, 0716, 0.823
To:
0.59, 0.729, 0.842

Proposed Response *Response Status* **W**

TFTD

WFP

TFTD LY
My name is Lennart and I have OCD.
Can we make it 0.59, 0.73 and 0.85

Cl **145** *SC* **145.2.10.1** *P* **173** *L* **14** # r03-115

Darshan, Yair

Comment Type **T** *Comment Status* **X** *PSE Power*

It is not clear in which cases Trise spec applies. Originally this was specified for EMI reasons but it is not a periodic signal and its effect on EMI is negligible. It is more useful for limiting the transients for the PD logic circuitry which is a good thing. Normally we have the transient at the first time when the PSE applies power and at around 30V the PD isolating switch is turned on which may result with fast drop of the voltage and then nice voltage ramping at Trise much greater than 15us due to larger capacitance at this point of time. So Trise could be measured and apply for the following cases:
a. from the application of Vport_pse i.e. the first rise of the PSE voltage OR
b. from Von_pd to Vport_pse-2P, OR
c. Any transient during the power up phase from t0 to t0+1msec.
d. Any transient during the powerup phase.
As we can see from the above possibilities, it is not clear where is the relevant transient location and its exact definition in which Trise applies.

SuggestedRemedy

Change from: " "TRise, as defined in Table 145-16, is referenced from 10% to 90% of the voltage difference between the positive and the negative conductors of a pairset in a power on state from the beginning of a power up state.""
To: "TRise, as defined in Table 145-16, is referenced from 10% to 90% of the voltage difference between the positive and the negative conductors of a pairset in a power up state from the application of PSE voltage to the beginning of a power up state."

Proposed Response *Response Status* **W**

TFTD

Yair, I don't understand your proposed text.

TFTD YD
I'll try to explain the issue with a drawing at the meeting. May be it will help to word the proposed remedy better

TFTD LY
The goal of Trise seems to be to set a maximum voltage dv/dt while turning on.
Why not define Vrise, similar to Islewrate in the PD, to accomplish this.
That takes care of the entire issue of defining the start and end moments.
The fastest permissibe per the current spec would be 0 to 57V in 15us.

Change Trise to Vrise, "Turn on voltage slewrate", V/us, maximum 4V/us.

Change text in 145.2.10.1 to read:
Vrise, as defined in Table 145-16, is the maximum voltage slewrate in POWER_UP, measured between
the positive and negative conductors of a pairset.

Cl **142** *SC* **142.2.10.5** *P* **174** *L* **6** # r03-82

Abramson, David Texas Instruments Inc

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt1*

The definitions for current need to be updated.

SuggestedRemedy

Edit equation 145-7 as follows:

1. Replace: "is the output current sourced on the Primary Alternative"
with "is the current on the negative pair of the Primary Alternative"

2. Make same change for Secondary Alternative

Proposed Response *Response Status* **W**

TFTD

WFP

TFTD YD
This comment is redundant since it is addressed yseboodt_01_0318_current in comment.pdf in comment 30 and may create a conflict with 82.

Response DNA: Yes, I will OBE it to whatever comment adopts Yseboodt1.

Cl **145** *SC* **145.2.10.5.1** *P* **176** *L* **15** # r03-102

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Unbalance*

Equation 145-13 (Rpse_min/max) is good also for Class 8 extended power since PD is the main factor that affect the fact that at extended power Iunbalance is violated if tighter Rpd_max/Rpd_min ratio will not be used. This need to be clarified in the text. Verified in simulation. There are other comments that adresses the effect of extended power on Equation 145-26 (which affect meeting Iunbalance) and its test verification model for the PD.

SuggestedRemedy

Add the following text:
"Equation 145-13 is valid for PClass_PD including the conditions specified in 145.3.8.2.1.

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.2.10.5.1** *P* **177** *L* **13** # r03-103

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Unbalance*

Rload2_max and Rload2_min in the test verification model (Figure 145-21 and Table 145-18) are correct only for the requested PClass_PD in Table 145-26 (e.g. 71.3W for Class 8) and not for the extended power case as specified in in 145.3.8.2.1. In order to meet Iunbalance at Pclass_PD higher than 71.3W, tighter ratio of Rload2_max/ Rload2_min are required (which is equivalent to Rpd_max/Rpd_min).

SuggestedRemedy

Add the following text after line 13 in page 177:
"Rload2_max and Rload2_min in the test verification model (Figure 145-21 and Table 145-18) are correct only for the requested PClass_PD in Table 145-26 and not for PClass_PD as specified in 145.3.8.2.1. In order to meet Iunbalance per the conditions of 145.3.8.2.1, tighter ratio of Rload2_max/ Rload2_min are required (which is equivalent to Rpd_max/Rpd_min in Equation 145-26. "

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.2.10.8** *P* **181** *L* **27** # r03-43

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **D** *PSE Power*

"The PSE shall limit a pairset current to I LIM-2P for a duration of up to T LIM ."

This is backwards, the PSE is required to limit the current to ILIM-2P for at least a duration of TLIM (which is a minimum).

SuggestedRemedy

Replace by:
"The PSE shall limit the pairset current to I LIM-2P for a duration of at least T LIM ."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
In Clause 33, a PSE limits the current for at least Tlim min, but may not maintain power if it is still in that condition at Tcutmax.
This is enforced by the upperbound and lowerbould template being at the same current level (time disparate).
Our template is such that a PSE may remain in a current limited mode indefinitely. This wasn't done intentionally and probably should not be allowed.

Change text to:
"The PSE shall limit the pairset current to ILIM-2P for a duration of at least T LIM and no longer than TCUTmax.

Cl **145** *SC* **145.2.10.8** *P* **181** *L* **51** # r03-87

Stewart, Heath Analog Devices Inc.

Comment Type **ER** *Comment Status* **X**

Different Tlim values exist for Type 3 and Type 4 PSEs. These PSEs may be otherwise indistinguishable at the PI.
We are really talking about the ability of the PSE to transition from the zero to tlim "shall provide" to the tlim to tcut "shall provide". The goal is to ensure that a PSE w/ only 50V gives the full 10ms.
It is reasonable to allow a Type 4 PSE to make use of the 6ms Tlim, regardless of PD assigned class, by monitoring Tlim, VPort_PSE-2P and VTran-2P for compliance as a group.

SuggestedRemedy

Add
Note - Type 3 and Type 4 PSEs may not be differentiated at the PI. A Type 4 PSE, regardless of assigned Class, may continue to use the Type 4 Tlim, min value as long as VPort_PSE-2P and VTran-2P continue to meet the Type 4 PSE requirements.

Proposed Response *Response Status* **W**

TFTD

Heath, I am not sure we need this text. If the PSE continues to meet the voltage requirements for Type 4, and the PI is not distinguishable from Type 4 in any other way (thus it is type 4), then why do we need this clarification?

Cl **145** *SC* **145.3.3.3.5** *P* **193** *L* **29** # r03-94

Stover, David — Analog Devices Inc.

Comment Type **TR** *Comment Status* **X** *NoPower*

PD is a voltage-controlled state machine with the exception of INRUSH state, which relies solely on tinrushpdmax_timer. I understand the accommodation for reasonable inrush load steps and consequent voltage transients, but VPD < Vmark_th should enter NOPOWER in all cases.

SuggestedRemedy

Add a transition arc from INRUSH to NOPOWER with the condition "VPD < Vmark_th". Add "nopower <= TRUE" to NOPOWER state.

Proposed Response *Response Status* **W**

TFTD

TFTD YD
"The problem with Heath proposal is that if during INRUSH the voltage is dropping to below Vmark and we go to nopower that we will have the same potential overload condition when in NOPOWER the PD assigns pse_power_level = 8.It is true that during Inrush, Vpd may drop to very low voltage due to a sudden short load condition when the Isolating switch is ON and PSE see short load due to the PD input cap and this is OK but in this case the PD Isolating switch is ON, current is flowing so the PD is POWERED and is not in NOPOWER (the isolating switch has ""memory'... which is very common behavior."

TFTD LY
This has the effect of allowing any PD to bypass the POWER_DELAY state if the voltage dips.

Cl **145** *SC* **145.3.3.4.2** *P* **194** *L* **47** # r03-19

Jones, Chad — Cisco Systems, Inc.

Comment Type **ER** *Comment Status* **D** *Editorial*

"A variable indicating that on Mode X, the PD is enabled and should request power from the PSE by applying a PD detection signature to the PI". sentence construct is awkward and doesn't match the form used by the rest of the variables WRT 'on Mode X' where it occurs after 'the PD'.

SuggestedRemedy

change: "A variable indicating that on Mode X, the PD is enabled and should request power from the PSE by applying a PD detection signature to the PI..."

to: "A variable indicating that the PD is enabled on Mode X and should request power from the PSE by applying a PD detection signature to the PI..."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
Additional changes:
- detection 'on that Mode'
- remove redundant 'set in an implementation dependent manner'.

Change description of mdi_power_required_mode(X)
A variable indicating that the PD is enabled on Mode X and should request power from the PSE
by applying a PD detection signature to that Mode, and when the PSE sources power to apply the MPS
to keep the PSE sourcing power. This variable may be set by the PD at any time.

Also remove sentence "A variable that is set in an implementation-dependent manner." from
page 187 line 40.

Cl **145** *SC* **145.3.3.4.3** *P* **197** *L* **18** # r03-110

Darshan, Yair

Comment Type **T** *Comment Status* **D** *PD SD*

The tpowerdly_timer_mode(X) text is not similar to the tpowerdly_timer.
In the single-signature PD we have: "tpowerdly_timer A timer used to prevent the PD from drawing more than IInrush_PD and IInrush_PD-2P during the PSE's inrush period; See Tdelay in Table 145-29."
The part " during the PSE's inrush period" doesn't look accurate and sync with what the PD state machine is actually doing. This timer is used to prevent the PD from drawing more than IInrush_PD and IInrush_PD-2P from TInrush_PD to Tdelay which is different than how it is specified here. See below in the timer for dual-signature PD which is better description of the timer role.

In the dual-signature PD we have: "tpowerdly_timer_mode(X) A timer used to prevent the PD from drawing more than IInrush_PD and IInrush_PD-2P from TInrush_PD to Tdelay. See Table 145-29."
Which is a correct description of the timer role.

SuggestedRemedy

Change from:
" tpowerdly_timer A timer used to prevent the PD from drawing more than IInrush_PD and IInrush_PD-2P during the PSE's inrush period; See Tdelay in Table 145-29.
To:
"tpowerdly_timer A timer used to prevent the PD from drawing more than IInrush_PD and IInrush_PD-2P from TInrush_PD to Tdelay. See Tdelay in Table 145-29. "

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

On pag 190, line 48
Change from:
" tpowerdly_timer A timer used to prevent the PD from drawing more than Iinrush_PD and Iinrush_PD-2P during the PSE's inrush period; See Tdelay in Table 145-29.
To:
"tpowerdly_timer A timer used to prevent the PD from drawing more than Iinrush_PD and Iinrush_PD-2P from Tinrush_PD to Tdelay. See Tdelay in Table 145-29. "

TFTD LY
Dave - I can't believe you wrote that revised remedy. Because it is so wrong.

"tpowerdly_timer: A timer used to limit the PD's power draw to Class 3 or less from Tinrush_PD until Tdelay. See Tdelay in Table 145-29."

Make similar fix for dual-signature.

Response DNA: Yeah, I copied from somewhere, obvioulsy copied the wrong thing.

TFTD HS

I would argue that the original (D3.3) text is indeed correct. tpower_dly is there to protect PSE inrush. The means of accomplishing this is to measure out to Tdelay. Regardless, the AIP change breaks the case of the subscripted inrush terms.

Cl **145** *SC* **145.3.3.4.5** *P* **199** *L* **22** # r03-107

Darshan, Yair

Comment Type **T** *Comment Status* **D** *NoPower*

The changes implemented for the PD state machine for POWER_OFF and NOPOWER was
not implemented in the dual-sig state machine.

SuggestedRemedy

1. Remove nopower_mode(X) from NOPOWER and move it to POWEROFF.
2. The exit from POWEROFF to NOPOWER, change it from:
VPD_mode(X)<Voff_PD_min
To: VPD_mode(X)<Vmark_th

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

1. Remove nopower_mode(X) from NOPOWER and move it to POWEROFF.
2. The exit from POWEROFF to NOPOWER, change it from:
VPD_mode(X)<Voff_PD_min
To: VPD_mode(X)<Vmark_th
3. Change nopower variable to match single-signature defintion.

TFTD to hold open for any other changes to nopower in the SS SD.

Cl **145** *SC* **145.3.4** *P* **199** *L* **41** # r03-45

Yseboodt, Lennart Philips Lighting

Comment Type **T** *Comment Status* **X** *PD Detection*

OOS

"A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 145-25 or Figure 145-27."

This tries to describe the case where the PD does not want power at all. "at the PI" leaves open if the invalid signature is on both pairsets at once, which it should be.

SuggestedRemedy

"A PD presents a non-valid detection signature on both pairsets at the PI while it is in a state where it does not accept power via the PI per Figure 145-25 or Figure 145-27."

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.3.6.1** *P* **203** *L* **6** # r03-109

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Editorial*

The text "Type 1 PDs that did not implement Physical Layer classification requested Class 0, with a power level equivalent to Class 3. PDs that request Class 0 are assigned Class 3 by Type 3 and Type 4 PSEs."
Missing "to".

SuggestedRemedy

Change to "Type 1 PDs that did not implement Physical
Layer classification requested Class 0, with a power level equivalent to Class 3. PDs that request Class 0 are assigned to Class 3 by Type 3 and Type 4 PSEs."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 37

TFTD YD
This comment addresses a text in page 203.comment #37 is dealing with the same text but in page 162. The remedy should be AIP and copy the remedy for #37.

Response DNA: part of the suggested remedy of 37 is "Also change on page 203, line 5 in 145.3.6.1.", thus this comment is OBE by 37.

Cl **145** *SC* **145.3.6.2** *P* **205** *L* **49** # r03-47

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **D** *NoPower*

"When the PD is in POWEROFF and V PD falls below V Off_PD min, the PD transitions to NOPOWER and may show a valid or invalid detection signature, and may or may not draw mark current, draw any class current, and show MPS."

VOff_PD min has been changed in the statediagram to VMark_th.

SuggestedRemedy

Change to:
"When the PD is in POWEROFF and V PD falls below VMark_th, the PD transitions to NOPOWER and may show a valid or invalid detection signature, and may or may not draw mark current, draw any class current, and show MPS."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
"The remedy is OK but the text is in clause 145.3.8.1 page 210 line 18 and not in 145.3.6.2 page 205 line 49. OBE it to #92 which is the same comment and remedy where the location is correct and to prevent conflicts with two identical comments"

Response DNA: Yair seems to be correct.

Cl **145** *SC* **145.3.8** *P* **207** *L* **18** # r03-111

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Editorial*

Table 145-16 item 4 title: Remove the first occurrence of "per the assigned class"

SuggestedRemedy

See comment.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
Wrong Table quoted.
Make Table 145-29 consistently use ", per the assigned Class" at the END of the description,
in line with how it is done on the PSE side.

Cl **145** *SC* **145.3.8.1** *P* **210** *L* **13** # r03-48

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *PD Power*

"The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by V Port_PSE-2P min to V Port_PSE-2P max (as defined in Table 145-16) with a series resistance less than or equal to R Ch ."

We can't ask Class 5+ PDs to correctly start and work when connected through a 2-pair channel.
Unfortunately the fix to this is bulky.

SuggestedRemedy

"The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by V Port_PSE-2P min to V Port_PSE-2P max (as defined in Table 145-16):
- with a series resistance less than or equal to R Ch for assigned Class 1 through 4 to a single-signature PD,
- with a series resistance less than or equal to R Ch / 2 for assigned Class 5 through 8 to a single-signature PD,
- with a series resistance less than or equal to R Ch connected to a given Mode of a dual-signature PD."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
The current text addresses bot single and dual signature PDs. The proposed new text is good but addresses only single-signature PDs. To complete it for dual-signature as well.

Cl **145** *SC* **145.3.8.3** *P* **211** *L* **29** # r03-49

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *PD Inrush*

"""
A PSE limits the inrush current to I Inrush and I Inrush-2P , defined in Table 145-16, which is sufficient current to charge C Port or C Port-2P to V Port_PSE-2P within T Inrush_PD max when:
-- C Port < 180 mF for single-signature PDs assigned to Class 1 through 6
-- C Port < 360 mF for single-signature PDs assigned to Class 7 or 8
-- C Port-2P < 110 mF for dual-signature PDs assigned to Class 1 through 4
-- C Port-2P < 180 mF for dual-signature PDs assigned to Class 5
"""

The latter part of this statement is extremely misleading and provides a false sense of security to PD designers.

If the PD limits the inrush current, any size of capacitor can be charged (as stated a few paragraphs earlier).

Let's consider PDs that don't perform inrush control. What do they actually do ?

option 1) Once the 100nF cap is charged to VOn_PD, the hotswap opens up and stays open for a while.
The PD PI and PSE PI voltage will collapse back to zero, at which point the PSE is allowed to reduce inrush current to 5mA.
Charging the bulk cap will take far more time than is allowed. Inrush will fail. The PD has violated the "Voff" requirement and is non-compliant.

option 2) Once the 100nF cap is charged to VOn_PD, the hotswaps opens up, but the PD stricktly follows Von_PD / VOff_PD.
The hotswap will now 'chatter' on/off repeatedly dumping the charge of the 100nF cap into the bulk cap. Essentially the PD
is performing a crude form of current limiting. Depending on how fast the PD can control the hotswap inrush will complete on time.
This is a horrible implementation, and the PD fails to comply with the 'startup without oscillation and at the first trial' requirement and is non-compliant.

Furthermore, the quoted statement only holds provided that the PD uses the delivered power to charge the cap, and not spend it on other things (like prematurely starting a DC/DC converter...).

As far as I can see it is not possible to implement a compliant PD without having inrush control.

SuggestedRemedy

This late in the process I would not suggest making substantive technical changes to inrush.
But we should change the quoted statement to avoid giving very misleading guidance to

PD designers.

Reduce quoted sentence to:
"The PSE limits the inrush current to I Inrush and I Inrush-2P, for at least TInrush_PD max, as defined in Table 145-16 and Table Table 145-29."

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.3.8.8** *P* **214** *L* **36** # r03-50

Yseboodt, Lennart Philips Lighting

Comment Type **T** *Comment Status* **X** *Backfeed*

"When any voltage in the range of 0 V to V Port_PD-2P max is applied across the PI at either polarity specified on the conductors of either Mode A or Mode B according to Table 145-20, the voltage measured across the PI for the other Mode with a 100 kOhm load resistor connected across that other Mode shall not exceed V bfd as defined in Table 145-29."

This requirement only applies when a true 2-pair voltage is applied.
In 4-pair systems, the reality is that the positive side pairs are tied together.
When one power channel is off, one would expect the PD to also meet the backfeed spec on that 'off' channel. As written, this is not required.

PDs that fail this requirement, might also be mis-identified by connection check or detection.

SuggestedRemedy

Replace by:
"When any voltage in the range of 0 V to V Port_PD-2P max is applied per any of the valid 2-pair configurations listed in Table 145-20, the voltage measured across the Mode which has a pair not connected to a supply rail, with a 100kOhm load resistor connected across that Mode shall not exceed Vbfd as defined in Table 145-29."

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.3.8.9** *P* **215** *L* **52** # r03-101

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Unbalance*

Icon-2P_unb, Iunbalance and Equation 145-26 (Rpd_min/max) where derived based on Pclass_PD per Table 145-26 which doesn't include PClass_PD under extended power conditions. Equation 145-26 doesn't apply to class 8 under the conditions of extended power.
For class 8=71.3W at the PD, Icon-2P_unb is 0.943A according to the 4-pair model parameters per Rpse_min/max, Rchan_min/max and Rpd_min/max.
In Extended power the PD consumes 89.7W at 2.65m cable lenght, the currents in CLASS 8 will be Icon-2P_unb=1.1A, Ipeak-2P_unb=1.148A for Ppeak=1.05*89.7W and ILIM-2P=1.15A under the same 4-pair model parameters in the spec. As a result, PD will need to improved its balance by selecting tighter ratio of Rpd_max/Rpd_min when extended power is used for class 8.

SuggestedRemedy

Add the following text after line 51:
"Meeting Iunbalance for Class 5 to Class 8 by meeting Equation 145-26 is based on the 4-pair model which is described by Equation 145-27 and Equations 145-26 when the requested Pclass_PD is specified per Table 145-26. When Pclass_PD is specified per 145.3.8.2.1, Equation 145-26 is no longer valid and tighter ratio of Rpd_max to Rpd_min should be used in order to meet Iunbalance.

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.3.9** *P* **217** *L* **46** # r03-97

Stover, David — Analog Devices Inc.

Comment Type **T** *Comment Status* **X** *MPS*

"A PD shall meet the TMPS_PD and TMPDO_PD requirements...when long_class_event = TRUE." Shouldn't a Type 3/4 PD meet these requirements when long_class_event = FALSE as well?

SuggestedRemedy

Strike "when long_class_event = TRUE".

Proposed Response *Response Status* **W**

TFTD

See comment r02-84 from last cycle to see how we ended up here. I would love better text, but I haven't come up with any yet.

See comment 51

TFTD YD
"I believe the reason was that:1. the time constant are more significant to the case for short MPS (long_class_event = TRUE). For long class event it doesn't matter you will not notice the differences so no additional requirements are needed.2. The 75msec already defined under worst case R and C.3. If we add now a tiny fraction to the timing for long MPS timing, marginal PDs may fail due to fractions of msec...So, the requirement to meet the timing is only relevant to short MPS. "

Cl **145** *SC* **145.3.9** *P* **217** *L* **46** # r03-51

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *MPS*

"A PD shall meet the T MPS_PD and T MPDO_PD requirements with any series resistance in the range of RChan between the PD PI and the source when long_class_event = TRUE."

RChan is a fixed number, not a range.
We're aiming for any resistance from 0 to RCh Ohms.

SuggestedRemedy

Change to:
"A PD shall meet the T MPS_PD and T MPDO_PD requirements with any series resistance in the range of 0 Ohm to RCh between the PD PI and the source when long_class_event = TRUE."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD for 97

TFTD HS
RChan accounts for 2P/4P connection and is correct.

Cl **145** *SC* **145.5.3.4.5** *P* **253** *L* **6** # r03-79

Law, David — Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *DLL*

On review of Figure 145-45 'Dual-signature PD power control state diagram in 2-pair mode' it appears that during 2-pair mode the 'original' TLV fields are used, such as 'PD Requested power value' rather than the 'new' mode A and B fields such as 'PD requested power value Mode A' and 'PD requested power value Mode B'. This is based on the variables that are tested and assigned in Figure 145-45, for example the assignments to 'PDRequestedPowerValue' in the IDLE, INITIALIZE and MIRROR_UPDATE states, and not to 'pd_initial_value_mode(P)'. Similarly the variable 'PDRequestedPowerValue' is tested on the exit from RUNNING state, not 'pd_initial_value_mode(P)'.

As a result:

(a) Subclause 145.5.3.4.2 'Variables', which states 'The PD power control state diagram (Figure 145-44 and Figure 145-45) use the following variables', is missing the definition for the following variables used in Figure 145-45.

PDRequestedPowerValue
MirroredPDRequestedPowerValueEcho
MirroredPSEAllocatedPowerValue
PSEAllocatedPowerValueEcho
PDMaxPowerValue
TempVar

(b) Table 145-40 'Attribute to state diagram variable cross reference for dual-signature PDs' is missing the following mappings:

aLldpXdot3LocPDRequestedPowerValue <= PDRequestedPowerValue
aLldpXdot3RemPDRequestedPowerValue => MirroredPDRequestedPowerValueEcho
aLldpXdot3RemPSEAllocatedPowerValue => MirroredPSEAllocatedPowerValue
aLldpXdot3LocPSEAllocatedPowerValue <= PSEAllocatedPowerValueEcho

SuggestedRemedy

Add the following to Subclause 145.5.3.4.2 'Variables':

PDRequestedPowerValue
Integer that indicates the PD requested power value in the PD in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD requests. This variable is mapped from the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).
Values: 0 through pd_dllmax_value, and 0xACAC

MirroredPDRequestedPowerValueEcho
The copy of the 'PD Requested Power Value' field in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).
Values: 0 through 999, and 0xACAC

MirroredPSEAllocatedPowerValue
The copy of the 'PSE Allocated Power Value' field in the Power Via MDI TLV that the PD receives from the remote system in units of 0.1 W. This variable is mapped from the aLldpXdot3RemPSE-AllocatedPowerValue attribute (30.12.3.1.18).
Values: 1 through 999, and 0xACAC

PSEAllocatedPowerValueEcho
This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).
Values: 0 through 999, and 0xACAC

PDMaxPowerValue
Integer that indicates the actual PD power value of the local system in units of 0.1 W. The actual PD power value for a PD is the maximum input average power (see 145.3.8.2) the PD ever draws under the current power allocation.
Values: 1 through 999, and 0xACAC

TempVar
A variable used to store Power Value in units of 0.1 W.
Values: 0 through 999, and 0xACAC

Add the following mappings to Table 145-40 'Attribute to state diagram variable cross reference for dual-signature PDs':

aLldpXdot3LocPDRequestedPowerValue <= PDRequestedPowerValue
aLldpXdot3RemPDRequestedPowerValue => MirroredPDRequestedPowerValueEcho
aLldpXdot3RemPSEAllocatedPowerValue => MirroredPSEAllocatedPowerValue
aLldpXdot3LocPSEAllocatedPowerValue <= PSEAllocatedPowerValueEcho

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
Remedy is good, however remove "0xACAC" from the valid values as this doesn't apply to dual-sig.

Cl **145** *SC* **145.5.5.1** *P* **255** *L* **28** # r03-88

Tremblay, David — Hewlett Packard Enter

Comment Type **TR** *Comment Status* **X** *DLL*

Interoperability issue - state change procedure does not cover how to handle power allocation values between 714-999

SuggestedRemedy

TFTD - Add procedure to cover class 8 exception allowing PSEAllocatedPowerValue to assign 714-999

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.5.5.2** *P* **255** *L* **47** # r03-89

Tremblay, David — Hewlett Packard Enter

Comment Type **TR** *Comment Status* **X** *DLL*

Interoperability issue - state change procedure does not cover how to handle power allocation values between 714-999

SuggestedRemedy

TFTD - Add procedure to cover class 8 exception allowing PDRequestedPowerValue to assign 714-999

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.5.6.2** *P* **257** *L* **11** # r03-90

Tremblay, David — Hewlett Packard Enter

Comment Type **TR** *Comment Status* **X** *DLL*

Interoperability issue - state change procedure does not cover how to handle power allocation values between 714-999

SuggestedRemedy

TFTD - Add procedure to cover class 8 exception allowing PSEAllocatedPowerValue to assign 714-999

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.5.6.3** *P* **257** *L* **31** # r03-91

Tremblay, David — Hewlett Packard Enter

Comment Type **TR** *Comment Status* **X** *DLL*

Interoperability issue - state change procedure does not cover how to handle power allocation values between 714-999

SuggestedRemedy

TFTD - Add procedure to cover class 8 exception allowing PDRequestedPowerValue to assign 714-999

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.6.5** *P* **259** *L* **3** # r03-70

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Environmental*

The text "The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance." is missing the fact that the AC voltage which is the ringing voltage is not continuous and has a cadence spec (duty cycle like but with integer number of AC cycles for the on time and off time which may be in the range of 2 sec on , 4sec off or 1sec on, 4 sec off i.e. a ratio of 0.2 to 0.33) which actually significantly reduces the average power dissipation on the device when applied. In addition, the test time is not defined. It doesn't make sense that the test time is infinite since this components are became very hot and may cause fire hazard.

SuggestedRemedy

Change from: "The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance."
To:
Option 1: Without definition for test time.
"The AC component is up to 175 Vp at 20 Hz to 60 Hz with a cadence spec per the relevant national standard with a 100 ohm source resistance."
Option 2: With definition for test time.
"The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance with a cadence spec per the relevant national standard, for a test time duration greater than 5 minutes.

Proposed Response *Response Status* **W**

TFTD

Arkadiy, did you mean "with a test duration less than 5 minutes."? Otherwise the test duration can still be infinite.

TFTD YD
"I looked at #70 and David ask a valid question. The following I hope will resolve 70 and 114.The Idea is to guarantee some minimum testing time so the PSE will be robust for such use case.On the other hand, we must limit the time to prevent fire hazard.So we may need to specify a range. The minimum value will be e.g. 10 times of the maximum cadence cycle which is 10x6sec=60sec.The maximum value will be 100% margin i.e. 2 minutes. As a result, I suggest the following Remedy:""The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance with a cadence spec per the relevant national standard, for a test time duration of minimum 1mintue and less than 2 minutes."" "

TFTD CJ
I think he means a test duration of at least 5 minutes.

TFTD LY
Given that the object of the shall is to "shall not result in any safety hazard", I would rather avoid adding weazel words to this requirement.

Cl **145** *SC* **145.6.5** *P* **259** *L* **3** # r03-114

Darshan, Yair

Comment Type **T** *Comment Status* **D**

The text "The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance." has not sufficient data in order to test the "shall" that follows this description.
The missing parts are:
- the cadence (depends on the national telephony standard)
-The test time duration (implementation specific, but we need to define some reasonable minimum for interoperability).

SuggestedRemedy

Change from: "The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance."
To:
"The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance with a cadence per the relevant national standard, for a test time duration greater than 5 minutes.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 70

TFTD YD
"I looked at #70 and David ask a valid question. The following I hope will resolve 70 and 114.The Idea is to guarantee some minimum testing time so the PSE will be robust for such use case.On the other hand, we must limit the time to prevent fire hazard.So we may need to specify a range. The minimum value will be e.g. 10 times of the maximum cadence cycle which is 10x6sec=60sec.The maximum value will be 100% margin i.e. 2 minutes. As a result, I suggest the following Remedy:""The AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 ohm source resistance with a cadence spec per the relevant national standard, for a test time duration of minimum 1mintue and less than 2 minutes."" "

Cl **145A** *SC* **145A.5** *P* **290** *L* **46** # r03-116

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Annex*

In the text "PD pair-to-pair voltage difference (e.g. Vf1-Vf3) was limited to 60 mV while generating values
for IUnbalance-2P under worst case conditions.", missing information that (Vf1-Vf3) maximum value can be found by measuring Vf1 and Vf3 at low current e.g. 1mA since at high current the effect of Vf3-Vf1 may go below 60mV.

SuggestedRemedy

Add a note after line 47:
"Note --- In order to measure the maximum value of Vf1-Vf3, an input current in the range of 1mA to 10mA is recommended."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

TFTD

Yair, I don't undstand the value of adding this text and it is OOS.

TFTD YD
"1. I agree that it is out of scope. However we have many of them in every cycle and yet we address it if we agree that it adds value.2. The value is significant. It clarifies that the 60mV (which was the limit in our model for the PD and all numbers at worst case conditions are depend on it) is specified at low current which is guarantee that you measure the correct maximum Vdiff. A user may believe that the 60mV is at high current which is wrong since at low current he will get way higher than 60mV and his design will fail the Iunbalance-2P test at worst case condition. Remember that as the current increase Vdiff is decreased due to internal and external resistance in series to the diode. The note clarifies it."