*Cl* **79** *SC* **79.3.8.2** *P* **100** *L* **36** # r04-3

Ran, Adee — Intel Corporation

*Comment Type* **E** *Comment Status* **X** *Editorial*

"The field is encoded as defined in Equation (79-1)"

This equation defines KPPI as a function of this field. So it can be used to decode the field.

Encoding requires solving the equation (numerically, since there is no analytical solution), but this is not stated.

*SuggestedRemedy*

As a simple remedy, change "encoded" to "decoded".

Consider adding "this field encodes the approximate value of KPPI based on Equation (79-1). The approximation is implementation dependent".

*Proposed Response* *Response Status* **W**

TFTD

TFTD LY
This is OOS.
The calculation is done both ways, and the sentence describes the field, which indeed is encoded. No change is needed.

*Cl* **79** *SC* **79.3.8.2** *P* **101** *L* **1** # r04-2

Ran, Adee — Intel Corporation

*Comment Type* **E** *Comment Status* **X** *Editorial*

The text here says "KPPI is the power price index expressed as a factor (...)"

This is confusing since "power price index" is a different value, defined in the next line. KPPI is computed from that index.

The introductory text in this subclause is:

"The 'PSE power price index' field shall contain an index of the current price of electricity compared to what the PSE considers the nominal electricity price".

My understanding is that KPPI is "the current price of electricity compared to what the PSE considers the nominal electricity price", so it is not an index - it is a relative price.

*SuggestedRemedy*

In the definition of KPPI, change "is the power price index" to "is the relative power price".

*Proposed Response* *Response Status* **W**

TFTD

TFTD LY
This is OOS.
Fail to see to confusion. No need for change.

*Cl* **145** *SC* **145.1.3** *P* **116** *L* **12** # r04-26

Yseboodt, Lennart — Philips Lighting

*Comment Type* **E** *Comment Status* **D** *Cabling*

OOS

"This clause uses "pairset DC loop resistance," which refers to two pairs in series."
"Therefore, RCh is related to, but not equivalent to, the "DC loop resistance" called out in the cable references."

In the first sentence we have to define RCh because it is not yet defined.
And move comma out of quotation mark.

*SuggestedRemedy*

Change first sentence to:
"This clause uses "pairset DC loop resistance" (RCh), which refers to two pairs in series."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD…let's make sure this section is correct, we seem to change it every meeting.

*Cl* **145** *SC* **145.2.5.4** *P* **130** *L* **39** # r04-65

Lukacs, Miklos

*Comment Type* **T** *Comment Status* **D** *PSE SD*

--THIS COMMENT WAS SUBMITTED AFTER THE COMMENT PERIOD ENDED, IT WILL BE CONSIDERED IF NO ONE IN THE COMMENT RESOLUTION GROUP OBJECTS.--
dll_4pid is a state machine variable and it exist with the same name in both the PSE and PD variable definitions. This variable is not used anywhere else in the PSE section.

*SuggestedRemedy*

Delete variable and its description from page 13

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD

*Cl* **145** *SC* **145.2.5.6** *P* **143** *L* **37** # r04-68

Tinsley, Janine

*Comment Type* **T** *Comment Status* **X**

--THIS COMMENT WAS SUBMITTED AFTER THE COMMENT PERIOD ENDED, IT WILL BE CONSIDERED IF NO ONE IN THE COMMENT RESOLUTION GROUP OBJECTS.--
The definition of "invalid" is ambiguous in regard to the open circuit condition. Is this an open circuit on both pairsets or either pairset? "Invalid" was spawned from "open_circ" in the remedy to comment 108 against D1.7. In the process, the qualifier "on both pairsets" was removed from the definition of open circuit.

*SuggestedRemedy*

Change: "Neither a single-signature nor a dual-signature configuration has been found. This includes an open circuit condition." To: "Neither a single-signature nor a dual-signature configuration has been found. This includes an open circuit condition on either pairset."

*Proposed Response* *Response Status* **W**

TFTD

*Cl* **145** *SC* **145.2.5** *P* **158** *L* **17** # r04-66

Lukacs, Miklos

*Comment Type* **T** *Comment Status* **D**

--THIS COMMENT WAS SUBMITTED AFTER THE COMMENT PERIOD ENDED, IT WILL BE CONSIDERED IF NO ONE IN THE COMMENT RESOLUTION GROUP OBJECTS.--
In Figure 145-16 "start tinrush_timer_sec" is missing from POWER_UP_SEC

*SuggestedRemedy*

In Figure 145-16 add "start tinrush_timer_sec" to POWER_UP_SEC

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 28

TFTD

*Cl* **145** *SC* **145.2.6.2** *P* **161** *L* **40** # r04-56

Peker, Arkadiy Microsemi Corporation

*Comment Type* **TR** *Comment Status* **D** *Negative Pair*

A requirements related to current need to be met at the negative pairs as we did in D3.3 for other parameters. Equation 145-1 is using currents to calculate the resistance during detection. I1 and I2 need to be the currents on the negative pairs.

*SuggestedRemedy*

In the where list change from:
"I1 and I2 are the first and second current measurements made of the pairset current, respectively"
To:
"I1 and I2 are the first and second current measurements made of the pairset current, respectively. I1 and I2 are measured on the negative pair."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change to:
"I1 and I2 are the first and second current measurements made on the negative pair of the pairset, respectively."

TFTD DS
In proposed response, “negative” is misspelled. Also, this requirement appears to preclude detection on the high side. Is this intentional?

Response DNA: I have fixed the spelling mistake. Yes, we have agreed that all PSE "measurements" must be done on the negative.

*Cl* **145** *SC* **145.2.8** *P* **165** *L* **19** # r04-22

Jones, Chad — Cisco Systems, Inc.

*Comment Type* **E** *Comment Status* **D** *Editorial*

sentence missing a verb or has extra words that make it need a verb. "When the PSE assigned Class 5 through 8 prior to a fault and then transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it reverts the allocation of power to PClass per the assigned Class with a maximum value of Class 4 and asserts local_system_change to update PSEAllocatedPowerValue."

*SuggestedRemedy*

two options:
one:delete 'and then' - "When the PSE assigned Class 5 through 8 prior to a fault transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it reverts the allocation of power to PClass per the assigned Class with a maximum value of Class 4 and asserts local_system_change to update PSEAllocatedPowerValue."
two: add 'is' - "When the PSE is assigned Class 5 through 8 prior to a fault and then transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it reverts the allocation of power to PClass per the assigned Class with a maximum value of Class 4 and asserts local_system_change to update PSEAllocatedPowerValue."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change to:
"When the PSE assigns Class 5 through 8 prior to a fault and then transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it reverts the allocation of power to Pclass per the assigned Class with a maximum value of Class 4 and asserts local_system_change to update PSEAllocatedPowerValue."

TFTD YD
"Yair: I prefer option 2 but option two also missing ""to"". Change option 2 from: ""When the PSE is assigned Class 5 through 8…""To: ""When the PSE is assigned to Class 5 through 8…"""

Response DNA: PSEs don't get assigned to a class, they assign a class.

TFTD LY
Note: I did not comment on this, and would like to hijack this editorial comment to make a technical change.
I do have an unsat negative comment pertaining to this topic.

When the PSE flips into a SEMI_PWRON state, we've made it such that it changes the assigned Class through the pse_allocated_pwr variable.

The normal procedure is that when a DLL transaction occurs, the
DLL state diagram will trigger the main state diagram to update pse_allocated_pwr. No mechanism for the reverse is in place.

This behavior is NOT covered in the state diagram, hence we do need a shall statement here.

Change to:
"When the PSE assigns Class 5 through 8 prior to a fault and then transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it shall revert the allocation of power to Pclass per the assigned Class with a maximum value of Class 4 and asserts local_system_change to update PSEAllocatedPowerValue."

*Cl* **145** *SC* **145.2.8.1** *P* **169** *L* **4** # r04-36

Yseboodt, Lennart — Philips Lighting

*Comment Type* **T** *Comment Status* **D** *PSE Class*

"The timing specification for PSEs in DO_CLASS_PROBE may be reduced to TCEV for all class events."
Are dual signature states not allowed to reduce to TCEV?

*SuggestedRemedy*

Change to:
"The timing specification for PSEs in a DO_CLASS_PROBE state may be reduced to TCEV for all class events."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We tend not to use an actuall state name when using the construct "a XXX state"

ex: "a power on state"

However, we do use this for "all CLASS states"

maybe we should align this usage…

TFTD

TFTD YD
Yair: I agree with the comment but not sure how the remedy is addressing this.

*Cl* **145** *SC* **145.2.10** *P* **171** *L* **39** # r04-37

Yseboodt, Lennart
Philips Lighting

*Comment Type* **T** *Comment Status* **X** *PSE Power*

OOS

"V Port_PSE_diff , as defined in Table 145-16, is the maximum voltage difference between pairs with the same polarity, at no load condition, when operating over 4 pairs, in a power on state."

V Port_PSE_diff is maximum 10mV.

This requirement only holds at a no load condition and was introduced to control current unbalance. However, at no load, there is no unbalance issue. And we have a pretty tight test for current unbalance. I would assert that if a PSE can meet the PSE unbalance test, VPort_PSE_diff does not do anything.

It's a meaningless parameter that is tricky to measure.

*SuggestedRemedy*

- Remove item 2 (VPort_PSE_diff) from Table 145-16
- Remove subclause 145.2.10.2
- Strike sentence on page 178 line 4:
" Effective resistances of R PSE_min and R PSE_max include the effects of V Port_PSE_diff as defined in Table 145-16 and the PSE PI resistive elements."
- Change on page 218, line 28:
"R source_min and R source_max represent the V source source common mode effective resistance that consists of the PSE PI components (R PSE_min and R PSE_max as defined in 145.2.10.5.1, V Port_PSE_diff as defined in Table 145-16, the link section resistance, and influence of R PD_min and R PD_max as function of system end-to-end unbalance)."
to read (note the parens have moves also):
"R source_min and R source_max represent the V source source common mode effective resistance that consists of the PSE PI components (R PSE_min and R PSE_max as defined in 145.2.10.5.1), the link section resistance, and influence of R PD_min and R PD_max as function of system end-to-end unbalance)."

*Proposed Response* *Response Status* **W**

TFTD

TFTD YD
"Yair: 1. The Vport_PSE_diff=10mV cannot be removed.2. In addition to unbalance, this parameter is a unique way to help us to limit implementations of PSEs that are not using single power supply with the same GND etc. This was done to simplify the spec and keep us from troubles e.g. a 4-pair PSE is implemented by 2-pair Endspan and 2-pair Midspan.3. Lennart said ""This requirement only holds at a no load condition and was introduced to control current unbalance. However, at no load, there is no unbalance issue."". This is misunderstanding of the unbalance affecting parameters. Unbalance is affected by the voltage difference between the voltage sources of two pairs of the same polarity. These voltage sources are internal and are not accessible at the PI. The only accurate way to know them is to measure it at no load because then the PI voltage equal to the value of these internal voltage sources. In addition, ONLY the no load value is affecting the unbalance at load and not the PI value of Vdiff at load. So, the above argument is incorrect.3.1 As a result, it is not ""meaning less"" parameter.3.2 It is also not ""tricky to measure"". You already need to measure Vport_PSE-2P on all pairs so you can extract Vdiff.3.2.1 One way to measure at no load is to measure PSE Vdiff at MPS level and it is accurate as at zero current.3.3 This parameter is critical for the PSE implementer to limit PSE unbalance contribution. Based on this number all the other requirements of unbalance are useless (Rload_min/max, Rsource_min/max in the test verification models). PSE vendor can't design for Pse_vdiff=30mV and use the test verification models to check if it meets Iunbalance….since those models where derived for 10mV max in PSE and 60mV max in PD.3.4 All the numbers in the spec; Icon-2P_unb, Ipeak-2P_unb, ILIM-2P are based on it."

*Cl* **145** *SC* **145.2.10** *P* **174** *L* **20** # r04-38

Yseboodt, Lennart — Philips Lighting

*Comment Type* **TR** *Comment Status* **D** *PSE Cap*

OOS

Item 23 in Table 145-16 (Cout) is defined as "Output capacitance during detection state over a pairset". This is untestable as there is no deterministic way to know when the PSE is IN the detection state. Furthermore any kind of measurement would be frustrated by the changing detection voltages.

Will someone think of the test engineers for once!?

Also, p161.5 says "Output capacitance shall be as defined in Table 145-16."
Which would force the output capacitance to be limited in ALL states.

Why is Cout even in Table 145-16 if it only applies during detection ?

*SuggestedRemedy*

- Delete Cout from Table 145-16
- Add new item to Table 145-7:

Item 6, 'Pairset output capacitance', Cout, nF, min ---, max 520

Change quoted sentence to read:
"Output capacitance shall be as defined in Table 145-16, when VPSE is in the range of 0V to Vvalid max."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD, shouldn't this apply to Connection Check as well? Pretty much all detection specs should apply to CC…

TFTD YD
"Yair:1. Cout limit was specified for detection in order to prevent timing issues in detection and guarantee reasonable convergence time to 1% of steady state.2. In addition, when PSE is detection PSE, the detected PSE is external device that its output capacitance need to be limited in order to get correct valid or invalid detection as function of time constant that can create errors.So, we must specify Cout and we need a shall requirement for its maximum value4. Cout may be moved to detection section and yes ut should be specified for detection AND connection check. 5. It is easy to test for Cout. You can test it by removing the device from power and measuring Cout by a capacitance meter. You can measure Cout by analyzing V,I,t plots when checking detection etc. 6. We must have a shall that limits Cout as it was so far otherwise we will have interoperability and functional issues when PSE will try to detect PSEs. The proposed remedy just move Cout to Table 145-7 BUT THERE IS NO SHALL THAT FORCE MEETING Table 145-7 old and new added parameters."

TFTD LY
Yes, this also applies to CC.
In general, during CC all of the detection electrical requirements apply. This shall (and other shalls) refer to "when VPSE is in the range of 0V to Vvalid max". So it automatically covers CC as well.

*Cl* **145** *SC* **145.2.10.1** *P* **175** *L* **3** # r04-39

Yseboodt, Lennart — Philips Lighting

*Comment Type* **TR** *Comment Status* **D** *PSE Power*

OOS

"The specification for V Port_PSE-2P in Table 145-16 shall be met with a load step of (I Hold max x V Port_PSE-2P min) to the maximum power per the PSE's assigned Class at a rate of change of at least 15 mA/ms."

We seem to have a difficult relation with minimums and maximums.
Per this requirement, VPort_PSE-2P needs to be met at any change greater than 15mA/uS up to instanteneous current changes.
Anything changing slower... is excluded from this shall ? But is picked up by the VPort_PSE-2P item in Table 145-16... ?

Assumption: this 802.3at era text probably wanted to have the shall no longer apply at rate of change faster than 15mA/us...
Remedy written under this assumption.

*SuggestedRemedy*

"The specification for V Port_PSE-2P in Table 145-16 shall be met with a load step of (I Hold max x V Port_PSE-2P min) to the maximum power per the PSE's assigned Class at a rate of change of up to 15 mA/ms."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
Yair: At the remedy, it is "us" and not "ms"

*Cl* **145** *SC* **145.2.10.5** *P* **176** *L* **28** # r04-23

Stewart, Heath — Analog Devices Inc.

*Comment Type* **E** *Comment Status* **D** *PSE Power*

It is unclear how to parse the sub-bullets. Are they being used as an AND or an OR? Propose to add clarity.

When powering a single-signature PD over 4 pairs, a PSE supports:
- A total current of ICon, defined in Equation (145-9), over both pairs with the same polarity;
- A minimum current of ICon-2P-unb on both the positive pair and the negative pair with the highest current to account for pair-to-pair unbalance.

*SuggestedRemedy*

Change:
When powering a single-signature PD over 4 pairs, a PSE supports:
- A total current of ICon, defined in Equation (145-9), over both pairs with the same polarity;
- A minimum current of ICon-2P-unb on both the positive pair and the negative pair with the highest current to account for pair-to-pair unbalance.
To:
When powering a PD over 4 pairs, a PSE provides at least:
- A total current of Icon, defined in Equation (145-9), over both pairs of the same polarity, and,
- A current of Icon-2p-unb on both the positive pair and the negative pair with the highest current to account for pair-to-pair unbalance.
A PSE may remove power when either of these conditions is not met, as shown in Figure 145-23 and Figure 145-24.

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

Change:
When powering a single-signature PD over 4 pairs, a PSE supports:
- A total current of Icon, defined in Equation (145-9), over both pairs with the same polarity;
- A minimum current of Icon-2P-unb on both the positive pair and the negative pair with the highest current to account for pair-to-pair unbalance.
To:
When powering a PD over 4 pairs, a PSE is capable of providing at least:
- A total current of Icon, defined in Equation (145-9), over both pairs of the same polarity, and
- A current of Icon-2p-unb on both the positive pair and the negative pair with the highest current to account for pair-to-pair unbalance.

TFTD YD
"Yair:1. I agree that the ""and"" between the two parts is missing.2. I disagree to add the last part ""A PSE may remove power when either of these conditions is not met, as shown in Figure145-23 and Figure 145-24."" since this is not the place and it is already addressed. In addition, Icon-2P_unb and Icon are not equals in terms of protection. All of our protections are based on ""per 2-pair"" and Icon for example cant replace it since Icon is not sensitive for Unbalance violation."

TFTD YD
To remove any possible ambiguity, make the last bullet:
- A current of Icon-2p-unb on both the positive pair with the highest current and the negative pair with the highest current to account for pair-to-pair unbalance.

*Cl* **145** *SC* **145.2.10.6** *P* **180** *L* **31** # r04-40

Yseboodt, Lennart — Philips Lighting

*Comment Type* **T** *Comment Status* **D** *Editorial*

OOS

"A PSE that provides current on both pairsets during POWER_UP shall complete power up within T Inrush max, starting when the first pairset exceeds a voltage of 30 V."

I don't think this applies when connected to a dual-signature PD.

*SuggestedRemedy*

"A PSE, connected to a single-signature PD, that provides current on both pairsets during POWER_UP shall complete power up within T Inrush max, starting when the first pairset exceeds a voltage of 30 V."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD

Is this change needed since I don't think the DS SD uses POWER_UP as a state (it should be _pri and _sec).

TFTD YD
"I agree to the remedy but equivalent text for dual-sig is missing.Propose to change from:

""A PSE that provides current on both pairsets during POWER_UP shall complete power up within TInrush max, starting when the first pairset exceeds a voltage of 30 V.""To: ""A PSE, connected to a single-signature PD, that provides current on both pairsets during POWER_UP shall complete power up within T Inrush max, starting when the first pairset exceeds a voltage of 30 V. A PSE, connected to a dual-signature PD, that provides current on a pairsets during POWER_UP_PRI or POWER_UP_SEC shall complete power up within T Inrush max starting when the pairset exceeds a voltage of 30 V"""

TFTD LY
Agree - no change is needed.

*Cl* **145** *SC* **145.2.10.6** *P* **180** *L* **35** # r04-41

Yseboodt, Lennart — Philips Lighting

*Comment Type* **TR** *Comment Status* **D** *PSE Power OOS*

"PSEs that have assigned Class 5 or Class 6 to a single-signature PD transition to 4-pair mode by T Inrush ."

The intent here is to say that they need to have completed inrush, and operate in 4-pair, in POWER_ON, within Tinrush of the first pairset switching to INRUSH.

We already have:
- "A PSE that has assigned Class 5 to 8 to a single-signature PD shall apply power to both pairsets while in POWER_ON." (p175.11)
- "A PSE that provides current on both pairsets during POWER_UP shall complete power up within T Inrush max, starting when the first pairset exceeds a voltage of 30 V." (p180.31)

Do we need the quoted requirement ? I think it is covered by the other two.

*SuggestedRemedy*

Strike:
"PSEs that have assigned Class 5 or Class 6 to a single-signature PD transition to 4-pair mode by T Inrush ."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD

*Cl* **145** *SC* **145.2.10.8** *P* **183** *L* **26** # r04-42

Yseboodt, Lennart — Philips Lighting

*Comment Type* **TR** *Comment Status* **X** *Pres: Yseboodt2*

p181.33 "A PSE may remove power from the PI if the current on any pair meets or exceeds the "PSE lowerbound template" in Figure 145-23 or Figure 145-24."

p183.26 "The PSE shall limit the pairset current to I LIM-2P for a duration of at least T LIM."

p184.1 "If a short circuit condition is detected on a pairset, power removal from that pairset shall begin within T LIM as defined in Table 145-16."

p184.5 "A PSE in a power on state may remove power from that pairset without regard to T LIM when the pairset voltage no longer meets the V Port_PSE-2P specification."

These statements are in conflict, both in intent and in precise wording.

*SuggestedRemedy*

Adopt yseboodt_02_0518_ilimtlim.pdf

*Proposed Response* *Response Status* **W**

TFTD

WFP

TFTD YD
"Yair: I don't see conflict between all 4 locations:1. The following is MAY REMOVE for the PSE lowerbound template: p181.33 ""A PSE may remove power from the PI if the current on any pair meets or exceeds the ""PSE lowerbound template"" in Figure 145-23 or Figure 145-24.""2. The following is a SHALL for pairset current ILIM-2P and TLIM: p183.26 ""The PSE shall limit the pairset current to I LIM-2P for a duration of at least T LIM."" This may require clarification that it applies to Vpse op range and also ""for at least Tlim"" need to be adressed.3. The following is a SHALL for short circuit and power removal within TLIM: ""p184.1 ""If a short circuit condition is detected on a pairset, power removal from that pairset shall begin within T LIM as defined in Table 145-16."" (similar to (2).4. The following is about removing power at T<TLIM when voltage is below Vpse_min: p184.5 ""A PSE in a power on state may remove power from that pairset without regard to T LIM when the pairset voltage no longer meets the V Port_PSE-2P specification.""Items (2) and (4) are completely orthogonal.Item (2) may also be clarified that is meant to support transient condition as lon as PSE is in the correct operating range."

*Cl* **145** *SC* **145.3.3.3.5** *P* **195** *L* **28** # r04-57

Lemahieu, Joris — ON Semiconductor

*Comment Type* **T** *Comment Status* **X** *PSE Power*

When the PSE has allocated the PD Class 7 or Class 8 power, it should not be an issue if the PD would already draw Class 4 power in the POWER_DELAY state.
The PD can actually use Class 3 power (13W) over each 2-pair, hence Class 4 power (25.5W) in total should be possible.

Nothing needs to be changed in the dual-signature state machine.

*SuggestedRemedy*

Replace
pd_max_power <= min(3, pd_req_class)
with
IF (pse_power_level = 8) THEN
pd_max_power <= min(4, pd_req_class)
ELSE
pd_max_power <= min(3, pd_req_class)
END

*Proposed Response* *Response Status* **W**

TFTD

Why would anyone build a PD that uses 13W during Power Delay when assigned class 6 or less, but uses 25W during Power Delay when assigned class 7 or 8?

TFTD YD
"Yair: I agree that the limit of class 3 during POWER_DELAY for assigned class 7 or 8 doesn't make sense.Regarding David Abramson question ""Why would anyone build a PD that uses 13W during Power Delay when assigned class 6 or less, but uses 25W during Power Delay when assigned class 7 or 8?"": The answer is: class 8 PDs may need more power during POWER_DELAY to keep important circuits in PD still ON than Class 6 PDs.Why we care why would anyone build such a PD. The only questions I believe we should care are:-Does the comment makes sense-Does building such PDs will create issues?At this point of time the comment makes sense to me, it give more flexibility to PDs, and I couldn't find issues of we accept the remedy. The remedy cover the previous behavior and allow class 4 power during POWER_DELAY when the assign class is 8."

TFTD LY
The time spent in the POWER_DELAY state is precisely 30 milliseconds. What purpose does this serve except further complicate the spec ? May have unintended side-consequences to make a change like this, this late in the process.

*Cl* **145** *SC* **145.3.3.3.5** *P* **195** *L* **38** # r04-59

Lemahieu, Joris — ON Semiconductor

*Comment Type* **T** *Comment Status* **X** *NoPower*

A PD can trick a PSE that implements a minimum IInrush below 400mA (only 60 mA required) when VPSE is between 10 V and 30 V. If the PD requests Class 8 power and then makes the Vpse voltage collapse below the Vmark threshold (with the lower than 400mA current limit at Vmark), according to the state machine it is allowed to use Class 8 power.

*SuggestedRemedy*

Remove the NOPOWER_INRUSH state.

*Proposed Response* *Response Status* **W**

TFTD

Should we create a new variable to replace Iinrush_PD_max that takes the lower current template into consideration?

TFTD YD
"This comment shows another example shown during the last cycles for how adding a state that doesn't happen with compliant PD behavior, creates a situation that a PD that request class 8 is assigned to class 8 by tricking a PSE that uses I<Iinrush_PD_max (60mA) when voltage is between 10-30V. As I said in previous comment cycles"" There are infinite non compliant behaviors and we can't cover them all. We need to cover in the state machine only what we define as compliant behavior.Regarding David A proposal: I am note sure that it will completely solve the problem:a) If we create new variable e.g. Iinrush_PD_min and use it as a condition to enter NOPOWER_INRUSH: (VPD < VMark_th) * (IPort < IInrush_PD_min) then we will get the same problem with Iport<Inrush_PD_min.b) I remember that in previous comment cycle the current condition was a trick to differentiate between who cause the problem and we need to verify that this logic stays. "

TFTD LY
We have piled fix upon fix to cover increasingly bizarre scenario's.
Suggest to remove NOPOWER_INRUSH and trust that compliance vendors will not test for behavior under conditions no PSE would ever cause.
NOPOWER_INRUSH has opened a much bigger hole than the problem it tried to solve.

*Cl* **145** *SC* **145.3.3.4.1** *P* **196** *L* **42** # r04-60

Darshan, Yair

*Comment Type* **T** *Comment Status* **D** *PD Power*

In the text "VOff_PD_min The minimum PD off voltage VOff_PD min (see Table 145-25)", Voff_Pdmin is not in Table 145-25. It is in Table 145-29.

*SuggestedRemedy*

Change link from Table 145-25 to Table 145-29

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD HS
Also,
145.3.3.3.1 p189 l33
VOff_PD_min The minimum PD off voltage VOff_PD min (see Table 145 -25) to Table 145-29
145.3.3.3.5 p196 l28
NOTE 2 --In general, there is no requirement for a PD to respond with a valid class signature for any DO_CLASS_EVENT duration less than TClass_PD as defined in Table 145 -29. to Table 145-25
145.3.6.1 p204 l52
After entering a DO_CLASS_EVENT state, the PD Physical Layer class signature shall be valid within TClass_PD as defined in Table 145 -29 to Table 145-25

*Cl* **145** *SC* **145.3.3.4.2** *P* **196** *L* **51** # r04-43

Yseboodt, Lennart Philips Lighting

*Comment Type* **TR** *Comment Status* **D** *PD SD*

OOS

The dual-signature state diagram makes use of mdi_power_required_mode(X), which can be set separate for both Modes. This would, for instance, allow a dual-signature PD to not show a valid detection signature when powered over 2-pair.
This breaks a number of other requirements, but is permitted by the state diagram.

*SuggestedRemedy*

- Change the variable mdi_power_required_mode(X) to be the same as the single-signature variable mdi_power_required
- Replace mdi_power_required_mode(X) by mdi_power_required_mode in the state diagram

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD

TFTD YD
Yair: The comment and remedy make sense for the beginning of operation of dual signature but is incorrect after it operates in 4-pair and for some reason power is turned off from one of the alternatives

*Cl* **145** *SC* **145.3.4** *P* **201** *L* **50** # r04-67

Yseboodt, Lennart

*Comment Type* **T** *Comment Status* **X**

--THIS COMMENT WAS SUBMITTED AFTER THE COMMENT PERIOD ENDED, IT WILL BE CONSIDERED IF NO ONE IN THE COMMENT RESOLUTION GROUP OBJECTS.--
"A single-signature PD that is powered over only one pairset shall present a non-valid detection signature on the
unpowered pairset. A dual-signature PD that is powered over only one pairset shall present a valid detection
signature on the unpowered pairset."

Does not unambiguously handle 3-pair.

*SuggestedRemedy*

Change to:
"A single-signature PD that is powered per any valid 2-pair configuration, as defined in Table 145-20, shall present a non-valid detection signature on the unpowered pairset.
A dual-signature PD that is powered per any valid 2-pair configuration, as defined in Table 145-20, shall present a valid detection signature on the unpowered pairset."

*Proposed Response* *Response Status* **W**

TFTD

TFTD YD
"Yair: This is tied with the complete 3-pair discussion and can not be resolved independently.If in single-signature PD, backfeed will be allowed in 3-pair than we should accept this comment."

*Cl* **145** *SC* **145.3.4** *P* **202** *L* **27** # r04-44

Yseboodt, Lennart Philips Lighting

*Comment Type* **TR** *Comment Status* **X** *PD Detection*

OOS

Table 145-21 indicates that a PD must show a valid Rdetect between 2.7V and 10.1V.
The state diagram however, forces the PD into IDLE if the PI voltage is less than 2.81V. In IDLE present_det_sig=either.

This is in conflict for the range 2.7 to 2.81 volt.
Note that the same gap exists in Clause 33.

*SuggestedRemedy*

The solution is to slice off 100mV of the PSEs detection range, and change the PD descriptive text to match with the state diagram.

- page 202, Table 145-21, change Conditions "2.7V to 10.1V" to read "2.81V to 10.1V" (3x)
- page 203, Figure 145-28, change 2.7 into 2.81
- page 203, line 24, change "3.7V" into "3.81V"
- page 161, Table 145-7, change VValid range to be from 2.9 to 10V

*Proposed Response* *Response Status* **W**

TFTD

We need to consider this carefully as existing PSEs can start detection at 2.8V, this change may cause interoperability problems. Is there a way to say that in the IDLE state, if the votlage > 2.7, the present_det_sig <= true?

TFTD YD
"Yair: 1. There are PSEs that start to detect at 2.8V so we can't change it to 2.9V (interoperability issue) 2. The proposed remedy contain many changes. I proposed instead, to change the PD state machine to go to IDLE at <2.7V instead of 2.81V which means to change only Vreset_PD in Table 145-25. I am aware that we move now th eburden of the fix to the PD but it make more sense in the PD since valid detection in the PD was always 2.7V to 10V which means the reset of the PD must be also <2.7V."

Response DNA: This would require changing the PSE requirement for reset voltage to 2.7V (from 2.8V).

TFTD DNA: How about describing in text the detection behavior in IDLE. So that we explain if the voltage is above 2.7V in IDLE, present detect sig = true.

*Cl* **145** *SC* **145.3.6** *P* **203** *L* **47** # r04-45

Yseboodt, Lennart — Philips Lighting

*Comment Type* **TR** *Comment Status* **D** *Editorial*

OOS

"The PD shall draw no more power across all input voltages than defined for the requested Class in Table 145-26 and Table 145-27."

This is a needlessly hard to meet requirement.
PDs that operate close to PClass_PD, but are exposed to voltage lower than VPort_PD-2P MIN, and behave as a constant-power device, would need to guard power consumption between Voff_PD and VPort_PD-2P MIN.
This requirement should only apply when the PD is exposed to a valid powering voltage.

*SuggestedRemedy*

"The PD shall draw no more power across any voltage in the range of VPort_PD-2P than defined for the requested Class in Table 145-26 and Table 145-27."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD DS
What is the specified max power draw for a PD in the range of VOff_PD and VPort_PD-2P,min? (That is, does removing this requirement address the commenters stated concern?)

*Cl* **145** *SC* **145.3.8.3** *P* **212** *L* **49** # r04-58

Lemahieu, Joris — ON Semiconductor

*Comment Type* **G** *Comment Status* **D** *PD Inrush*

Single reference to Tdelay-2P.

*SuggestedRemedy*

Replace
Tdelay-2P
by
TInrush_PD
or by
TInrush_PD max

If TInrush_PD max is chosen, then it seems like there is no longer a configurable TInrush_PD. Only TInrush_PD max is used. Then the emdash for TInrush_PD Min in Table 145-29 on page 209 could be replaced by 50 for clarity.

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace "Tdelay-2P" by "Tdelay"

TFTD YD
"Yair; Tdelay-2P is not Tinrush or Tinrush_PD_max.Just change Tdelay-2P to Tdelay"

Response DNA: Yair, that is exactly what my response says.

*Cl* **145** *SC* **145.3.8.8** *P* **216** *L* **37** # r04-47

Yseboodt, Lennart — Philips Lighting

*Comment Type* **TR** *Comment Status* **X** *Pres: Yseboodt1*

"When any voltage in the range of 0 V to V Port_PD-2P max is applied across the PI at either polarity specified on the conductors of either Mode A or Mode B according to Table 145-20, the voltage measured across the PI for the other Mode with a 100 kOhm load resistor connected across that other Mode shall not exceed V bfd as defined in Table 145-29."

We need to clarify the backfeed spec.

*SuggestedRemedy*

Adopt yseboodt_01_0518_backfeed.pdf

*Proposed Response* *Response Status* **W**

TFTD

WFP

TFTD YD
Yair: I have presentation too. darshan_01_0518.pdf

*Cl* **145** *SC* **145.3.8.8** *P* **216** *L* **37** # r04-63

Darshan, Yair

*Comment Type* **T** *Comment Status* **D** *Backfeed*

This comment is marked BACKFEED-DUAL.
The current text requring to meet backfeed should cover both single-signature and dual-signature PDs (and it looks like that it does) however dual-signature PD must meet backfeed in any operation modes; 2-pair, 3-pair or 4-pair otherwise the PD will show invalid-signature on the unpowered mode and/or PSE will fail to detect valid signature due to higher offset voltage.

*SuggestedRemedy*

1. Add after line 40 dedicated backfeed requirement for dual-signature (the first paragraph will be reserved for single-signature PD 3-pair discussion if it is going to be changed):
"When any voltage in the range of 0 V to VPort_PD-2P max is applied across the PI at either polarity specified on the conductors of either Mode A or Mode B according to Table 145-20 for any valid 2-pair or 4-pair configuration, the voltage measured across the PI for the other Mode with a 100 kohm load resistor connected across that other Mode shall not exceed Vbfd as defined in Table 145-29."

*Proposed Response* *Response Status* **W**

PROPOSED REJECT.

You are correct that DS PDs cannot backfeed in any 2-pair configuration (including 3-pair power). But if they do, they will fail the detection requirements of a DS PD (to show a valid signature on one pairset, when the other is powered). Thus DS PDs are already not allowed to backfeed (they can't use the bridges that backfeed with 3-pair power). There is no reason to add this extra sentence (which by the way, would apply to all PDs since it never mentions that it only applies to DS PDs).

TFTD YD
"Yair:1. It will be better to discuss this comment after we decide what to do with backfeed for 3-pair in single-signature PDs.2. David, you are correct in your analysis and I thought about it too i.e. the requirement of valid signature include Rsig value and offset voltage etc. However backfeed is not offset voltage at the PD. They are two different things. Offset is the forward voltage of the diode and backfeed is low energy/voltage/current transferred back to the PSE. For the PSE it looks the same i.e. if you have backfeed > 2.8V e.g. 4V, the PSE may detect a valid signature due to the fact that PSEs uses differential measurement to detect Rsig and a 4V backfeed will look like a 4V offset and will be canceled resulting by Valid 25K signature. I agree that in the PD tests backfeed>2.8V will not be a compliant behavior but I am not sure that it will be sufficiently clear to the designer. Therefore we need specific text for dual-signature PDs.3. Yes in the proposed new text I forgot to mention that it is for dual-signature (I said it in the comment but not correctly implement it in the text) so here is a revised remedy:a) Keep the current text for single-signature (If backfeed will include 3-pair then the existing text can be used for both single or dual-sig with some clarifications) however I prefer two separate text for clarity due to the importance of it .b) Add the following text after line 40:""When any voltage in the range of 0 V to VPort_PD-2P max is applied across the PI of a dual-signature PD at either polarity specified on the conductors of either Mode A or Mode B according to Table 145-20

for any valid 2-pair or 4-pair configuration, the voltage measured across the PI for the other Mode with a 100 kohm load resistor connected across that other Mode shall not exceed Vbfd as defined in Table 145-29."" "

*Cl* **145** *SC* **145.3.8.8** *P* **216** *L* **40** # r04-64

Darshan, Yair

*Comment Type* **T** *Comment Status* **X** *Pres: Darshan1*

The issue is:
Failing to meet Backfeed voltage in D3.4 when 4-pair PSE is connected to single-signature PD equipped with a specific implementation of ideal-diode bridge that doesn't work correctly in a 3-pair mode which result in maximum PD input voltage backfeed to the unpowered PSE alternative. This ideal diode bridge doesn't behave as expected from diode based bridges that do not have this problem.
The above behavior is a violation of two important principles we have so far:
a) Clause 145.3.2 Page 188 Line 3: "The PD shall not source power on its PI."
b) Clause 145.3.8.8 Page 216 Lines 35-40: The backfeed requirement currently required for 2-pair, 3-pair and 4-pair modes.

Now we need at a very late stage in the project to examine all possible use cases that may cause damage or interoperability issues to PSEs if we want to exclude 3-pair mode from meeting backfeed OR we can keep the current text that in my opinion cover all valid 2-pair (3-pair) and 4-pair modes per Table 145-20 in the PD to meet backfeed requirements.
The safe and worry free thing to do I believe, is to include 3-pair mode however, there is one main argument that need to be discussed that suggest excluding 3-pair mode from meeting backfeed.
See darshan_01_0518.pdf for details of what was tested and what needs more inputs frpm PSE/PD vendors.

*SuggestedRemedy*

Option 1:
Keep the current backfeed text. It covers 3-pairs and both single-signature and dual-signature PDs.

Option 2:
If and only if we are all convinced that there are no issues to exclude 3-pair mode, to modify the current text and use it for single signature and add the text for dual-signature to include all 2-pair and 4-pair modes per table 145-20. This text is proposed in my comment marked BACKFEED-DUAL.
See darshan_01_0518.pdf for updated comment and remedy as this topic is still in evaluations and discussions.

*Proposed Response* *Response Status* **W**

TFTD

WFP

I don't agree that the current text applies to all cases. It is an exact copy from AT, which means that it was written for a world that did not include 3-pair or 4-pair power. However, I do agree that we need to clarify this.

TFTD YD
Yair: The current text is not 100% a copy of what we have in 802.3af/at. There is Table 145-

20 that we have change to include all Lennart's operating mode... The current text doe's include 3-pair in the 2-pair section in Table 145-20. See details on page 4 at darshan_01_0518.pdf that show it clearly or in 802.3bt D3.4 page 188 lines 19, 26-37.

Response DNA: yes, the table was pointed to, but just for the definition of Mode A and Mode B, not for the valid configurations (the sentence itself tells you how to connect things).

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*Cl* **145** *SC* **145.3.9** *P* **219** *L* **46** # r04-49

Yseboodt, Lennart — Philips Lighting

*Comment Type* **T** *Comment Status* **D** *Editorial*

"A PD shall meet the TMPS_PD and TMPDO_PD requirements with any series resistance in the range of RChan max between the PD PI and the source."

Rchan max is not a range but a value.

*SuggestedRemedy*

Change to:
"A PD shall meet the TMPS_PD and TMPDO_PD requirements with any series resistance up to RChan max between the PD PI and the source."

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD DS
Replace “up to” with “less than or equal to”

Change to:
"A PD shall meet the TMPS_PD and TMPDO_PD requirements with any series resistance less than or equal to RChan max between the PD PI and the source."

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*Cl* **145** *SC* **145.4.1** *P* **221** *L* **37** # r04-61

Darshan, Yair

*Comment Type* **T** *Comment Status* **X** *Backfeed*

As a result of darshan_01_0518.pdf which shows that higher backfeed voltage may increase cross pairs/port leakage current and increase PSE susceptibility to detection pollution, it is recommended to add link to the backfeed requirement in the text: "In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents."

*SuggestedRemedy*

Change from: "In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents."
To: "In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents. See 145.3.8.8.

*Proposed Response* *Response Status* **W**

TFTD

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*Cl* **145** *SC* **145.5.3.3.1** *P* **245** *L* **42** # r04-51

Yseboodt, Lennart — Philips Lighting

*Comment Type* **TR** *Comment Status* **D** *DLL*

There are mistakes in the "valid values" for the DLL variable lists.

*SuggestedRemedy*

Change as follows:
// (PSE section)
- p236.12 MirroredPDRequestedPowerValue: 0 through 999, and 0xACAC
- p236.23 MirroredPSEAlloctedPowerValueEcho: 0 through 999, and 0xACAC
- p236.33 PDRequestedPowerValueEcho: 0 through 999, and 0xACAC
- p236.45 PSEAllocatedPowerValue: 0 through 999, and 0xACAC
- p237.16 TempVar: 0 through 999, and 0xACAC

// (single-sig PD section)
- p245.5 MirroredPDRequestedPowerValueEcho: 1 though 999, and 0xACAC
- p245.42 PDRequestedPowerValue: 1 through pd_dllmax_value, and 0xACAC
- p245.49 PDRequestedPowerValue_mode(X): 0
- p246.39 PSEAllocatedPowerValueEcho: 1 through 999, and 0xACAC
- p246.44 PSEAllocatedPowerValueEcho_mode(X): 0

// (dual-sig PD section)
- p251.23 MirroredPSEAlloctedPowerValue: 0 through 999
- p251.30 DELETE PDMaxPowerValue
- p251.39 PDMaxPowerValue_mode(X): 1 through 499
- p251.45 PDRequestedPowerValue: 0 through pd_dllmax_value_mode(P)

*Proposed Response* *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
Yair: Missing the justification for the proposed remedy. Lennart to explain and include it in the comment response

Response DNA: Yair, most of these have only changed if 0 or 1 is the minimum valid value. I went through these with Lennart and they all look correct.

*Cl* **145** *SC* **145.6.5** *P* **262** *L* **9** # r04-54

Yseboodt, Lennart
Philips Lighting

*Comment Type* **T** *Comment Status* **X** *AES*

OOS

"The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference."

This requirement applies to the CABLE connecting the PSE and the PD and links to 'applicable codes' that are not in our purview.

Out of scope for our document and provides no value.

*SuggestedRemedy*

Delete 145.6.5.

*Proposed Response* *Response Status* **W**

TFTD

That is a holdover from AT.

TFTD YD
"Yair: 1. We need it and we cannot delete it.2. It is part of Objective (implicite). 3. We need to meet local and national EMI codes for PSEs and PDs with their cables when they are powered or not. 4. The value of this text is that the common mode ripple and noise specified in Table 145-16 and Table 145-29 are not sufficient to meet EMI and much lower values are required.5. It is specified for all IEEE systems and subsystems."