Cl **1**   *SC* **1.4**   *P* **20**   *L* **35**   *#* 126
Stewart, Heath   LTC

Comment Type **T**   *Comment Status* **D**   *Pres: Stewart2*

Number of specified PD configurations may be reduced.

SuggestedRemedy

See stewart_2_0116.pdf

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **1.4**   *SC* **1.4**   *P* **20**   *L* **39**   *#* 21
Darshan, Yair   Microsemi

Comment Type **T**   *Comment Status* **D**   *Definitions*

In the definitions of Type3 and 4 PDs the support of LLDP is missing in Type 3.
"Type 3 PD: A PD that provides a Class 1 to Class 6 signature during Physical Layer classification, implements multiple-Event classification, and accepts power on both modes simultaneously (see IEEE 802.3, Clause 33)."

"Type 4 PD: A PD that provides a Class 7 or 8 signature during Physical Layer classification, implements multiple-Event classification, is capable of Data Link Layer classification, and accepts power on both Modes simultaneously (see IEEE 802.3, Clause33)."

SuggestedRemedy

To implement the following proposed remedy If there is no reason why support of LLDP was omitted in Type 3 PD definition.

Change from:
"Type 3 PD: A PD that provides a Class 1 to Class 6 signature during Physical Layer classification, implements multiple-Event classification, and accepts power on both modes simultaneously (see IEEE 802.3, Clause 33)."
To:
"Type 3 PD: A PD that provides a Class 1 to Class 6 signature during Physical Layer classification, implements multiple-Event classification, is capable of Data Link Layer classification, and accepts power on both modes simultaneously (see IEEE 802.3, Clause 33)."

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

I believe we left this out because class 1-3 PDs are not required to support LLDP even if they are Type 3.

Cl **25**   *SC* **25.4.5**   *P* **24**   *L* **1**   *#* 168
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

original text: "A 100BASE-TX receiver in a Type 2 or greater Endpoint PSE or Type 2 or greater PD (see Clause 33) shall meet the requirements of 25.4.7."
in Clause 25 new types are included with the phrase "Type 2 or greater" which conceivably could be misinterpreted.

SuggestedRemedy

"A 100BASE-TX receiver in a Type 2, Type 3 and Type 4 Endpoint PSE or Type 2, Type 3 and Type 4 PD (see Clause 33) shall meet the requirements of 25.4.7."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adding serial commas:

"A 100BASE-TX receiver in a Type 2, Type 3, and Type 4 Endpoint PSE or Type 2, Type 3, and Type 4 PD (see Clause 33) shall meet the requirements of 25.4.7."

EZ

Cl **30**   *SC* **30**   *P* **28**   *L* **1**   *#* 169
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

The test that goes after BEHAVIOUR of an ATTRIBUTE should end with a period + semicolon. This is not always done.

SuggestedRemedy

Bulk-fix.

Response   *Response Status* **C**

ACCEPT.

I have no idea what you are suggesting. An example would have been very helpful.

TFTD (Task Force to Discuss).

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **28**
Li **1**

Page 1 of 55
1/21/2016 1:23:24 PM

Cl **33**   *SC* **33**   *P* **43**   *L* **1**   # 170
Yseboodt, Lennart   Philips

Comment Type   **E**   *Comment Status*   **A**   *Editorial*

In order to prepare the document for WG ballot, we should consider what our final amendment will look like.
     At the moment we are using Change/Add/Delete editing instructions at the paragraph and section level.
     This has become quite convoluted.

     The 802.3at endearment to 802.3-2008 replaced the complete Clause.
     Since we are changing at least as much as the .at TF did, this seems like a good idea to repeat.

SuggestedRemedy

Add "Replace Clause 33 with the following:" before the Clause 33 title.
     Remove redundant editing instructions.

Response   *Response Status*   **C**

ACCEPT.

Cl **33**   *SC* **33**   *P* **43**   *L* **1**   # 171
Yseboodt, Lennart   Philips

Comment Type   **E**   *Comment Status*   **A**   *Editorial*

The change bars in the draft are intended to show us where changes have been made.
     The current change bars are the accumulative result of 9 draft revisions.
     As a result on many pages the change bar is a continuous black line (there is nearly no part of the text untouched).

     A possibility, which I believe will aid us in subsequent reviews, would be to reset the change bars for every draft. It would then be clearly visible which text has been touched as a result of the current draft cycle.

     Question to the TF: which would you prefer?
     - Maintain change bars as is
     - Reset change bars for every draft

SuggestedRemedy

TFTD (Task Force To Decide)

Response   *Response Status*   **C**

ACCEPT IN PRINCIPLE.

Lennart to reset the change bars after deleting the editing instructions. Lennart to create diff document for D1.6 to 2012.

Cl **33**   *SC* **33.1.4**   *P* **46**   *L* **6**   # 89
Lukacs, Miklos   Silicon Labs

Comment Type   **E**   *Comment Status*   **A**   *Editorial*

The title of the clause refers to Type 1 and 2 only.

SuggestedRemedy

Replace the title with:
System parameters

Response   *Response Status*   **C**

ACCEPT.

This was already done. D1.4 shows the title as "System Parameters". Somehow that got reversed.

EZ

Cl **33**   *SC* **33.1.4**   *P* **46**   *L* **6**   # 149
Johnson, Peter   Sifos Technologies

Comment Type   **E**   *Comment Status*   **A**   *Editorial*

Heading for 3.1.4 is Type 1 and Type 2 System parameters. Needs updating.

SuggestedRemedy

Change to:

System Parameters for Type 1, 2, 3, and 4 Systems

Response   *Response Status*   **C**

ACCEPT IN PRINCIPLE.

OBE by 89.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **46**   Page 2 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **6**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33** *SC* **33.1.4** *P* **46** *L* **9** # 90
Lukacs, Miklos Silicon Labs

Comment Type **E** *Comment Status* **A** *Editorial*

The text is talking about that PSEs and PDs are categorized by Type. However Types are not mentioned anyhow in the refernced tables (table 33-1, below the text). This is confusing, because the reader may think that the basic system parameters are based on Type.

SuggestedRemedy

Leave out the cited section from the first sentence:
"A power system consists of a single PSE, link segment, and a single PD."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 172

TFTD

Cl **33** *SC* **33.1.4** *P* **46** *L* **17** # 172
Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *Editorial*

Table 33-1 has become a bit clunky due to the Type 4 power range discussion. Using Class seems out of place.

SuggestedRemedy

Change Table caption to: "System parameters"
Change column 1 header to: "PSE Type"
Change column 1 entries into: "Type 1, Type 2, Type 3, Type 4"

Response *Response Status* **C**

ACCEPT.

This is reversing a change we made at the last meeting.

TFTD.

Cl **33** *SC* **33.1.4** *P* **46** *L* **36** # 150
Johnson, Peter Sifos Technologies

Comment Type **E** *Comment Status* **A** *Editorial*

Footnote 2: In Type 3 and Type 4 oeratoins, the current per pairset will be impacted by pair-to-pair system unbalance...

Pair-to-Pair unbalance not applicable if Dual Signature. Change "will" to "may".

SuggestedRemedy

In Type 3 and Type 4 oeratoins, the current per pairset may be impacted by pair-to-pair system unbalance...

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In Type 3 and Type 4 operations, the current per pairset may be impacted by pair-to-pair system unbalance…

NonEasy

Cl **33** *SC* **33.1.4** *P* **46** *L* **44** # 151
Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **A** *System Parameters*

The sentence:

All four twisted pairs, connected from PSE PI to PD PI are required to source greater than Class 4 power at the PSE PI - ....

This is awkward and technically incorrect because wire pairs don't source power at all.

SuggestedRemedy

Revise paragraph to:

Icable is the maximum continuous current on either one or both pairsets in the multi-twisted pair cable. Each pairset consists of one pair capable of carrying (+Icable) and the other pair capable of carrying (-Icable).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

"All four twisted pairs, connected from PSE PI to PD PI are required **in order for the PSE** to source greater than Class 4 power at the PSE PI - ...."

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Cl **33**　　*SC* **33.2.0a**　　　　*P* **48**　　*L* **17**　　# 173
Yseboodt, Lennart　　　　　　　Philips

Comment Type **E**　　*Comment Status* **A**　　　　　*Editorial*
Table 33-1a Optional features column essentially is an Autoclass yes/no selection.

SuggestedRemedy
Change header to "Autoclass" and in column use "Yes/No".

Response　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

Change header to "Autoclass" and in column use "Optional/No".

NonEasy

Cl **33**　　*SC* **33.2.0a**　　　　*P* **48**　　*L* **23**　　# 152
Johnson, Peter　　　　　　　Sifos Technologies

Comment Type **T**　　*Comment Status* **A**　　　　　*PSE Types*
Improve readability of Table 33-1a and delete a footnote.

SuggestedRemedy
Split 'Type-2' row under 'Physical Layer Classification' and 'Data Link Layer Classification' into 2 rows with following content:

Single Event　　|　Mandatory

Multiple Event　|　Optional

Remove footnote 2.

Response　　　　　*Response Status* **C**
ACCEPT.

Cl **33**　　*SC* **33.2.2**　　　　*P* **50**　　*L* **1**　　# 189
Yseboodt, Lennart　　　　　　　Philips

Comment Type **ER**　　*Comment Status* **A**　　　　　*Editorial*
Figures 33-4* to 33-7* use "2-Pair" and "4-Pair" in their captions.
　　Should not be capitalized.

SuggestedRemedy
This should be "2-pair" and "4-pair".

Response　　　　　*Response Status* **C**
ACCEPT.

EZ

Cl **33**　　*SC* **33.2.4**　　　　*P* **57**　　*L* **35**　　# 35
Darshan, Yair　　　　　　　Microsemi

Comment Type **ER**　　*Comment Status* **A**　　　　　*Editorial*
Typo in line 35. Need to be Figure 33-10 and not 33-10e
"Type 1 and Type 2 PSEs shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10e.
Type 3 and Type 4 PSEs shall provide the behavior of the state diagrams shown in Figure 33–10a to Figure 33–10d and Figure 33–10e."

SuggestedRemedy
Change from:
"Type 1 and Type 2 PSEs shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10e.
Type 3 and Type 4 PSEs shall provide the behavior of the state diagrams shown in Figure 33–10a to Figure 33–10d and Figure 33–10e."
To:
"Type 1 and Type 2 PSEs shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10.
Type 3 and Type 4 PSEs shall provide the behavior of the state diagrams shown in Figure 33–10a to Figure 33–10d and Figure 33–10e."

Response　　　　　*Response Status* **C**
ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **57**
Li **35**

Page 4 of 55
1/21/2016 1:23:24 PM

Cl **33**	*SC* **33.2.4.1**	*P* **57**	*L* **53**	# 6

Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **A**   *PSE Power*

There is missing text that clearly sets the polarity of the PSE voltages during its operating states as the one determined right after IDLE state. The voltage polarity of all PSE operating states (Detection, Connection Check, Classification, POWER_UP and POWER_ON) must be the same.
We can find the following:
a)Clause 33.2.5.1 Figure 33-11 and Figure 33-12, we clearly see that the polarity is the same as Vpse+ and Vpse- however there is no "shall" text involved.
b)Clause 33.2.6 P.92 Line 2:
"The PSE shall provide VClass with a current limitation of IClass_LIM, as defined in Table 33-10 only for a pairset with a valid detection signature. Polarity shall be the same as defined for VPort_PSE-2P in 33.2.3 and timing specifications shall be as defined in Table 33-10."

This text requires that Vclass polarity shall be the same as defined in 33.2.3 Table 33-2. It is not sufficiently clear that Vclass polarity should track detection voltage polarity.

c)Clause 33.2.6.2 P.97 Line 38-39:
"All class event voltages and mark event voltages shall have the same polarity as defined for VPort_PSE-2P in 33.2.3."

This text requires that Vclass and Vmark polarity shall be the same as defined in 33.2.3. It is not sufficiently clear that Vclass polarity should track detection voltage polarity.
We need to make sure that:
1.POWER_UP and POWER_ON voltage polarity per 33.2.3 is similar to detection, connection check and classification polarity.
2.Changing polarity per the possibilities in 33.2.3 Table 33-2 is possible only after passing through IDLE state.
Currently, although the above is obvious, it is not clear from the standard that this is the requirement.

SuggestedRemedy

To add the following text in 33.2.4.1 page 57 after line 53:
"The polarity of PSE voltages during its operating states (Detection, Connection Check, Classification, POWER_UP and POWER_ON) shall be the same as was used in the Detection state and defined per Table 33-2 in 33.2.3."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

To add the following text in 33.2.4.1 page 57 after line 53:
"The polarity of PSE voltages during its operating states (Detection, Connection Check, Classification, POWER_UP and POWER_ON) is the same as was used in the Detection state and defined per Table 33-2 in 33.2.3."

Cl **33**	*SC* **33.2.4.4**	*P* **59**	*L* **9**	# 190

Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *PSE Power*

"Iport: Output current (see 33.2.7.6)."

The referred section only talks about Iport-2P.

SuggestedRemedy

Change first lines of 33.2.7.6 to:

"If I_Port, the current supplied by the PSE to the PI, exceeds I_CUT-2P for longer than T_CUT-2P, Type 1 and Type 2 PSEs may remove power from the PI.
If I_Port-2P, the current supplied on a pairset by the PSE to the PI, exceeds I_CUT-2P for longer than T_CUT-2P, Type 3 and Type 4 PSEs may remove power from that pairset."

Response   *Response Status* **C**

ACCEPT.

Cl **33**	*SC* **33.2.4.4**	*P* **61**	*L* **25**	# 69

Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **D**   *Editorial*

To make the specification easier to comprehend replace Table 33-3 with text. The proposed text focus the reader on differences (exceptions) rather than reiterating things already covered in other parts of the specification.

The existing sentence above the table is,
"PSEs shall meet at least one of the allowable variable definition permutations described in Table 33-3."

SuggestedRemedy

Delete Table 33-3 and the associated change statement.

Replace the called out sentence with,
"Type 1 PSEs may classify using a single event. Type 2 PSEs shall use data link layer classification, covered in 33.6, when using single event classification."

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

As we decided not to touch the Type 1/2 State Diagram, I would not recommend chanign the associated variables.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **61**
Li **25**

Page 5 of 55
1/21/2016 1:23:24 PM

Cl **33**   *SC* **33.2.4.8**   *P* **66**   *L* **40**   # 154

Johnson, Peter   Sifos Technologies

Comment Type **T**   *Comment Status* **A**   *PSE SD*

Description of CC_DET_SEQ value "1" says:
..... and both pairsets for a dual-signature PD.

Description of CC_DET_SEQ value "0" says:
..... and parallel detection for a dual-signature PD.

From the state diagram, it appears that they are both doing parallel detection for a dual
signature PD. Suggest the same phrase.

SuggestedRemedy

Change description of CC_DET_SEQ value "1" to:

..... and parallel detection for a dual-signature PD.

Response   *Response Status* **C**

ACCEPT.

Chris/Dylan: Is this correct?

Cl **33**   *SC* **33.2.4.8**   *P* **66**   *L* **41**   # 153

Johnson, Peter   Sifos Technologies

Comment Type **T**   *Comment Status* **D**   *PSE SD*

The constant CC_DET_SEQ describes four possible values with different descriptions of
behavior. However, inspecting the state diagram, I don't see any differences in state
behavior between CC_DET_SEQ= 0 and CC_DET_SEQ= 3. They are grouped together
as (CC_DET_SEQ= 0 or CC_DET_SEQ= 3) throughout the state diagram.

Issue may be here or may be in state diagram.

SuggestedRemedy

Revise description in 33.2.4.8 or state diagram (Figure 33-10a), or at least make editor
note about this.

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD (Chris/Dylan, can you comment?)

Cl **33**   *SC* **33.2.4.9**   *P* **67**   *L* **28**   # 205

Yseboodt, Lennart   Philips

Comment Type **TR**   *Comment Status* **A**   *Pres: Picard5*

class_num_events:
"A variable indicating the maximum number of classification events performed by
the PSE."

Does not take dual signature into account.

SuggestedRemedy

"A variable indicating the maximum number of classification events performed by the PSE
on a pairset."

Works for both single and dual.
Type 3 dual will produce max 3 events/pairset (and 4 is allowed and needed for
single)
Type 4 dual will produce max 4 events/pairset (and 5 is allowed and needed for
single)

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 87

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **67**   Page 6 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **28**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.4.9**   *P* **68**   *L* **1**   # 155
Johnson, Peter   Sifos Technologies

Comment Type **T**   *Comment Status* **A**   *PSE SD*

The variable det_temp is described as:

A temporary variable that indicates whether a 4-pair PSE has completed detection on only one alternative.....

This whole description is awkward and can be improved:

SuggestedRemedy

Change to:

A temporary variable that indicates whether a 4-pair PSE has completed detection on a first pairset but not on a second pairset.

Values:
0: The PSE has either not completed detection of a first pairset or has completed detection of the second pairset.
1: The PSE has completed detection of a first pairset but not the second pairset.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change to:

A temporary variable that indicates whether a 4-pair PSE has completed detection on a first alternative but not on a second alternative.

Values:
0: The PSE has completed detection on both alternatives or neither alternatives.
1: The PSE has completed detection on only one alternative.

Cl **33**   *SC* **33.2.4.9**   *P* **68**   *L* **26**   # 187
Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *Pres: Yseboodt2*

"Editor's note (remove D1.6): Variables I Port , I Port-2P , and I Port-2P-other are not present in the current variable list. Section 33.2.7 depends on these. To be resolved."

If yseboodt_2_0116_v4xx.pdf is adopted, there is no need for a definition of any of these terms in the variable list.

SuggestedRemedy

Remove note.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**   *SC* **33.2.4.9**   *P* **68**   *L* **43**   # 206
Yseboodt, Lennart   Philips

Comment Type **TR**   *Comment Status* **A**   *Pres: Yseboodt9*

The variable list for the new SM contains mr_mps_valid, which serves no purpose in the SM.
mr_mps_valid_pri and mr_mps_valid_sec supersede it.

SuggestedRemedy

Remove mr_mps_valid from the variable list.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adopt yseboodt_9_0116.pdf

Leave mr_mps_valid in the variable list pending further work.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **68**
Li **43**

Page 7 of 55
1/21/2016 1:23:24 PM

Cl **33**   *SC* **33.2.4.9**   *P* **72**   *L* **19**   # 101

Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **A**   *Pres: Picard5*

Table 33-3a provides information that may permit unintended behavior. The unintended behavior could allow Type 4 PSEs to limit power output to less than class 7 power levels. The correct information in this table already appears elsewhere in the specification.

SuggestedRemedy

Delete Table 33-3a.

Delete the sentence, on line 16,
"PSEs shall meet at least one of the allowable variable definition permutations described in Table 33-3a."

Replace the following text on line-36,
"Editor's Note (remove prior to D2.0): Table 33-3a must be updated to take dual-signature into account. Reason: when connected to a DS PD, PSEs need to produce 3 events in order to verify Type." with,

"Editor's Note (remove prior to D2.0): Provide text that covers PSE connected to a DS PD, PSEs need to produce 3 events in order to verify Type."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 207.

Cl **33**   *SC* **33.2.4.9**   *P* **72**   *L* **19**   # 95

Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Editorial*

Reference to this Table 33-3a seem to be in error.

SuggestedRemedy

On page 57, line 42, a reference to Table 33-3a is in error that should point to Table 33-3b on page 87.

On page 87 line 16, line 20, line-40 should point to Table 33-3b as well.

On page 72 line-50 Table 33-3a should reference Table 33-3b.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement suggested remedy plus:

On page 73 line-14 Table 33-3a should reference Table 33-3b.

NonEasy

Cl **33**   *SC* **33.2.4.9**   *P* **72**   *L* **23**   # 207

Yseboodt, Lennart   Philips

Comment Type **TR**   *Comment Status* **A**   *Pres: Picard5*

Type 4 PSEs are required to be capable of 5 class events.
Table 33-3a allows 1,2,4 or 5.

SuggestedRemedy

Change the value of class_num_events for Type 4 to "5".

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adopt yseboodt_10_0116_Table_33_3a.pdf as new Table 33-3a.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **72**
Li **23**

Page 8 of 55
1/21/2016 1:23:24 PM

Cl **33**   *SC* **33.2.4.9**   *P* **72**   *L* **27**   # 208
Yseboodt, Lennart   Philips

Comment Type **TR**   *Comment Status* **A**   *PSE SD*
Table 33-3a shows the allowed PSE variable definition permutations.
        Since this is in the Type 3+4 SD section, Type 1 and 2 should not be listed (that is
in Table 33-3).

SuggestedRemedy
Remove the rows for Type 1 and Type 2
        Change caption of Table to "Allowed Type 3 and Type 4 PSE variable definition
permutations"

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **33**   *SC* **33.2.4.9**   *P* **72**   *L* **36**   # 188
Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *Pres: Picard5*
"Editor's Note (remove prior to D2.0): Table 33-3a must be updated to take dual-signature
into account.
        Reason: when connected to a DS PD, PSEs need to produce 3 events in order to
verify Type."

         Not correct. We might need a bit of text in the definition of class_num_events, but
the Table values are correct for single and dual-signature.

SuggestedRemedy
Remove editor`s note.

Response   *Response Status* **C**
ACCEPT.

Cl **33**   *SC* **33.2.4.10**   *P* **72**   *L* **48**   # 104
Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Editorial*
tcc2det_timer definition refers to Table 33-3a, which holds no information about tcc2det.

SuggestedRemedy
Replace reference to Table 33-3a with Table 33-3b.

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 95

EZ

Cl **33**   *SC* **33.2.4.10**   *P* **73**   *L* **13**   # 105
Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Editorial*
tdet2det_timer definition refers to Table 33-3a, which holds no information about tdet2det.

SuggestedRemedy
Replace reference to Table 33-3a with Table 33-3b.

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 95

NonEasy

Cl **33**   *SC* **33.2.4.10**   *P* **73**   *L* **15**   # 156
Johnson, Peter   Sifos Technologies

Comment Type **E**   *Comment Status* **A**   *Editorial*
Error in table reference: ....See Table 33-3a.

SuggestedRemedy
Change to: ... See Table 33-3b.

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 95

NonEasy

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **73**   Page 9 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **15**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.4.10**   *P* **73**   *L* **33**   # 75
Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Editorial*
New text uses LCF to represent long-class-finger. Text on page 132 uses the word "finger." The legacy specification references class "events." Text should use existing terminology.

SuggestedRemedy
Replace all occurrences of LCF with LCE. Replace all occurrences of finger with event.

Response   *Response Status* **C**
ACCEPT.

NonEasy

Cl **33**   *SC* **33.2.4.10**   *P* **73**   *L* **43**   # 209
Yseboodt, Lennart   Philips

Comment Type **TR**   *Comment Status* **D**   *PSE SD*
The timer list for the new SM contains tmpdo_timer, which serves no purpose in the SM. tmpdo_timer_pri and tmpdo_timer_sec supersede it.

SuggestedRemedy
Remove tmpdo_timer from the variable list.

Proposed Response   *Response Status* **Z**
REJECT.

This comment was WITHDRAWN by the commenter.

Tmpdo_timer is used twice in figure 33-10a (page 80, line 41), as well as in figure 33-10e.

Cl **33**   *SC* **33.2.4.11**   *P* **74**   *L* **12**   # 91
Lukacs, Miklos   Silicon Labs

Comment Type **E**   *Comment Status* **A**   *Editorial*
Typo: 'in' is not required.

SuggestedRemedy
This function initiates the Connection Check as specified in ...

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **33**   *SC* **33.2.4.11**   *P* **75**   *L* **33**   # 92
Lukacs, Miklos   Silicon Labs

Comment Type **E**   *Comment Status* **A**   *Editorial*
the indentation of the returned variable "mr_pd_class_detected_ pri" is wrong

SuggestedRemedy
indent similarly like the other variables returned.

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **33**   *SC* **33.2.4.11**   *P* **75**   *L* **40**   # 10
Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **D**   *PSE SD*
Class 5 is missing from mr_pd_class_detected_pri.
Also missing in mr_pd_class_detected_sec on page 76 line 17.

SuggestedRemedy
Add class 5 to the list of values for mr_pd_class_detected_pri and mr_pd_class_detected_sec.

Proposed Response   *Response Status* **Z**
PROPOSED REJECT.

This comment was WITHDRAWN by the commenter.

This is the signature seen during a specific class event (which can only be 0-4). This is not the class of the PD.

Cl **33**   *SC* **33.2.4.11**   *P* **77**   *L* **1**   # 106
Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Editorial*
Stale "or" in definition of set_parameter_type: "…are set to values corresponding to either a Type 1, or Type 2, Type 3, or Type 4 PSE."

SuggestedRemedy
Replace with "Type 1, Type 2, Type 3, or Type 4 PSE."

Response   *Response Status* **C**
ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **77**   Page 10 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **1**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.4.11**   *P* **77**   *L* **4**   # 107

Stover, David   LTC

Comment Type   **E**   *Comment Status* **A**   *Editorial*

Stale "and" in definition of parameter_type: "…to pick between Type 1, and Type 2, Type 3, and Type 4 PI electrical requirement…"

SuggestedRemedy

Replace with "Type 1, Type 2, Type 3, and Type 4 PI electrical requirement…"

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **33.2.4.11**   *P* **77**   *L* **12**   # 108

Stover, David   LTC

Comment Type   **T**   *Comment Status* **A**   *PSE SD*

Agree with editor's note "This paragraph is a Type 2 requirement and does not belong here." A Type 2 PSE will only power a Type 3, 4 PD if that PD is capable of operating as Type 2. No additional guidance on Type 2 PSE behavior is appropriate.

SuggestedRemedy

Strike paragraph beginning with "When a Type 2 PSE powers…" from this section.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Strike the paragraph and the editor's note.

Cl **33**   *SC* **33.2.4.11**   *P* **77**   *L* **52**   # 63

Schindler, Fred   Seen Simply

Comment Type   **TR**   *Comment Status* **D**   *PSE SD*

This section only covers Type 3 and 4 PSEs.

SuggestedRemedy

Replace existing text,
"set_parameter_type
This function is used by a PSE to evaluate the Type of PD connected to the link based on Physical
Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements
defined in Table 33-11 are set to values corresponding to either a Type 1, or Type 2, Type 3, or
Type 4 PSE. This function returns the following variable:

parameter_type: A variable used by a PSE to pick between Type 1, and Type 2, Type 3 and Type 4 PI
electrical requirement parameter values defined in Table 33-11.
Values:
1: Type 1 PSE parameter values (default)
2: Type 2 PSE parameter values
3: Type 3 PSE parameter values
4: Type 4 PSE parameter values
When a Type 2 PSE powers a Type 2, Type 3 or Type 4 PD, the PSE may choose to assign a value of '1' to
parameter_type if mutual identification is not complete (see 33.2.6) and shall assign a value of '2' to
parameter_type if mutual identification is complete."

With,

"set_parameter_type
This function is used by a PSE to evaluate the Type of PD connected to the link based on Physical
Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements
defined in Table 33-11 are set to values corresponding to either a Type 3 or
Type 4 PSE. This function returns the following variable:

parameter_type: A variable used by a PSE to pick between Type 3 and Type 4 PI
electrical requirement parameter values defined in Table 33-11.
Values:
1: Type is not 3 or 4 (default)
2: Type is not 3 or 4
3: Type 3 PSE parameter values
4: Type 4 PSE parameter values
"

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **77**
Li **52**

Page 11 of 55
1/21/2016 1:23:24 PM

Strike the related Editor's Note.

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD, but I believe Type 1 and Type 2 values should still be there…

Cl **33** *SC* **33.2.4.12** *P* **78** *L* **7** # 109

Stover, David   LTC

Comment Type **TR** *Comment Status* **A**   *PSE SD*

The port state machine (Figure 33-10a) should command the pairset state machines to a safe state whenever it leaves PISM_START, including asynchronous exits (e.g., mr_pse_enable changed).

SuggestedRemedy

Add assignment "pism <= false" to port states "TEST_MODE" and "DISABLED".

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **33.2.4.12** *P* **78** *L* **24** # 161

Yseboodt, Lennart   Philips

Comment Type **E** *Comment Status* **A**   *PSE SD*

SM: Fig 33-10a, exit arc from START_CXN_CHX
  Condition: do_cxn_chk_done * (tcc_timer > tcc_min)

Not the usual way to check a timer.
Tcc has a minimum only, it is not a range.
It will evaluate as TRUE whenever the minimum is crossed.

SuggestedRemedy

Change to: do_cxn_chk_done * tcc_timer_done

Response *Response Status* **C**

ACCEPT.

EZ

Cl **33** *SC* **33.2.4.12** *P* **79** *L* **6** # 157

Johnson, Peter   Sifos Technologies

Comment Type **T** *Comment Status* **R**

Figure 33-10a (continued)
The function DETECT_EVAL has logic that sets "start tpon_timer" if not det_temp=1.

What if the signature was invalid ? tpon_timer should not apply.

SuggestedRemedy

Logic in DETECT_EVAL should be extended to include signature validity as a condition of staring the tpon_timer.

Response *Response Status* **C**

REJECT.

I need specific remedies…

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general *Pa* **79** Page 12 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn *Li* **6** 1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.4.12**   *P* **80**   *L* **1**   # 158
Johnson, Peter   Sifos Technologies

Comment Type **T**   *Comment Status* **A**

Figure 33-10a (continued)
There are two general problems that eventually need solutions in this diagram:

1) It appears there is a redundancy is setting alt_pri_pwrd <- TRUE and alt_sec_pwrd <- TRUE in both POWER_UP and POWER_ON. Seems like this should only happen in POWER_UP or under some other condition in POWER_ON.

2) The notion that 4-pair powering turns on both pairsets together if powering 4-pairs is inconsistent with text elsewhere including 33.2.7.1 where it says:
"A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and is in the POWER_ON state may transition between 2-pair and 4-pair power at any time, including after the expiration of Tpon."

SuggestedRemedy

I'm not sure, but I think the POWER_ON (and POWER_UP ?) logic needs to evolve to consider cases where power is not turned on simultaneously to both pairsets. Those cases include:

1) Cases such as described in 33.2.7.1
2) Dual signature powering where some PSE's will power one pairset prior to detection / classification of the other pairset.

This could be editor comment for now.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

State diagram work on power up timing to continue…

No changes to draft result from accepting this comment.

Cl **33**   *SC* **33.2.4.12**   *P* **80**   *L* **5**   # 110
Stover, David   LTC

Comment Type **T**   *Comment Status* **A**   *PSE SD*

Transition logic between CLASS_EVAL and POWER_UP may be reduced with no effect on behavior.

SuggestedRemedy

Replace
((pd_req_pwr < pse_avail_pwr) + ((pd_req_pwr > pse_avail_pwr) * (pse_avail_pwr > 2))) * ted_timer_done
with
((pd_req_pwr < pse_avail_pwr) + (pse_avail_pwr > 2)) * ted_timer_done

Response   *Response Status* **C**

ACCEPT.

Cl **33**   *SC* **33.2.4.12**   *P* **81**   *L* **5**   # 111
Stover, David   LTC

Comment Type **T**   *Comment Status* **A**   *Pres: Stover1*

The possibility exists for alt state machines to loop in perpetuity through detection, power_on and power removal in a staggered fashion, while connection check is never updated.

SuggestedRemedy

See stover_1_0116.pdf

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Work to continue. No changes to the draft result from accepting this comment.

Cl **33**   *SC* **33.2.4.12**   *P* **81**   *L* **32**   # 162
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

Figure 33-10b is titled "Type 3 and Type 4 Alternative B dual-signature pseudo-independent PSE state diagram"

SuggestedRemedy

Change to: "Type 3 and Type 4 Primary Alternative dual-signature <semi>-independent PSE state diagram"

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Editor to change all PISMs to SISMs

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **81**
Li **32**

Page 13 of 55
1/21/2016 1:23:24 PM

Cl **33**   *SC* **33.2.4.12**   *P* **81**   *L* **32**   # 159
Johnson, Peter   Sifos Technologies

Comment Type **E**   *Comment Status* **A**   *Editorial*
Figure 33-10b:

This figure is titled Type 3 ad Type 4 Alternative B dual-signature...

Also, figure 33-10b is continued on 3 pages with different titles but same figure number.

SuggestedRemedy
At a minimum, it needs to be changed to "Alternative A".

More generally, should Figure 33-10b (or whatever figure numbers these become) be titled "Primary Pairset" and "Seconday Pairset" rather than Alternative A and Alternative B ? Seems like this would be more consistent with the content and would not force Primary to be Alterntative A.

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 162

Cl **33**   *SC* **33.2.4.12**   *P* **83**   *L* **33**   # 163
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*
Figure 33-10c is titled "Type 3 and Type 4 Alternative B dual-signature pseudo-independent PSE state diagram"

SuggestedRemedy
Change to: "Type 3 and Type 4 Secondary Alternative dual-signature <semi>-independent PSE state diagram"

Response   *Response Status* **C**
ACCEPT.

Cl **33**   *SC* **33.2.4.12**   *P* **85**   *L* **1**   # 201
Yseboodt, Lennart   Philips

Comment Type **T**   *Comment Status* **A**   *Pres: Yseboodt4*
Autoclass behaviour is still missing from the SD.

SuggestedRemedy
Adopt yseboodt_4_0116_Autoclass_PSE_v100.pdf

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

Adopt pages 3 and 4 of yseboodt_4_0116_Autoclass_PSE_v130.pdf

---

Cl **33**   *SC* **33.2.4.12**   *P* **85**   *L* **4**   # 87
Picard, Jean   Texas Instruments

Comment Type **TR**   *Comment Status* **A**   *Pres: Picard1*
Needs an Updated PSE Classification state diagram (Type 3 and 4) for SS and DS PD.

SuggestedRemedy
See CLASS SD presentation (JP)

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

Adopt picard_02_0116.pdf, picard_03_0116.pdf, picard_04_0116.pdf, picard_05_0116.pdf.

With the changes:
1. removal of values '0' and '5' from class_num_events_pri and class_num_events_sec.
2. remove mention of single event physical layer class from the same variables.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **85**   Page 14 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **4**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.5**   *P* **86**   *L* **45**   # 7

Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **A**   *PSE Power*

"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset, **except as specified in 33.2.7.1**"

The part marked in ** is linked to 33.2.7.1 which is input voltage topic.
The logic to link it to 33.2.7.1 is not clear although we can guess that is related to 33.2.7.1 page 105 lines 16-17 regarding the transition between 2P and 4P.

"A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and is in the POWER_ON state may transition between 2-pair and 4-pair power at any time, including after the expiration of Tpon.

This is unclear to a new reader, and it requires guessing which part of 33.2.7.1 we refer too.

SuggestedRemedy

Group to consider two options.
Option 1:
Change from:
"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset, except as specified in 33.2.7.1"
To:
"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset, except as specified in 33.2.7.1 regarding transition between 2-pair and 4-pair when single-signature PDs operated by Type 3 and Type 4 PSEs"

Option 2 (preferred):
1. Change from:
"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset, except as specified in 33.2.7.1"
To:
"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset, except as specified in 33.2.7.1.1"
2. Move the text in 33.2.7.1 page 105 lines 16-17 to new sub clause 33.2.7.1.1:
"33.2.7.1.1 PSE transition from 2-pair to 4-pair
A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and is in the POWER_ON state may transition between 2-pair and 4-pair power at any time, including after the expiration of Tpon."

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

Change from:
"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset, except as specified in 33.2.7.1"
To:
"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset, except as specified in 33.2.7.1 regarding transitions between 2-pair and 4-pair power."

Cl **33**   *SC* **33.2.5.0a**   *P* **87**   *L* **24**   # 112

Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Editorial*

Mixed precision in Table 33-3b (eg Tcc2det,max = 0.400; Tcc,min = 0.2)

SuggestedRemedy

Replace "0.400" with "0.4" for Tcc2det,max and Tdet2det,max

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

Editor to implement whatever the style guide says is correct.

EZ

Cl **33**   *SC* **33.2.5.0a**   *P* **87**   *L* **28**   # 93

Lukacs, Miklos   Silicon Labs

Comment Type **E**   *Comment Status* **A**   *Editorial*

This comment is about Table 33–3b.
The unit for all parameters is [s].
The precision of the values are not consistent, and 3 digit precision is not needed.

SuggestedRemedy

Use 1 digit precision after the decimal separator for all values (0.4; 0.4; 0.2)

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 112.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **87**
Li **28**

Page 15 of 55
1/21/2016 1:23:24 PM

Cl **33**   *SC* **33.2.5.0a**   *P* **87**   *L* **43**   *#* 8
Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **D**   *Connection Check*

The text says:
"If the voltage on either pairset rises above Vvalid max, (defined in Table 33–4) during connection check, the PSE shall reset the PD by bringing the voltage at the PI below Voff max, defined in Table 33–11 before performing classification."

We asked to work with up to Vvalid_max and to reset at Voltage>Vvalid_max without any gray area.
The reason for reset above Vvalid_max is to prevent that any voltage above Vvalid_max (=10v) will not be interpreted by PD as class event but Vclass is starting at 14.5V at the PD so we can generate gray area of 2V which allows design flexibility.

SuggestedRemedy

Change from:
"If the voltage on either pairset rises above Vvalid max, (defined in Table 33–4) during connection check, the PSE shall reset the PD by bringing the voltage at the PI below Voff max, defined in Table 33–11 before performing classification."
To:
"If the voltage on either pairset rises above Vvalid max to Vvalid max+2V, (Vvalid defined in Table 33–4) during connection check, the PSE shall reset the PD by bringing the voltage at the PI below Voff max, defined in Table 33–11 before performing classification."

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **33**   *SC* **33.2.5.3**   *P* **90**   *L* **5**   *#* 70
Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Editorial*

The existing text,
"A pairset with all of the characteristics specified in Table 33-5 shall be accepted as a valid PD detection signature by a PSE."

should be rewritten to improve clarity.

SuggestedRemedy

Replace the text with,
"A valid PD detection shall occur when a pairset has all of the characteristics specified in Table 33-5."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change to:

"A PSE shall accept as a valid PD signature a pairset with all of the characteristics specified in Table 33-5."

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **90**
Li **5**

Page 16 of 55
1/21/2016 1:23:24 PM

Cl **33**   *SC* **33.2.5.5**   *P* **91**   *L* **15**   # 71

Schindler, Fred   Seen Simply

Comment Type   **ER**   *Comment Status*   **A**   *Editorial*

Changes made to legacy text have made the specification more difficult to understand.

A new 33.2.5.5 indicates,
"If a PSE that is performing detection using Alternative B (see 33.2.3) determines that the impedance at the
PI is greater than Ropen as defined in Table 33-6, it may optionally consider the link to be open circuit and
omit the tdbo_timer interval."

A modified legacy Section 33.2.4.1 p58, indicates,
"A PSE performing detection using only Alternative B may fail to detect a valid PD detection signature.
When this occurs, the PSE shall back off for at least Tdbo as specified in Table 33-11 before attempting
another detection. During this backoff, the PSE shall not apply a voltage greater than VOff to the PI. See
33.2.5.5 for more information on Alternative B detection backoff requirements."

Stricken legacy text immediate follows this,
"If a PSE performs performing detection using Alternative B detects an open circuit (see 33.2.5.5 for more information on detection backoff requirements.) on the link section, then that PSE may optionally omit the detection backoff."

It makes more sense to grouping text, as was previously done in the legacy specification. This also keeps related text on page 58 line 15 to 18 next to the related text above it.

SuggestedRemedy

The Task Force should discuss this and decide where the collected text (page 58 lines 5 to 18) should be placed.

Recommend,
Delete section 33.2.5.5.

Restore stricken text on page 58, lines 11 to 13, with the following adjustments,
"If a PSE performs performing detection using Alternative B detects an open circuit (see Table 33-6) on the link section, then that PSE may optionally omit the detection backoff."

Delete the last sentence of the paragraph on page 58 lines 6 to 9, so that this paragraph reads,
"A PSE performing detection using only Alternative B may fail to detect a valid PD detection signature.
When this occurs, the PSE shall back off for at least Tdbo as specified in Table 33-11 before attempting
another detection. During this backoff, the PSE shall not apply a voltage greater than VOff to the PI."

Response   *Response Status*   **C**

ACCEPT IN PRINCIPLE.

Change text in 33.2.4.1 to:
"A PSE performing detection using only Alternative B may fail to detect a valid PD detection signature.
When this occurs, the PSE shall back off for at least Tdbo as specified in Table 33-11 before attempting
another detection, except in the case of an open circuit as specified in 33.2.5.5. During this backoff, the PSE shall not apply a voltage greater than Voff to the PI."

Cl **33**   *SC* **33.2.5.6**   *P* **91**   *L* **26**   # 72

Schindler, Fred   Seen Simply

Comment Type   **ER**   *Comment Status*   **A**   *Editorial*

Fix Typo "33.2.5.0aa"

SuggestedRemedy

Replace with "33.2.5.0a"

Response   *Response Status*   **C**

ACCEPT.

EZ

Cl **33**   *SC* **33.2.5.6**   *P* **91**   *L* **26**   # 160

Johnson, Peter   Sifos Technologies

Comment Type   **E**   *Comment Status*   **A**   *Editorial*

Typo: ...described in 33.2.5.0aa..

SuggestedRemedy

Remove extra 'a'

Response   *Response Status*   **C**

ACCEPT IN PRINCIPLE.

OBE by 72.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **91**   Page 17 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **26**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.6**   *P* **91**   *L* **29**   # 210

Yseboodt, Lennart   Philips

Comment Type **TR**   *Comment Status* **A**   *Pres: Yseboodt2*

Dual-signature behaviour has been described in an inconsistent manner in 33.2.6, 33.2.7 and the relevant PD sections.

SuggestedRemedy

Adopt yseboodt_2_0116_v4xx.pdf

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adopt yseboodt_2_0116_v421.pdf

Cl **33**   *SC* **33.2.6**   *P* **91**   *L* **48**   # 164

Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

original text: "Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto one or both pairsets and the PD responds to each class event with a current representing one of a limited number of classification signatures."
This text is too compact and the term class event is coming as a surprise. Change it to a real intro to the whole section

SuggestedRemedy

"Physical Layer classification occurs before a PSE supplies power to a PD, when the PSE asserts a voltage in the range of Vclass as defined in Table 33-10 onto one or both pairsets. This is called a class event. The PD responds to each class event with a current representing one of a limited number of classification signatures."

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **33.2.6**   *P* **91**   *L* **50**   # 43

Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **A**   *Pres: Darshan12*

This comment addresses the following topics:
1.33.2.6 and 33.2.7.4 Contains editorial errors.
2.Ipeak text was planned to be with the same concept as Icon text regarding all PD types and Ipeak, Ipeak-2P, Ipeak-2P_unb etc. however, dual-signature PD with the same class and different class was not addressed properly.
3.To update 33.2.6 and 33.2.7.4 per the agreement made in offline discussions that Dual Signature PDs will be responsible to meet Pclass-2P over each pairset.
4.Does DS signature PDs need to meet unbalance requirements i.e:
a)   PSE PI Rpse_min/max?: YES. PD is affected by PSE unbalance and will change Pclass-PD-2P vendor design.
b)   Icon-2P_unb?: No. Pclass-2P is controlled by PD so we need just to meet Icont-2P=Pclass-2P/VPSE.
c)   PD PI unbalance requirements?: No. Pclass-2P is controlled by PD so whatever PD unbalance is, the PD need to handle it or by reducing Pclass-PD so Pclass-PD-2P will meet PD advertised class over that pairset or use current balancing techniques for utilization of maximum power available.

As a result, the working assumptions are:

DS PDs with the same class is a single load PD as well as SS PD does. This means that:
a) PSE PI Rpse_min/max requirements apply for all connected PDs (SS and DS)DS
b) PD PI unbalance (requirements per 33.3.7.10) need to be updated for DS PDs to meet Icon-2P=Pclass-2P/Vpse over each pair set and not Icon-2P_unb. In addition DS PDs and SS PDs will be continue to be tested per the test circuit I n33.3.7.10.
c) DS PDs with different class is treated as DS PDs with the same class which resulted with no differentiation in the spec for DS PD with same class or different class.

SuggestedRemedy

See darshan_012_0116.pdf for proposed remedy.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **91**   Page 18 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **50**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.6**   *P* **92**   *L* **39**   # 9
Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **A**   *Pres: Darshan1*

In order to clarify and simplify the spec we need to define DS PDs requirements per the following guide lines:
1. dual signature PDs shall be designed to have pclass-PD_2P max on each pairset.
1.1 dual signature PDs will be tested to meet (1) with unbalanced PSE and channel according to 33.3.7.10 in order to guarantee that (1) is kept for all operating system (PSE +PD+Channel) conditions.
2. As a result of (1) and (1.1), the dual signature PD with same class and different class will be treated equally and we can use just the term dual-signature PD.
3. The fact that dual signature PD with the same class is also single load and therefore has unbalance issues as the same as single signature PD is resolved by (1) and (1.1).
4. PSE PI unbalance requirements need to be met for all PDs including DS PDs. This will ensure controlled environment to all PDs so the effect of PSE and channel unbalance on the dual signature PD (and single signature PD) will be known to PD designer so he can guarantee Pclass-PD-2P over each pairset.

SuggestedRemedy

Implement darashan_01_0116.pdf.
See also related comments addressing the need to update 33.2.6, 33.2.7.4 and other clauses per the above guidelines.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adopt darashan_01_0116_Rev7.pdf

Cl **33**   *SC* **33.2.6**   *P* **93**   *L* **10**   # 23
Darshan, Yair   Microsemi

Comment Type **T**   *Comment Status* **A**   *Editorial*

Table 33-7 "Assigned Class" column title can be much clearer if it is explained.

SuggestedRemedy

1. Change "Assigned Class" to "Assigned Class^3" to include the footnote number.
2. Add footnote 3 at line 31 below Table 33-7:
"Assigned Class is the actual PD class that is assigned to the PSE based on the operating conditions of Table 33-7.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add:

"Assigned class is the Class that results from the PD requested Class and the number of classification events produced by the PSE as shown in Table 33-7 and Table 33-7a."

to section 33.2.6 where appropriate.

Cl **33**   *SC* **33.2.6**   *P* **93**   *L* **10**   # 16
Darshan, Yair   Microsemi

Comment Type **ER**   *Comment Status* **D**   *Pres: Yseboodt3*

Table 33-7a clarity can be improved by the following actions:

Column "Requested Class ALT A" is actually "PD Requested Class mode A" and "Requested Class ALT B" is actually "PD Requested Class mode B".

SuggestedRemedy

1. Change "Requested Class ALT A" to "PD Requested Class mode A"
2. Change "Requested Class ALT B" to "PD Requested Class mode B".

Proposed Response   *Response Status* **Z**

PROPOSED REJECT.

This comment was WITHDRAWN by the commenter.

WFP

This is the PSE spec. The PSE has alternatives defined, not modes.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **93**   Page 19 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **10**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.6**   *P* **93**   *L* **36**   # 98
Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Pres: Yseboodt3*

Table 33-7a provides details that make the information provided more difficult to understand.

This comment is related to others referenced by COMMENT-3.

SuggestedRemedy

Replace the first table column label "PD Requested Class Alt A" with "ALT Classification". Delete the second table column with header "PD Requested Class Alt B".   Replace the third table column header "Number of PSE Classification Events on Alt A" with "Number of PSE Classification Events". Delete the forth column labeled "Number of PSE Classification Events on Alt B"

Add a note below the table, "Table 33-7a provides data for dual-signature PDs providing the same signature on each PSE Alternative. PSEs classify each Alternative using the same number of classification events."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**   *SC* **33.2.6**   *P* **93**   *L* **36**   # 144
Johnson, Peter   Sifos Technologies

Comment Type **T**   *Comment Status* **A**   *Pres: Yseboodt3*

Table 33-7a, covering Dual Signature mutual ID alternatives, may have a couple of issues:
1) Unlike Table 33-7 above, it does not cover any power demotion cases so it is inconsistent in that way.
2) It makes no allowance for a PSE that might power dual signature PD's independently to avoid multi-event classification when unable to furnish Type-2 power, for example.

SuggestedRemedy

Unless there is a more sweeping alternative to this table to be presented, there should be a comment added to present the above issues.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**   *SC* **33.2.6**   *P* **94**   *L* **1**   # 211
Yseboodt, Lennart   Philips

Comment Type **TR**   *Comment Status* **A**   *Pres: Yseboodt3*

Table 33-7b lists the power classifications for dual-signature PDs.
    - it does not properly show power demotion for all the supported combinations
    - it requires 3 class events in many cases where 1 or 2 is possible as well

SuggestedRemedy

Replace Table 33-7b by yseboodt_3_0116_Table_33_7b_v100.pdf

Response   *Response Status* **C**

ACCEPT.

Cl **33**   *SC* **33.2.6**   *P* **94**   *L* **1**   # 99
Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Pres: Yseboodt3*

Table 33-7a provides details that make the information provided more difficult to understand. The provide solution also reduces duplication of class power levels.

This comment is related to others referenced by COMMENT-3.

SuggestedRemedy

After Table 33-7a, add text (after the note created by related comment-3),
"PSEs provide the ALT Classification power value on each pairset, Pclass-2p, to provide at least the Assigned Class power level."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **94**   Page 20 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **1**   1/21/2016 1:23:24 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.6**   *P* **95**   *L* **4**   # 100

Schindler, Fred   Seen Simply

Comment Type   **ER**   *Comment Status* **D**   *Editorial*

The Task Force needs determine how to eliminate duplicated shall statements. We should use this example to help determine how other duplicates will be handled in subsequent draft reviews.

For example, Table 33-8, replaced legacy Table 33-8, both versions of the table duplicate information already provided in other parts of the specification. Therefore, the shall-statement related to this table located on page 94 is also duplicated.
"A PSE shall meet one of the allowable classification configurations permutations listed in Table 33-8."

For example, on page 95 line 34 duplicates the may allowance for Type-1 PSEs, "A Type 1 PSE may optionally implement Data Link Layer classification."

SuggestedRemedy

A solution is to replace the duplicate requirement on page 95 line 34 with,
 "PSEs meet one of the allowable classification configurations permutations listed in Table 33-8." which makes the Table informative.

A second solution is to,
Delete Table 33-8.

Delete the modified legacy requirement that also affects new Types on page 94,
"A PSE shall meet one of the allowable classification configurations listed in Table 33-8."

Proposed Response   *Response Status*   **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD

Cl **33**   *SC* **33.2.6.2**   *P* **96**   *L* **35**   # 113

Stover, David   LTC

Comment Type   **T**   *Comment Status* **A**   *PSE Class*

"Type 2 PSEs shall provide a maximum of 2 class and 2 mark events. Type 3 PSEs shall provide a maximum of 4 class and 4 mark events. Type 4 PSEs shall provide a maximum of 5 class and 5 mark events."
Maximum allowable class/mark event for Type 3/4 PSEs is dependant upon signature of connected PD, which is not specified here.

SuggestedRemedy

"Type 2 PSEs shall provide a maximum of 2 class and 2 mark events. Type 3 PSEs shall provide a maximum of 4 class and 4 mark events for single-signature PDs and a maximum of 3 class and 3 mark events for dual-signature PDs. Type 4 PSEs shall provide a maximum of 5 class and 5 mark events for single-signature PDs and a maximum of 4 class and 4 mark events for dual-signature PDs."

Response   *Response Status*   **C**

ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **96**   Page 21 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **35**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33** *SC* **33.2.6.2** *P* **96** *L* **39** *#* 73
Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **A** *Editorial*
The text,
"A PSE in the state CLASS_EV1 shall provide to the PI VClass as defined in Table 33-10.
The timing specification shall be as defined by TCLE1 in Table 33-10.

A PSE in the state CLASS_EV1_LCF shall provide to the PI VClass as defined in Table 33-10. The timing specification shall be as defined by TLCF in Table 33-10. The PSE shall measure IClass and classify the PD based on the observed current according to Table 33-9 between 6 ms and 75 ms after transitioning into the state CLASS_EV1_LCF. The PSE may continue to monitor the current past 75 ms. If the PSE did not measure IClass in the range of Class 0 before TACS min and the PSE measures IClass in the range of Class 0 after TACS max this indicates the PD will perform Autoclass. (see 33.3.5.3)."

provides incomplete and incorrect information. It is not clear which PSE Type requirements apply to.

SuggestedRemedy
Replace the referenced text with,

"A PSE in the state CLASS_EV1 shall provide to the PI VClass as defined in Table 33-10.

The timing specification for Type 1 and 2 PSEs shall be as defined by Table 33-10 value TCLE1, and by TLCF for Type 3 or 4 PSEs. The PSE shall measure IClass and classify the PD based on the observed current according to Table 33-9 within Table 33-10 Tpdc. Type 3 and 4 PSEs may continue to monitor the current past Tpdc. If the Type 3 or 4 PSE does not measure IClass in the range of Class 0 before TACS min and the PSE measures IClass in the range of Class 0 after TACS max this indicates the PD will perform Autoclass. (see 33.3.5.3)."

Response *Response Status* **C**
ACCEPT IN PRINCIPLE.

Replace the referenced text with,

"A Type 1 or Type 2 PSE in the state CLASS_EV1 or a Type 3 or Type 4 PSE in the state CLASS_EV1_LCF shall provide to the PI VClass as defined in Table 33-10. The timing specification for Type 1 and 2 PSEs shall be as defined by Table 33-10 value TCLE1, and by TLCF for Type 3 or 4 PSEs. The PSE shall measure Iclass and classify the PD based on the observed current according to Table 33-9 within Table 33-10 Tpdc. Type 3 and 4 PSEs may continue to monitor the current past Tpdc. If the Type 3 or 4 PSE does not measure Iclass in the range of Class 0 before TACS min and the PSE measures Iclass in the range of Class 0 after TACS max this indicates the PD will perform Autoclass. (see 33.3.5.3)."

Cl **33** *SC* **33.2.6.2** *P* **96** *L* **42** *#* 74
Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **A** *Editorial*
Several broken hyperlinks are used for Table 33-10 on lines 42 and 43.

SuggestedRemedy
Use valid hyperlinks.

Response *Response Status* **C**
ACCEPT.

EZ

Cl **33** *SC* **33.2.6.2** *P* **97** *L* **32** *#* 76
Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **A** *Editorial*
The Editor's note may be removed:
"Editor's note: Cleanup of previous paragraph due to bad readability (strikeouts/underlines).
Remove note for D1.5."

SuggestedRemedy
Remove the referenced Editor's note.

Response *Response Status* **C**
ACCEPT.

EZ

Cl **33** *SC* **33.2.6.2** *P* **97** *L* **44** *#* 64
Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **A** *PSE Class*
The text,
"Type 3 and Type 4 PSEs, when connected to single-signature PDs, shall transition directly from CLASS_EV1_LCF to MARK_EV_LAST if they implement only one class event."

Is no longer applicable to Type 4 PSEs.

SuggestedRemedy
Replace the sentence with,
"Type 3 PSEs, when connected to single-signature PDs, shall transition directly from CLASS_EV1_LCF to MARK_EV_LAST if they implement only one class event."

Response *Response Status* **C**
ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **97**
Li **44**

Page 22 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.2.6.2**   *P* **98**   *L* **13**   # **114**
Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Editorial*
"…and transition directly to Mark_EV_LAST if the class…" MARK_EV_LAST is not proper case.

SuggestedRemedy
Replace "Mark_EV_LAST" with "MARK_EV_LAST".

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **33**   *SC* **33.2.6.2**   *P* **98**   *L* **17**   # **145**
Johnson, Peter   Sifos Technologies

Comment Type **T**   *Comment Status* **A**   *Pres: Picard1*
"A Type 3 or Type 4 PSE connected to a dual-signature PD shall skip all subsequent class events and transition directly to MARK_EV_LAST if the class signature detected during CLASS_EV3 is 0, 1, 2 or 4."

1) Has the state machine 'caught up' to this ?
2) What if CLASS_EV3 is 3 because of a dual-signature (dual) Class 3 PD (i.e. signature is 3-3-3) ?

SuggestedRemedy
If this is not in the state machine and is not commented into the state machine during this cycle, an editor's note should be added to address these cases.

Also, is the case of mutual ID for dual signature with Class 3 clear ? What prohibits this PSE from getting 4 events ? Or does it 4 events by design ?

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 87.

Cl **33**   *SC* **33.2.6.2**   *P* **98**   *L* **18**   # **115**
Stover, David   LTC

Comment Type **T**   *Comment Status* **A**   *PSE Class*
"See Annex 33D for an overview of Multiple-Event physical layer classification."
Annex 33D for classification was removed in D1.5, in favor of Table 33-7.

SuggestedRemedy
"See Table 33–7 for an overview of Multiple-Event physical layer classification."

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

Remove sentence.

Cl **33**   *SC* **33.2.6.2**   *P* **98**   *L* **20**   # **165**
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*
Caption of Table 33-9 is "PD classification" while in PSE section.
Also, it used to be that Iclass indicated the PD Class.
With the current classification scheme, this is no longer true.

SuggestedRemedy
Change to: Class signature electrical requirements

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

Change to:

"PD classification signatures"

Cl **33**   *SC* **33.2.6.3**   *P* **100**   *L* **20**   # **166**
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*
Table 33-10a does not describe any electrical parameters but only timing parameters.

SuggestedRemedy
Change header to: Autoclass timing requirements

Response   *Response Status* **C**
ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **100**   Page 23 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **20**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**　　　*SC* **33.2.6.3**　　　　　*P* **100**　　　*L* **47**　　　　# 29
Darshan, Yair　　　　　　　　　Microsemi

Comment Type **E**　　　*Comment Status* **A**　　　　　　　　*Editorial*

Comment 6 from D1.4 was not implemented completely.
"PAutoclass is the measured power during the Autoclass window between TAUTO_PSE2 and TAUTO_PSE2"

Typo in first occurrence of TAUTO_PSE2

SuggestedRemedy

Change from;
"PAutoclass is the measured power during the Autoclass window between TAUTO_PSE2 and TAUTO_PSE2"

To:
"PAutoclass is the measured power during the Autoclass window between TAUTO_PSE1 and TAUTO_PSE2"

Response　　　　　*Response Status* **C**

ACCEPT.

EZ

Cl **33**　　　*SC* **33.2.7**　　　　　*P* **101**　　　*L* **7**　　　　# 52
Schindler, Fred　　　　　　　　Seen Simply

Comment Type **E**　　　*Comment Status* **A**　　　　　　　　*Editorial*

Changed text,
"When the PSE provides power to the PI, it shall conform with Table 33-11. Table 33-11 limit values support operation under worst-case operating conditions."

May be improved.

SuggestedRemedy

Replace the text with,
"When the PSE provides power to the PI, it shall conform with Table 33-11. Table 33-11 values support worst-case operating conditions."

Response　　　　　*Response Status* **C**

ACCEPT.

EZ

Cl **33**　　　*SC* **33.2.7**　　　　　*P* **101**　　　*L* **11**　　　　# 4
Darshan, Yair　　　　　　　　　Microsemi

Comment Type **TR**　　　*Comment Status* **D**　　　　　　　*PSE Power*

In order to control the P2P unbalance effects, it is required that the point of switching and measuring the current will be defined in the negative path for both Type 3/4 PSE and PD and for single port and multiport PSE systems.

SuggestedRemedy

1. Clause 33.2.7 page 101 line 11, Add the following text:
Multiport and Single port Type 3 and 4 PSEs, shall switch their power and measure their currents at least over the more negative power pairs.

2. Clause 33.3.7 page 135 line 7, Add the following text:
Type 3 and 4 PDs, shall switch their power and measure their currents at least over the more negative power pairs.

Proposed Response　　　*Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **101**
Li **11**

Page 24 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.2.7**   *P* **101**   *L* **45**   *#* 24

Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **A**   *Pres: Darshan7*

See darshan_07_0116.pdf for more details.

Is it correct to use Icon-2p_unb_MIN=Icon for Type 3 and 4 operating class 0-4 PDs?
The reason for this question is that it could be per the current spec that the Icon-2P_unb min for class 4 will be greater than Class 5 which may raise confusion and the following analysis meant to explain why it happens for the record and suggest text for clarity.
Analysis:
a) When Type 3 or 4 connected to class 0-4 PDs working over 2P or 4P we may have the following behaviors:
-If working over 2-pairs than Icon-2P_unb_min=Icon=Pclass/Vport = 0.6A for class 4 as an example.
-If working over 4-pairs, the worst case unbalance will cause the current to be only 365mA on the pair with maximum current however per the current spec 0.6A will be the value for this case too ending with situation that class 4 Icon-2P_unb current is greater than class 5. But due to the fact that there are no unbalance requirements for class 0-4 operating over 4-pairs, we have no choice but to use for 2P and 4P operation with class 0-4 PD the same "Icon-2P_unb" min value which is Icon and we need to clarify this in the spec.

The same discussion is apply to ILIM-2P in table 33-11 item 9 which is discussed in separate comment.

SuggestedRemedy

See darshan_07_0116.pdf for more details (the full remedy is shown below).
1.Change Icon to Icon3 in Table 33-11 item 4a Icon-2P_unb minimum value.
2.Add note 3 at the end of table 33-11 with the following text:
"3 For class 4, Icon-2P_unb minimum value may be higher than their minimum values for class 5 due to the fact that class 4 pair-to-pair is not controlled."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

adopt darshan_07_0116_Rev2.pdf

Cl **33**   *SC* **33.2.7**   *P* **102**   *L* **7**   *#* 146

Johnson, Peter   Sifos Technologies

Comment Type **E**   *Comment Status* **A**   *Pres: Darshan2*

Table 33-11, items 5, 5a, and 5c are all labeled "Output current in POWER_UP state".
We could better distinguish from 5b and 5d, and also remove "Additional Information" that says "Total current for both pairsets."

SuggestedRemedy

Label items 5, 5a, and 5c:
Total output current in POWER_UP state.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 33.

Cl **33**   *SC* **33.2.7**   *P* **102**   *L* **10**   *#* 33

Darshan, Yair   Microsemi

Comment Type **E**   *Comment Status* **A**   *Pres: Darshan2*

The following:
a) Table 33-11 item 5-5d and 33.2.7.5
b) Table 33-18 items 5-5d and 33.3.7.3
Can be simplfied.

SuggestedRemedy

See proposal in darshan_02_0116.pdf.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adopt darshan_02_0116_Rev 011j.pdf

With the following changes:
1. remove "same class per pairset" where needed.
2. remove editor's note 1 at top of page 2.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **102**
Li **10**

Page 25 of 55
1/21/2016 1:23:25 PM

Cl **33**　　*SC* **33.2.7**　　　　　*P* **102**　　*L* **47**　　　# **37**

Darshan, Yair　　　　　　　　　Microsemi

Comment Type **ER**　　*Comment Status* **A**　　　　*Editorial*

Table 33-11 item 7, Icon-2P, Type 3,4 additional information column:
There is missing link to 33.2.7.4 that explains what is Icon-2P.

SuggestedRemedy

Add to the additional information column:
"See 33.2.7.4 for Icon-2P details."

Response　　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

add "33.2.7.4" to additional information column.

Cl **33**　　*SC* **33.2.7**　　　　　*P* **103**　　*L* **7**　　　# **26**

Darshan, Yair　　　　　　　　　Microsemi

Comment Type **TR**　　*Comment Status* **A**　　　*Pres: Darshan10*

See darshan_10_0116.pdf.
Table 33-11 item 9, ILIM-2P.
This item was planned to be modified from D1.4 to D1.5 with only editorial changes and better table clarity however some technical changes were made compare to D1.4 and need to be evaluated.

a) There is missing PD class information for PSE Type 1 and 2 rows 1 and 2 in the item number column. In D1.4 it was there. In D1.5 it is missing. (The text in rectangular brackets is not part of the baseline).

b) We can see that class 0-4 with Type 3,4 PSE is 0.68A and class 5 with Type 3,4 PSE is 0.562A which perceived as incorrect in initial review to have class 4 current > class 5 current. If we will run simulations to find ILIM-2P for class 4 when operated over 4pairs we will see that ILIM-2P for class 4 will be 0.410A and not 0.68A. The reason why we can't use the 0.410A value and need to use the 0.684A value is as follows:
We decided that that there are no unbalance requirements for class 4 and below. So if PD class 4 is connected to Type 3 PSE and operates with 4-pairs, the unbalance theoretically may be 100% i.e. all the current flows through one of the pairs. In this case ILIM-2P minimum value will be the same as required for Type 3 PSE connected to class 4 PD operating over 2P which is 0.684A. That is why it could be that ILIM-2P minimum of class 4 will be higher than class 5 (0.562A). Class 5 unbalance is controlled. Class 4 is not.

SuggestedRemedy

Update Table 33-11 item 9 per darshan_10_0116.pdf

Response　　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

Update Table 33-11 item 9 per darshan_10_0116_Rev3.pdf

Cl **33**　　*SC* **33.2.7**　　　　　*P* **103**　　*L* **10**　　　# **97**

Schindler, Fred　　　　　　　　Seen Simply

Comment Type **ER**　　*Comment Status* **A**　　　　*Editorial*

Fix the broken hyperlink on Figure 33-14.

SuggestedRemedy

Fix the broken hyperlink on Figure 33-14.

Response　　　　　　*Response Status* **C**

ACCEPT.

EZ

Cl **33**　　*SC* **33.2.7**　　　　　*P* **103**　　*L* **10**　　　# **116**

Stover, David　　　　　　　　　LTC

Comment Type **E**　　*Comment Status* **A**　　　　*Editorial*

Link to Figure 33-14 is broken in Table 33-11.

SuggestedRemedy

Repair link to Figure 33-14.

Response　　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 97.

Cl **33**　　*SC* **33.2.7**　　　　　*P* **103**　　*L* **11**　　　# **96**

Schindler, Fred　　　　　　　　Seen Simply

Comment Type **ER**　　*Comment Status* **A**　　　*Pres: Darshan10*

Table 33-11, item-9 is for output current during a short circuit, but parameter lists two blank lines and then class ranges. This listing is not clear and contains incomplete information. I also want the Task Force to confirm the unbalance factors used for the current values.

SuggestedRemedy

In the Parameter column for item-9 replace the first parameter blank line with Class 0-3. Replace the second parameter blank line with Class 4.

Class-5 PSEs provide 45W over 4-pairs. This is, 45/50/2 = 450 mA per pairset. The value shown in the table is 1.25x more, which includes 1.05x for the ILIM adjustment and must use 1.19 for unbalance. Is this value of unbalance correct? If not we need to make corrections to Item-9 values.

Response　　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 26

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **103**
Li **11**

Page 26 of 55
1/21/2016 1:23:25 PM

Cl **33** *SC* **33.2.7** *P* **103** *L* **51** # 147

Johnson, Peter   Sifos Technologies

Comment Type **E** *Comment Status* **A**   *Pres: Darshan4*

Sub-heading in Table 33-18, item 17 says:
"DC MPS current to be met on both pairsets".

This could be a tad clearer.

SuggestedRemedy

Change to:

"DC MPS current to be met on each pairset."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Adopt darshan_04_116.pdf with the following change:

Merge 17, 17a, and 17b into item 17.

Cl **33** *SC* **33.2.7** *P* **104** *L* **47** # 42

Darshan, Yair   Microsemi

Comment Type **T** *Comment Status* **A**   *Pres: Darshan6*

Editor Note #2.
"2. The following case needs to be addressed: If PSE is using active or passive pair-to-pair current balancing circuitry, K_Icut may be lower (down to 0.5) per equation TBD."

The accuracy of this comment is addressed in the comment marked ED_2 due to the fact that after D1.4 changes when K_Icut was removed and other terms were used.

The following comment addresses the main issue of Editor Note #2.
1.According the current spec we can implement active or passive current balancing. This is not the issue.
2.According to the current spec if we build active or passive current balancer and we use the limits of Icon-2P_unb, Ipeak-2P_unb and ILIM-2P we will surely be fine. This is not the issue too.
3.The issue is that if we leave that spec as it is, we can't benefit from using active or passive current balancer due to the fact that we are not allowed to use lower limits of Icon-2P_unb, Ipeak-2P_unb and ILIM-2P (that was planned for the worst case unbalance) due to the improved unbalance now. As a result we can't optimize the PSE designs for lower cost as it the only reason for using current balancer.
4.The fact that we can use ILIM, Icon etc. which doesn't include unbalance effect doesn't help to PSEs that wants to have independent Iport-2P measurements and protection over each pairset (this concept of XXX-2P is all over the spec now).

Example: In Type 4 class 8 ILIM-2P min is 0.99A which includes unbalance effect.
Normally PSEs set their ILIM-2P protection to >0.99A per each pairset e.g. 1.08A.
It means that the 2nd pair with the lowest current will have much lower current during normal operation: Iport-2P_other= (90W/52V/2 - (0.925A-90W/52V/2)=0.865A-0.0596A=0.805A :
So if there is a fault at the pair with the pair with the lowest current, the protection on this pairset will happen only when the pair with the lowest current will get to > 1.08A which is a current difference of 1.08A-0.805A=0.275A. This means that the PSE have to be designed to such conditions, it is not a problem to design it as such however we can relax requirements to PSE if PSE is using active or passive current balancer.

SuggestedRemedy

See presentation and proposed Remedy in darshan_06_0116.pdf

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

adoptvdarshan_06_0116.pdf

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **104**   Page 27 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn *Li* **47**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**　　　*SC* **33.2.7**　　　　　*P* **104**　　　*L* **47**　　　# 17
Darshan, Yair　　　　　　　　　Microsemi

Comment Type **ER**　　　*Comment Status* **A**　　　　*Pres: Darshan6*

This comment is marked as ED_2
Editor Note #2.
"2. The following case needs to be addressed: If PSE is using active or passive pair-to-pair
current balancing circuitry, K_Icut may be lower (down to 0.5) per equation TBD."
We made some changes for K_Icut in D1.4 so it is no longer exists.
Instead it should be replaced with new parameter or new description that is related to Icon-
2P, Icon-2P_unb, Ipeak-2P, ILIM-2Pmin.

SuggestedRemedy

Change Editor Note #2 from:
"2. The following case needs to be addressed: If PSE is using active or passive pair-to-pair
current balancing circuitry, K_Icut may be lower (down to 0.5) per equation TBD."
To:
"2. The following case needs to be addressed: If PSE is using active or passive pair-to-pair
current balancing circuitry, Icon-2P_unb, Ipeak-2P, ILIM-2Pmin may be lower per equation
TBD."

Response　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 42

Cl **33**　　　*SC* **33.2.7.1**　　　　*P* **105**　　　*L* **15**　　　# 148
Johnson, Peter　　　　　　　　Sifos Technologies

Comment Type **T**　　　*Comment Status* **D**　　　　*PSE Power*

The final phrase:
"A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and is in
the POWER_ON state may transition between 2-pair and 4-pair power at any time,
including after the expiration of Tpon."

This has no coverage in the state diagram for Type 3/4, at least that I can determine. Also,
does this suggest that the PSE can revert from 4-pair powering to 2-pair powering ?

SuggestedRemedy

Assuming this phrase exists to address 2-pair inrush limiting by some PSE's, we need to
get coverage in state diagram. (editorial note ?)

Secondly, it might be better phrased.

"A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and
powered just one pairset of that PD, may apply power to the other pairset of that PD while
in the POWER_ON state."

Proposed Response　　　*Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general　　　*Pa* **105**　　　Page 28 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn　*Li* **15**　　　1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.7.1**   *P* **105**   *L* **16**   # 46
Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **D**   *PSE Power*

The text:
"A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and is in
the POWER_ON state may transition between 2-pair and 4-pair power at any time,
including after the expiration of Tpon."
is correct also when the PD assigned class is 5-8 and the PD power level at that time is at
any power up to class 4.

SuggestedRemedy

Change the text from:
"A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and is in
the POWER_ON state may transition between 2-pair and 4-pair power at any time,
including after the expiration of Tpon."
To:
"A Type 3 or Type 4 PSE that has assigned Class 1-4 to a single-signature PD and is in
the POWER_ON state may transition between 2-pair and 4-pair power at any time,
including after the expiration of Tpon.
"A Type 3 or Type 4 PSE that has assigned Class 5-8 to a single-signature PD and is in
the POWER_ON state may transition between 2-pair and 4-pair power at any time,
including after the expiration of Tpon only if during the time the PSE is transitioning
between 2-pair and 4-pair power the actual power is below class 4"

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD

Cl **33**   *SC* **33.2.7.4**   *P* **106**   *L* **4**   # 34
Darshan, Yair   Microsemi

Comment Type **E**   *Comment Status* **A**   *Editorial*

"ICon-2P is the current the PSE supports on each pairset and is defined by Equation
Equation (33–3d)."

The word "Equation" apears twice.

SuggestedRemedy

Change from:
"ICon-2P is the current the PSE supports on each pairset and is defined by Equation
Equation (33–3d)."
To:
"ICon-2P is the current the PSE supports on each pairset and is defined by Equation
(33–3d)."

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **33.2.7.4**   *P* **106**   *L* **28**   # 38
Darshan, Yair   Microsemi

Comment Type **ER**   *Comment Status* **A**   *Editorial*

"PClass-2P is PClass-2P as defined in Table 33–11"
Pclass-2P is not defined in Table 33-11. It is defined in Equation 33-3a

SuggestedRemedy

Change from:
"PClass-2P is PClass-2P as defined in Table 33–11"
To:
"PClass-2P is PClass-2P as defined in Equation 33-3a"

Response   *Response Status* **C**

ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **106**   Page 29 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **28**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33** *SC* **33.2.7.4** *P* **106** *L* **41** *#* 31

Darshan, Yair Microsemi

Comment Type **E** *Comment Status* **A** *Editorial*

Typo in.
"VPSE is the voltage at the PSE PI as defined in 1.4.423"

SuggestedRemedy

Change from:
VPSE is the voltage at the PSE PI as defined in 1.4.423
To:
VPSE is the voltage at the PSE PI as defined in 1.4.426

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

All definition references keep changing and need to be kept up to date…

NonEasy

Cl **33** *SC* **33.2.7.4** *P* **107** *L* **26** *#* 11

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **A** *Pres: Yseboodt2*

The text:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a single-signature PD, shall be able to source......."

Applies to dual signature PDs with the same class too.
This is the same concept used for Icon, Icon-2P and Icon-2P_unb in pages 105-106.

SuggestedRemedy

Change from:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a single-signature PD, shall be able to source......."
To:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a single-signature PD or dual-signature PD that advertise the same class signature on each pairset, shall be able to source......."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33** *SC* **33.2.7.4** *P* **107** *L* **27** *#* 28

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **A** *Pres: Yseboodt2*

"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a single-signature PD, shall be able to source IPeak , IPeak-2P , and IPeak-2P_unb as specified in Table 33–11 and Equation (33–4d)."

IPeak , IPeak-2P , and IPeak-2P_unb are not defined in Table 33-11. They are defined in pages 106 and 107.

SuggestedRemedy

Change:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a single-signature PD, shall be able to source IPeak , IPeak-2P , and IPeak-2P_unb as specified in Table 33–11 and Equation (33–4d)."
To:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a single-signature PD, shall be able to source IPeak , IPeak-2P , and IPeak-2P_unb as specified in Equation (33–4d)."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33** *SC* **33.2.7.4** *P* **107** *L* **27** *#* 39

Darshan, Yair Microsemi

Comment Type **ER** *Comment Status* **A** *Pres: Yseboodt2*

The text "Icon-2P is the current.."
Is wrong. It should be Ipeak-2P.

SuggestedRemedy

Change from:
"Icon-2P is the current.."
To:
"Ipeak-2P is the current.."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general *Pa* **107** Page 30 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn *Li* **27** 1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**　　*SC* **33.2.7.4**　　　　　*P* **107**　　*L* **38**　　# 20
Darshan, Yair　　　　　　　　　Microsemi

Comment Type **ER**　　*Comment Status* **A**　　　　*Pres: Yseboodt2*
The text:
"IPort-2P-other is the output current on the other pairset (see 33.2.4.4 (XREF))"

The reference should be 33.2.4.9.

SuggestedRemedy
Change to 33.2.4.9.

Response　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**　　*SC* **33.2.7.4**　　　　　*P* **107**　　*L* **42**　　# 12
Darshan, Yair　　　　　　　　　Microsemi

Comment Type **TR**　　*Comment Status* **A**　　　　*Pres: Yseboodt2*
The text:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a dual-signature PD, shall be able to source Ipeak-2P on each pairset......."

Applies to dual signature PDs with different class and not just dual-signature PD. This is the same concept used for Icon-2P in pages 105-106.

SuggestedRemedy
Change from:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a dual-signature PD, shall be able to source Ipeak-2P on each pairset......."
To:
"Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a dual-signature PD that advertised a different class signature on each pairset, shall be able to source Ipeak-2P on each pairset......."

Response　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**　　*SC* **33.2.7.4**　　　　　*P* **107**　　*L* **54**　　# 59
Schindler, Fred　　　　　　　　Seen Simply

Comment Type **ER**　　*Comment Status* **A**　　　　*Editorial*
Fix the broken hyperlink on "Table 33-11".

SuggestedRemedy
Fix the broken hyperlink on "Table 33-11".

Response　　　　　*Response Status* **C**
ACCEPT.

EZ

Cl **33**　　*SC* **33.2.7.4**　　　　　*P* **108**　　*L* **1**　　# 25
Darshan, Yair　　　　　　　　　Microsemi

Comment Type **TR**　　*Comment Status* **A**　　　　*Pres: Yseboodt2*
Ppeak_PD-2P is not defined in table 33-18.
Actually Ppeak_PD-2P in equation 33-4e is not defined.
It was defined in previous drafts as 0.5*Ppeak_PD while Ppeak_PD is defined in Table 33-18.

SuggestedRemedy
Change from:
"PPeak_PD-2P is the total peak power a PD may draw for its Class on a pairset; see Table 33–18"
To:
PPeak_PD-2P is the total peak power a PD may draw for its Class on a pairset and is defined as 0.5*Ppeak_PD. Ppeak_PD is defined in Table 33–18.

Response　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 210

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Cl **33**   *SC* **33.2.7.5**   *P* **109**   *L* **12**   *#* 86
Picard, Jean   Texas Instruments

Comment Type **TR**   *Comment Status* **A**

"Type 3 and Type 4 PSEs that apply power to both pairsets when connected to a
single-signature PD shall reach the POWER_ON state on both pairsets within TInrush-2P
max, starting with
the first pairset transitioning into the POWER_UP state."

Need to clearly state that both pairset do not necessarily have to turn on at same time, with
the exception of Type 4 having allocated Class 7-8 power.

SuggestedRemedy

Insert the following sentence after the paragraph:

"The second pairset may transition to POWER_UP within Tinrush-2P min."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Insert

"The second pairset may transition to POWER_UP anytime within this time period."

after the commented sentence.

Cl **33**   *SC* **33.2.7.5**   *P* **110**   *L* **5**   *#* 36
Darshan, Yair   Microsemi

Comment Type **ER**   *Comment Status* **A**   *Pres: Darshan3*

Figure 33-13:
a) Y axis lable Iport-2P is too close to the Y axis end point.
b) Iinrush-2P_max is too close to the Y axis.
c) The lable "Iinrush-2P at Vpse-2P>30V" need to include now Iinrush as well.

SuggestedRemedy

Make the above suggested editing.
See darshan_03_0116.pdf for details.

Response   *Response Status* **C**

ACCEPT.

Cl **33**   *SC* **33.2.7.7**   *P* **111**   *L* **27**   *#* 3
Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **D**   *PSE Power*

Referring to the text:
"When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove
power from both pairsets before the current exceeds the "PSE upperbound template" on
either pairset."
Due to the fact that we normally have addressed the requirements per pairset in order to
protect each pairset and we already cover the pairset protection in the previous lines 25-26:
"Power shall be removed from a pairset PI of a PSE before the pairset PI current exceeds
the "PSE upperbound template" in Figure 33-14, Figure 33-14a, and Figure 33-14b."
So in single signature PD if current over a pairset approaches the upper bound template
and as a result power is removed from that pairset, the whole current will flow through the
remaining pairset and it will be disconnected as well, so there is no need for the redundant
text in line 27.

SuggestedRemedy

Delete:
"When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove
power from both pairsets before the current exceeds the "PSE upperbound template"

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD

Cl **33**   *SC* **33.2.7.7**   *P* **111**   *L* **27**   *#* 167
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

single signature <= missing hyphen

SuggestedRemedy

Change to single-signature

Response   *Response Status* **C**

ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **111**
Li **27**

Page 32 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.2.7.6**   *P* **111**   *L* **30**   # 77

Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Pres: Yseboodt2*

Figures 33-14, 14a, 14b, and 14c, are missing one or more axis labels.

SuggestedRemedy

Add Iport-2P to y-axis of Figure 33-14, and time for the x-axis for all referenced figures.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**   *SC* **33.2.7.7**   *P* **111**   *L* **31**   # 117

Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Pres: Yseboodt2*

The top of new Figure 33-14 (I_port-2p and "8.2ms") has been cropped from new Figure 33-14.

SuggestedRemedy

Repair Figure 33-14 to include top portion.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**   *SC* **33.2.7.7**   *P* **111**   *L* **31**   # 118

Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Editorial*

10µs and 8.2ms are related values, pertaining only to upperbound template, and so could benefit from living on the same axis.

SuggestedRemedy

Move "10µs" to same axis as "8.2ms" in all Figure 33-14 variants.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Need to merge with any changes from Yseboodt2

Cl **33**   *SC* **33.2.7.6**   *P* **112**   *L* **41**   # 103

Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **A**   *Pres: Yseboodt2*

I am not able to parse this section in a reasonable amount of time. I see too much duplication that exists for no apparent reason. Comments already provided attempt to improve this section but continued review shows even more issues. For example, Figures 33-14b and 33-14c have the same titles, which is an error.

Figure 33-14b prevents operational modes that are important to architectures providing control of both pairsets. Figures also permit more power than is intended for compliant PD devices.

SuggestedRemedy

Correct typo in Figure-33-14c title by replacing "Type 3" with "Type 4". This is supported by text on page 111 lines 18 to 22.

Add Editor's note:
"Task Force members are encouraged to review this section to improve clarity. Figures may prevent operational modes PSEs with pairset control require. Figures also permit more power than is intended for compliant PD devices."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add Editor's note:
"Task Force members are encouraged to review this section to improve clarity. Figures may prevent operational modes PSEs with pairset control require. Figures also permit more power than is intended for compliant PD devices."

Cl **33**   *SC* **33.2.7.7**   *P* **113**   *L* **23**   # 119

Stover, David   LTC

Comment Type **E**   *Comment Status* **A**   *Pres: Yseboodt2*

Figures 33-14b and 33-14c have identical caption text. As per 33.2.7.7 paragraph 1, 33-14c should reference Type 4 PSEs.

SuggestedRemedy

In Figure 33-14c caption, replace "Type 3" with "Type 4"

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 210

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **113**
Li **23**

Page 33 of 55
1/21/2016 1:23:25 PM

Cl **33**　　　*SC* **33.2.7.7**　　　　　*P* **114**　　　*L* **7**　　　　# 120
Stover, David　　　　　　　　　　　LTC

Comment Type **E**　　　*Comment Status* **A**　　　　　*Pres: Yseboodt2*
I_TBDNAME was not updated to I_LPS. This is the only occurrence of I_TBDNAME.

SuggestedRemedy
Replace I_TBDNAME with I_LPS.

Response　　　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**　　　*SC* **333.2.7.6**　　　　*P* **114**　　　*L* **26**　　　# 53
Schindler, Fred　　　　　　　　　Seen Simply

Comment Type **E**　　　*Comment Status* **A**　　　　　*Pres: Yseboodt2*
Formulas 33-7, 33-7a, 33-7b, and 33-7c are identical and should be replaced by one formula.

SuggestedRemedy
Delete formulas 33-7a, 33-7b, and 33-7c.

Replace references to the deleted formulas so that they point to formula 33-7. The corrected references are on page 111.

Response　　　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 210

Cl **33**　　　*SC* **33.2.7.12**　　　　*P* **116**　　　*L* **31**　　　# 121
Stover, David　　　　　　　　　　　LTC

Comment Type **E**　　　*Comment Status* **A**　　　　　*Editorial*
I_Port-2P-other definition points to T1/T2 SD variables section. Should point to T3/T4 SD variables.

SuggestedRemedy
Replace description of I_Port-2P-other with "is the output current on the other pairset (see 33.2.4.9)"

Response　　　　　　　*Response Status* **C**
ACCEPT.

EZ

Cl **33**　　　*SC* **33.2.8**　　　　　*P* **117**　　　*L* **4**　　　　# 200
Yseboodt, Lennart　　　　　　　　Philips

Comment Type **ER**　　　*Comment Status* **A**　　　　　*PSE Power*
original text: "A PSE shall not initiate power provision to a link if a PD would not be able to ascertain the available amount of power based on the number of classification events produced by the PSE."

Unless a reader already fully understands the intricacies of power demotion,this might have well been written in Klingon.

SuggestedRemedy
Better & shorter:
"A PSE shall not provide power to a Class 0 to 3 PD, unless the PSE can supply the requested Class of that PD."

Response　　　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

"A PSE shall not initiate power provision to a link or a pairset if the connected PD is not able to ascertain the available power based on the number of classification events produced by the PSE.

For example, a PSE that has less than Class 3 power would not provision power to the link or pairset for a PD requesting a Class 3 or higher power level."

"A PSE shall not provide power to a single-signature Class 0 to 3 PD, unless the PSE can supply the requested power of that PD."

Cl **33**　　　*SC* **33.2.9.1.2**　　　*P* **119**　　　*L* **22**　　　# 125
Stewart, Heath　　　　　　　　　LTC

Comment Type **T**　　　*Comment Status* **A**　　　　　*Pres: Stewart1*
DC MPS requirements are unclear.

SuggestedRemedy
See stewart_1_0116.pdf

Response　　　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

Adopt hstewart_01_0116_baseline_v6.pdf

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **119**
Li **22**

Page 34 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.3.1**   *P* **120**   *L* **40**   # 65
Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **D**   *PD Power*

The existing sentence,
"PDs that are not implemented to be insensitive to polarity, are specifically not allowed by this standard."

provides an incomplete requirement.

SuggestedRemedy

Add the additional requirement after the referenced sentence that clarifies what insensitive means,
"PDs shall have the same capabilities when powered using either polarity."

Proposed Response   *Response Status* **Z**
REJECT.

This comment was WITHDRAWN by the commenter.

TFTD

See 78, 174

Cl **33**   *SC* **33.3.1**   *P* **120**   *L* **40**   # 78
Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **R**   *PD Power*

The existing sentence,
"PDs that are not implemented to be insensitive to polarity, are specifically not allowed by this standard."

Should be reworded to indicate what is required.

SuggestedRemedy

Replace the sentence with,
"PDs shall be insensitive to polarity of the applied voltage."

Response   *Response Status* **C**
REJECT.

Cl **33**   *SC* **33.3.1**   *P* **120**   *L* **40**   # 174
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *PD Power*

original text: "PDs that are not implemented to be insensitive to polarity, are specifically not allowed by this standard."

Remove triple negation for clarity

SuggestedRemedy

"PDs that are sensitive to polarity, are specifically not allowed by this standard."

Response   *Response Status* **C**
ACCEPT.

Cl **33**   *SC* **33.3.1**   *P* **120**   *L* **46**   # 66
Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **R**   *PD Power*

Existing text,
"The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage."

is not correct and should be removed. For example, page 99 provides an Editor's note, "Editor's note: Need to perform thermal analysis on new classification timings/events on both existing and new", which shows concern that PD may not accept a classification voltage indefinitely. It is also clear that providing 57V across MDI pins connected to Ethernet transformers should not be allowed. The original meaning of this sentence is no longer clear and the Task Force has not been able to find acceptable text.

SuggestedRemedy

Delete the sentence.

Response   *Response Status* **C**
REJECT.

It is my understanding that this requirement was originally included to make sure PDs can handle being stuck in class indefinitely without permanent damage. That should still be a requirement.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **120**   Page 35 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **46**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.3.2**   *P* **121**   *L* **32**   # 49
Bennett, Ken   Sifos Technologies, In

Comment Type **ER**   *Comment Status* **R**   *PD Class*

The text states: "Editor's Note: Classification section to be updated to move all Type 3 and Type 4 PSEs to multiple-event (Mark is considered an event)."

Legacy text has taught readers that when the word "Event" is followed by "Classification", the count is equal to the number of class pulses. In 802.3bt, it is being redefined to include a single-event classification (Class-Mark) as > 1. This is likely to confuse readers.

802.3bt text updates have been, and will continue to be, complicated by this. Consistency in this definition involves changes to be made to (at least) Tables 33-1a, 33-8, 33-15a, and several text references. The tables have rows that separate type 3 single-event and Multiple-event classifications, so the change isn't simple.

The suggested remedy is one possible option for a naming change.

SuggestedRemedy

Change "Multiple-Event classification" to "Marked-Event classification".
(Terms like "Single Marked-Event" or # Marked Events could then be used.)

Response   *Response Status* **C**
REJECT.

The mark events are actually called events.

Cl **33**   *SC* **33.3.2**   *P* **121**   *L* **46**   # 122
Stover, David   LTC

Comment Type **TR**   *Comment Status* **A**   *PD Class*

"Such Type 3 PDs advertise a class signature of 4, 5, or 6, while Type 4 PDs advertise a class signature of 7 or 8." 5, 6, 7, and 8 are Class results, not class signatures. A proper example of usage may be found on page 122, line 1.

SuggestedRemedy

"Such Type 3 PDs advertise Class 4, 5, or 6, while Type 4 PDs advertise Class 7 or 8."

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **33**   *SC* **33.3.2**   *P* **121**   *L* **51**   # 123
Stover, David   LTC

Comment Type **TR**   *Comment Status* **A**   *PD Class*

"Type 3 dual-signature PDs advertise a class signature of 1, 2, 3, or 4 on each pairset, while Type 4 dual-signature PDs advertise a class signature of 5 on at least one pairset." Paragraph refers to class signature rather than Class result, which is clearly the intent.

SuggestedRemedy

"Type 3 dual-signature PDs advertise Class 1, 2, 3, or 4 on each pairset, while Type 4 dual-signature PDs advertise Class 5 on at least one pairset."

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **33**   *SC* **33.3.3.5**   *P* **126**   *L* **1**   # 202
Yseboodt, Lennart   Philips

Comment Type **T**   *Comment Status* **A**   *Pres: Yseboodt5*

Autoclass is still missing from the PD SD.

SuggestedRemedy

Adopt yseboodt_5_0116_Autoclass_PD_v100.pdf

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

Adopt pages 1 and 2 of yseboodt_5_0116_Autoclass_PD_v100.pdf

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **126**   Page 36 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **1**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**　　*SC* **33.3.3.5**　　　　　*P* **126**　　*L* **1**　　　# 191
Yseboodt, Lennart　　　　　　　Philips

Comment Type **ER**　　*Comment Status* **A**　　　　*Editorial*
The D1.5 state machine is still drawn in draw.io format.
　　　yseboodt_8_0116_PD_SM.pdf is a redrawn version in Visio.
　　　It is identical in every way, except I've placed the states a bit different to get a
better layout.

SuggestedRemedy
Adopt yseboodt_8_0116_PD_SM.pdf
　　　In case any deviation is found between yseboodt_8_0116_PD_SM.pdf and the
D1.5 SM, the D1.5SM is leading.
　　　Other comments against the SM to be executed on
yseboodt_8_0116_PD_SM.pdf

Response　　　　　*Response Status* **C**
ACCEPT.

EZ

Cl **33**　　*SC* **33.3.3.5**　　　　　*P* **126**　　*L* **4**　　　# 212
Yseboodt, Lennart　　　　　　　Philips

Comment Type **TR**　　*Comment Status* **A**　　　　*PD SD*
Entry arc into IDLE uses variable V_Reset which isn`t listed in the constants section.
　　　Note: this is wrong in 802.3-2012 as well.

SuggestedRemedy
Add:
　　　"V_Reset　　Reset voltage (see Table 33-17)"
　　　to 33.3.3.2

Response　　　　　*Response Status* **C**
ACCEPT.

NonEasy

Cl **33**　　*SC* **33.3.3.5**　　　　　*P* **126**　　*L* **4**　　　# 213
Yseboodt, Lennart　　　　　　　Philips

Comment Type **TR**　　*Comment Status* **A**　　　　*Pres: Yseboodt7*
PD state machine global entry arc into IDLE has following condition:
　　　[(Vpd < Vreset) + !power_received] * mdi_power_required * !pd_reset

　　　The effect is that at ANY voltage below Vport_pd min, this condition will apply
and reset the state machine to IDLE.
　　　The intent is to allow a global override to reset the SM to IDLE when the PI
voltage drops below Vreset.

SuggestedRemedy
Replace condition by:
　　　(Vpd < Vreset) * mdi_power_required * !pd_reset
　　　See yseboodt_7_0116_idlestuck.pdf

Response　　　　　*Response Status* **C**
ACCEPT IN PRINCIPLE.

Please file a maintenance request.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **126**
Li **4**

Page 37 of 55
1/21/2016 1:23:25 PM

Cl **33**　　*SC* **33.3.5**　　　　*P* **130**　　*L* **11**　　　# 67

Schindler, Fred　　　　　　　Seen Simply

Comment Type **TR**　　*Comment Status* **A**　　　　*PD Class*

Added Table 33-15a replaced Table 33-8 to improve readability and remove PSE information. The new table consumes most of the page while not providing significant information. It takes some readers too much time to comprehend the table.

This comment is related to others marked COMMENT-2.   The resolution of this comment provides two solutions, one that provides a translation of the table and a preferred one that translates the table AND corrects an error covered in COMMENT-2.

SuggestedRemedy

PREFERRED:
Delete the requirement on line 4 that references Table 33-15a. Replace this sentence with, "All PDs shall provide physical layer classification. Type-1 PDs optionally provides DLL classification (see 33.6) while Type-2, Type-3 and Type-4 PDs shall provide DLL classification. "

Delete Table 33-15a and its footnote.

TRANSLATION:
Delete the requirement on line 4 that references Table 33-15a. Replace this sentence with, "All PDs shall provide physical layer classification. Type-1 PDs optionally provides DLL classification (see 33.6) while Type-2, Type-3 and Type-4 PDs shall provide DLL classification.   DLL classification may be omitted by Type 3 or Type-4 Single-signature PDs not capable of drawing more than Class 3 power levels."

Delete Table 33-15a and its footnote.

Response　　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

I thought we all agreed that DLL is not required for class 0-3.

Delete the requirement on line 4 that references Table 33-15a and the table.

Replace this sentence with,

"All PDs shall provide physical layer classification. Type 1 PDs and Class 1-3 Type 3 PDs optionally provide DLL classification (see 33.6) while Type 2 PDs, Class 4-6 Type 3 PDs, and Type 4 PDs shall provide DLL classification. "

Cl **33**　　*SC* **33.3.5**　　　　*P* **130**　　*L* **37**　　　# 60

Schindler, Fred　　　　　　　Seen Simply

Comment Type **TR**　　*Comment Status* **D**　　　　*PD Class*

"Single-signature PDs not capable of drawing more than Class 3 power levels may omit Data Link Layer
classification (see 33.6)."

Is a stealth way to permit new PDs to omit DLL, which is not a goal of this standard. Type 3 and 4 PDs are required to provide DLL support.

This comment is related to others marked COMMENT-2.

SuggestedRemedy

Strike footnote-1

Proposed Response　　　*Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

See 67

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **130**
Li **37**

Page 38 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.3.5**   *P* **130**   *L* **41**   # 61

Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **D**   *PD Class*

Existing text,
"Type 2, Type 3, and Type 4 PDs at Class 4 or greater power levels shall implement both Multiple-Event
class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6)."

Is a stealth way to permit new PDs to omit DLL, which is not a goal of this standard. Type 3 and 4 PDs are required to provide DLL support. The legacy sentence modified to accomplish this appears to have been,
"Type 2 PDs implement both 2-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6)."

This comment is related to others marked COMMENT-2.

SuggestedRemedy

Replace the reference sentence with,
"Type 2, Type 3, and Type 4 PDs shall implement both Multiple-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6)."

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

See 67.

Cl **33**   *SC* **33.3.5.1**   *P* **131**   *L* **4**   # 88

Lukacs, Miklos   Silicon Labs

Comment Type **ER**   *Comment Status* **R**   *PD Class*

class_sig_B is left out from the first sentence.

SuggestedRemedy

"PDs implementing a Multiple-Event class signature shall return class_sig_A and class_sig_B in accordance with..."

Response   *Response Status* **C**

REJECT.

This sentence is in the single-event classification section. Thus, only class_sig_A applies.

Cl **33**   *SC* **33.3.5.1**   *P* **131**   *L* **17**   # 94

Lukacs, Miklos   Silicon Labs

Comment Type **E**   *Comment Status* **D**   *PD Class*

This text is nto clear enough:
"Type 1 and Type 2 PDs shall present one, and only one, classification signature during classification."

SuggestedRemedy

Type 1 and Type 2 PDs shall present one, and only one, classification signature during the whole (all events of the) classification.

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Better language is welcome….

Cl **33**   *SC* **33.3.5.2**   *P* **132**   *L* **46**   # 79

Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Pres: Yseboodt2*

The existing text,
"It is not recommended to use different class signatures if the dual-signature PD powers a single electrical load."

should be rewritten to show preference.

SuggestedRemedy

Replace the referenced text with,
"Dual-signature PDs with a single electrical load should use the same class signature."

Or use,
"It is recommended that Dual-signature PDs with a single electrical load use the same class signature."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

"It is recommended that Dual-signature PDs with a single electrical load use the same class signature."

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **132**   Page 39 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **46**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**　　*SC* **33.3.7**　　　　　*P* **135**　　*L* **18**　　　# 15

Darshan, Yair　　　　　　　　Microsemi

Comment Type **ER**　　*Comment Status* **A**　　　　*Editorial*

Table 33-18 item 1 parameter name:
"Input voltage per pairset."
It should be DC voltage.

SuggestedRemedy

Change from:
"Input voltage per pairset"
To:
"Input DC voltage per pairset

Response　　　　　*Response Status* **C**

ACCEPT.

Cl **33**　　*SC* **33.3.7**　　　　　*P* **137**　　*L* **6**　　　# 40

Darshan, Yair　　　　　　　　Microsemi

Comment Type **ER**　　*Comment Status* **D**　　　　*Editorial*

Table 33-18 item 7 parameter name "Peak operating power" need to be "Total peak operating power"

SuggestedRemedy

Change Table 33-18 item 7 parameter name "Peak operating power"
to:
"Total peak operating power"

Proposed Response　　　*Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

We don't call item 4 Total Input average power (we just say "Input average power").

We should be consistant.

Cl **33**　　*SC* **33.3.7**　　　　　*P* **137**　　*L* **30**　　　# 18

Darshan, Yair　　　　　　　　Microsemi

Comment Type **ER**　　*Comment Status* **A**　　　　*PD Power*

Table 33-18 items 11 and 12 (PD power supply turn on voltage, PD power supply turn off voltage, and PD classification stability time need to be per pairset.

SuggestedRemedy

Add to each parameter name of items 11 and 12: "per pairset"

Response　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

Add to line 51 in 33.3.7.1
"For dual-signature PDs the requirements for Von and Voff apply to each pairset individually."

Cl **33**　　*SC* **33.3.7.1**　　　　*P* **137**　　*L* **53**　　　# 62

Schindler, Fred　　　　　　　Seen Simply

Comment Type **TR**　　*Comment Status* **A**　　　　*PD Power*

A"The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by VPort_PSE-2P min to VPort_PSE-2P max (as defined in Table 33-11) with a series resistance within the range of valid Channel Resistance."

The "valid Channel Resistance", covers the entire range of channel resistance values was restricted to Rch, which is the worst-case channel resistance. The standard provides interoperability for PSE that operate over a range of values not one specific value.

SuggestedRemedy

Restore the legacy text.

Response　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

Replace with:
"...with a series resistance less than or equal to RCh".

"valid Channel Resistance" is not defined anywhere.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general　　　　*Pa* **137**　　Page 40 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn　*Li* **53**　　1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.3.7.3**   *P* **138**   *L* **41**   # 30
Darshan, Yair   Microsemi

Comment Type **E**   *Comment Status* **A**   *Editorial*

Typo in the text regarding Table reference number since D1.3:
"Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with Vport_PD-2P requirements as defined in Table **33–16a**,..."

It should be Table 33-18

SuggestedRemedy

Change to:
"Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with Vport_PD-2P requirements as defined in Table 33–18,..."

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **33.3.7.3**   *P* **138**   *L* **42**   # 27
Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **D**   *Pres: Darshan2*

Does the requirement to finish Iirush within Tinrus-2P min is only if PSE is incharge of controlling Iinrus i.e. Cpd<=180uF and if PD is limiting Iinrush than there is no Tinrush_max requirement for the PD?
This interpretation makes sense to me since it fits the original intention to support Cport>180uF so time is not a concern.
If this is correct than it is not clear from clause 33.3.7.3

SuggestedRemedy

To be discussed by the group.

Proposed Response   *Response Status* **Z**
REJECT.

This comment was WITHDRAWN by the commenter.

TFTD

Cl **33**   *SC* **33.3.7.3**   *P* **138**   *L* **42**   # 84
Picard, Jean   Texas Instruments

Comment Type **TR**   *Comment Status* **A**   *PD Inrush*

"... CPort has reached a steady state and is charged to 99% of its final value. This period shall be less than TInrush-2P min per Table 33–11."

For more clarity, a link to the PSE inrush section is needed.

SuggestedRemedy

"… Cport has reached a steady state and is charged to 99% of its final value. This period shall be less than Tinrush-2P min per Table 33–11, with the PSE minimum inrush behavior defined in 33.2.7.5 a, b, and c."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

"... CPort has reached a steady state and is charged to 99% of its final value. This period shall be less than TInrush-2P min per Table 33–11, with the PSE minimum inrush behavior defined in 33.2.7.5."

Cl **33**   *SC* **33.3.7.3**   *P* **138**   *L* **43**   # 85
Picard, Jean   Texas Instruments

Comment Type **TR**   *Comment Status* **A**   *Pres: Darshan2*

"All PDs shall consume a maximum of Class 3 power for at least Tdelay-2P min."

Referring to Class 3 is misleading and incorrect. What we want to say is a type 2 or 3 PD must ensure that regardless of its load power consumption, its capacitor must be charged within Tinrush-2P min, while not drawing more than 400 mA total (capacitor recharge + load power). We also want to apply this rule to type 4 PD when connected to Type 1, 2 or 3 PSE.

SuggestedRemedy

Remedy:
"Single signature PDs with assigned class 0-6 shall behave like a Type 1 PD for at least Tdelay min."

Response   *Response Status* **C**
ACCEPT IN PRINCIPLE.

OBE by 33.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **138**   Page 41 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **43**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.3.7.3**   *P* **139**   *L* **26**   # 32

Darshan, Yair   Microsemi

Comment Type **E**   *Comment Status* **A**   *Editorial*

Figure 33-17a
Change "PSE encounters Cx" to "PSE sees Cx".

SuggestedRemedy

Change from:
"PSE encounters ..."
to:
"PSE sees ..." in Figure 33-17a.
4 occurrences.

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **33.3.7.3**   *P* **139**   *L* **42**   # 19

Darshan, Yair   Microsemi

Comment Type **ER**   *Comment Status* **A**   *PD Power*

Figure 33-17a.
The original intent for the Dual Signature PD drawing is that its Cport can be 2xCx if it is isolated and Cport=2*Cx (or <=2*Cx) when it is not isolated.
Currently the drawing shows isolated so the label need to be Cport=2*Cx and not Cport<=2*Cx.

SuggestedRemedy

Change line 42 in Figure 33-17a from:
Cport<=2*Cx.
To:
Cport=2*Cx.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Make bottom drawing of 33-17a have a Cx and a Cy and change to Cport = Cx + Cy.

Cl **33**   *SC* **33.3.7.4**   *P* **140**   *L* **2**   # 102

Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **A**   *PD Power*

Legacy text "Peak operating power shall not exceed PPeak max." provides a requirement that affects all Types. The value Ppeak is not defined or used in the specification. This appears to be a typo. I suspect the intended requirement is covered by requirements related to Ppeak_PD.

SuggestedRemedy

I recommend striking the line on p140 ,
"Peak operating power shall not exceed PPeak max." because it has no meaning.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change Ppeak to Ppeak_PD.

Cl **33**   *SC* **33.3.7.4**   *P* **140**   *L* **7**   # 50

Bennett, Ken   Sifos Technologies, In

Comment Type **ER**   *Comment Status* **R**   *PD Power*

Line 7 through 49, which discusses PD Iport limits for current that includes AC ripple, appears to be redundant and adds unnecessary complexity.

If PClass_PD and Ppeak_PD limits are met, then everything discussed there will have been met.

SuggestedRemedy

Remove lines 7 through 49.

Response   *Response Status* **C**

REJECT.

Cl **33**   *SC* **33.3.7.5**   *P* **142**   *L* **6**   # 175

Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

In figure 33-18 we have "PClass PSE".
Words should be swapped.

SuggestedRemedy

Change to "PSE PClass"

Response   *Response Status* **C**

ACCEPT.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **142**   Page 42 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **6**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.3.7.5**   *P* **142**   *L* **18**   *#* 203

Yseboodt, Lennart   Philips

Comment Type **T**   *Comment Status* **A**   *Editorial*

Figure 33-18 uses T_CUT min which no longer exists.

SuggestedRemedy

Change to T_CUT-2P min

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **33.7.6**   *P* **143**   *L* **11**   *#* 5

Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **D**   *PD Power*

In the text:
"A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.7.2."

33.2.7.2 defines the transients at the PSE PI so when connected to the PD, the PD need to continue to operate.

The problem is that it is not clear what should we expect from the PD when it is tested when this transient behavior is applied directly to the PD PI?
It is obvious that the transients in the PSE PI are identical to PD PI transients at short cable which is one of the operating scenarios.

SuggestedRemedy

Change from:
"A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.7.2."
To:
"A PD shall continue to operate without interruption in the presence of transients applied at the PSE PI or applied at the PD PI as defined in 33.2.7.2."

Proposed Response   *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **33**   *SC* **33.3.7.10**   *P* **145**   *L* **8**   *#* 44

Darshan, Yair   Microsemi

Comment Type **TR**   *Comment Status* **A**   *PD Power*

The text
"All Class 5 and higher PDs shall not exceed Icon-2P-unb for longer than TCUT-2P min as defined in Table 33-11 on any pair. PDs shall...."

Need to be updated to differentiate between single signature PD that need to meet Icon-2P_unb and for dual-signature PD that need to meet IcoN-2P=Pclass-2P/Vport as defined in Equation 33-3c AND YET both PDs need to be tested per 33.3.7.10 WITH UNBALANCED PSE+Channel to ensure that if PD vendor designed his PD to meet Pclass-PD-2P over each pair set, it will not be changed by Type 3 and Type 4 PSEs that doesn't meet PSE PI unbalance requirements.
So PD will have a controlled PSE and Channel environment of unbalance like he has with all other PSE parameters.

SuggestedRemedy

Change from:
"All Class 5 and higher PDs shall not exceed Icon-2P-unb for longer than TCUT-2P min as defined in Table 33–11 on any pair. PDs shall...."
To:
"All Class 5 and higher single-signature PDs shall not exceed Icon-2P-unb for longer than TCUT-2P min as defined in Table 33-11 on any pair. Dual-signature PDs shall not exceed Icon-2P as defined in Equation 33-3c for longer than TCUT-2P min as defined in Table 33-11. Single-signature PDs and dual-signature PDs shall......"

Response   *Response Status* **C**

ACCEPT.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **145**   Page 43 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   *RESPONSE STATUS*: O/open W/written C/closed Z/withdrawn   *Li* **8**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**   *SC* **33.3.7.10**   *P* **145**   *L* **31**   *#* 22

Darshan, Yair   Microsemi

Comment Type **T**   *Comment Status* **A**   *Pres: Darshan1*

The following comments received during D1.3 and D1.4 regarding 33.3.7.10:
1.D1.5 requires in its Editor Note in page 145 line 31 to address longer channel as well since it appears from the current text that Icon-2P_unb need to be met only at short channel while it need to be met at all operating conditions.
On the other hand we know that if Icon-2P_unb is met when PD is tested at short channel (low resistance), it will be the worst case so at longer channel it will meet the requirement too so there is no need to measure the current at two extreme points. To fix this issue we change the text by changing the text from "PD shall meet this requirement …" to PD shall have the pair current measured…".

2.The old test looks like compliance test and some commenters said that we shouldn't do it also there are many examples that we specify test circuit and ask to meet parameters when measured with the test circuit (see 33.4.2, 33.4.3, 33.4.4 33.4.5, 33.4.6, 33.4.9.2.1 and many more in 802.3.
Anyhow, this issue was addressed also by the fix for item 1 with a requirement to meet the Icon-2P_unb by measuring the current at specific conditions.

3.It need to be clear that the two common mode test resistors can flip locations and still the requirement should be met. This was fixed by "……..two common mode resistances of Rsource_min=0.16 ? ± 1% and one with Rsource_max=0.19 ? ± 1%"

4.It was noted also that the test circuit doesn't address the fact that Rsource min/max are very low resistance and it is not clear if the connectors are part of Rsource and if it is, the connectors may affect very much the total value of Rsource etc. To fix this problem the following changes were made:
a)The drawing of the test circuit was modified to show clear boundaries of Rsourc min/max
b)The effect of the test circuit connector resistance on Rsource is minimized by specifying max connector resistance (plug of the test circuit, it is practical to use in test circuit side high quality connector) and substructing it from Rsource. In addition we increase the Rsource ABS numbers by 5% and allow 5% variations with negligible effect on current measurements. The PD RJ45 Jack is not part of the test circuit.

5. Differentiating between DS and SS PD in order to ensure DS PDs meets Icon-2P_unb as defined in Equation 33-3c with unbalanced PSE and channel.

SuggestedRemedy

Change the text per darshan_01_0116.pdf.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 9

Cl **33**   *SC* **33.3.8**   *P* **145**   *L* **46**   *#* 68

Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **A**   *PD MPS*

The existing text,
"A Type 1 or Type 2 PD, or a PD which does not detect a long first class event, shall in addition show the input impedance with resistive and capacitive components defined in Table 33-19."

I assume PDs that want to be very power efficient would draw close to 0 current that would be swamped by the current drawn by Rpd_d of Table 33-19. Only Type 3 and 4 PDs are provided requirements for Autoclassification.

The text, "or a PD which does not detect a long first class event" grants new PD Types with Autoclassification an allowance that would break compatibility legacy AC disconnect PSEs.

SuggestedRemedy

Task Force should discuss the implications of this. The preferred solution is replace the referenced text with,

"All PDs shall show the input impedance with resistive and capacitive components defined in Table 33-19 when connected to a Type 1 or 2 PSE."

This permits new systems to be power efficient and legacy systems to interoperate.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

"A Type 1 or Type 2 PD, or a PD connected to a Type 1 or Type 2 PSE, shall in addition show the input impedance with resistive and capacitive components defined in Table 33-19."

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **145**
Li **46**

Page 44 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.3.8**   *P* **147**   *L* **27**   # 45

Darshan, Yair   Microsemi

Comment Type   **TR**   *Comment Status* **D**   *PD MPS*

See darshan_11_0116.pdf for details.
The use case under discussion is a Type 3 PSE (with asynchronous operation of its pairset) that wants to implement the MPS option in which he looks on the pair with maximum current (for a single signature PD only) and follow the MPS rules on that pair only, and the only PD load is minimum MPS current amplitude, modulated with short MPS (7msce every TMPDO) and the minimum load is introduced right after startup.
In addition there is unbalance e.g. 1mA on the 1st pair and 9mA over the 2nd pair.
In order to perform this task PSE needs to:
-sample pair A
-average pair A
-send the sample to the host (D1).
-sample pair B
-average pair B
-send the sample to the host (D2).
-Host to compare if A>B and follow MPS rules if to disconnect or not.
We can have two problems:
a)Sampling rate of the host for getting the information D1 and D2.
b)Sampling rate of the pairs to generate D1 and D2.
c)The sampling action is not synchronized i.e. there is a time shift between generating the data on pairs A and B and between the acquisition of the data by the host for pairs A and B.
Both (a) and (b) can result with missing the pulses on A or B or both and result with false MPS disconnect action.
When we don't have any issues?
1.If the PD load DC current is > MPS minimum current i.e. 30mA 100mA etc.
2.If the PD load current >= MPS DC current modulated with 75msec pulses every TMPDO.
When we have issues?
When the only load right after the startup is minimum MPS load modulated with 7msec for every TMPDO.
How we can solve the issues?
1.Increasing the sample rate of PSE analog driver to be < 7msec/(2xN).
Problem: No so cost effective I few want to use shared resources e.g. A/D for several ports instead of A/D for each port.
2.Increasing the sample rate of host in addition to (1) to be < 7msec/(2xNxNumber_of_Ports).
Problem: This looks impossible with the current low cost communication used between the host and to the PSE chips e.g. 100kbps which generate about 40-60msec sample rate between PSE chip samples (and this is just for MPS while there are many functions that the host do..)
3.To require PD that for 500msec only after startup, it will use Type 1 MPS values or higher and after 500msec it will continue to use Type 3 short MPS.
-It doesn't add new requirements to PSE.
-It doesn't add additional burden on PD since PD need to support both Type 1/ 2 and Type 3/4 MPS rules anyway and we just reuse it.

-It will guarantee high reliability of MPS detection at the PSE
-It will allow flexible design of PSEs

SuggestedRemedy
See darshan_011_0116.pdf for updated comment and remedy.

Proposed Response   *Response Status* **Z**
PROPOSED REJECT.

This comment was WITHDRAWN by the commenter.

I expect Yair to withdraw this comment as there is an update (comment 47).

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **147**
Li **27**

Page 45 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.3.8**   *P* **147**   *L* **27**   # 47

Darshan, Yair   Microsemi

Comment Type   **TR**   *Comment Status* **D**   *Pres: Darshan11*

This is updated comment to similar one regarding darshan_11_0116.pdf.
See darshan_11_0116.pdf for details.
The use case under discussion is a Type 3 PSE (with asynchronous operation of its
pairset) that wants to implement the MPS option in which he looks on the pair with
maximum current (for a single signature PD only) and follow the MPS rules on that pair
only, and the only PD load is minimum MPS current amplitude, modulated with short MPS
(7msce every TMPDO) and the minimum load is introduced right after startup.
In addition there is unbalance e.g. 1mA on the 1st pair and 9mA over the 2nd pair.
In order to perform this task PSE needs to:
-sample pair A
-average pair A
-host need to read the sample (D1).
-sample pair B
-average pair B
-host need to read the sample (D2).
-Host to compare if A>B and follow MPS rules if to disconnect or not.
We can have two problems:
a)Sampling rate of the host for getting the information D1 and D2.
b)Sampling rate of the pairs to generate D1 and D2.
c)The sampling action is not synchronized i.e. there is a time shift between generating the
data on pairs A and B and between the acquisition of the data by the host for pairs A and
B.
Both (a) and (b) can result with missing the pulses on A or B or both and result with false
MPS disconnect action.
When we don't have any issues?
1.If the PD load DC current is > MPS minimum current i.e. 30mA 100mA etc.
2.If the PD load current >= MPS DC current modulated with 75msec pulses every
TMPDO.
When we have issues?
When the only load right after the startup is minimum MPS load modulated with 7msec for
every TMPDO.
How we can solve the issues?
1.Increasing the sample rate of PSE analog driver to be < 7msec/(2xN).
Problem: Not so cost effective If we want to use shared resources e.g. A/D for several
ports instead of A/D for each port.
2.Increasing the sample rate of host in addition to (1) to be <
7msec/(2xNxNumber_of_Ports).
Problem: This looks impossible with the current low cost communication used between the
host and to the PSE chips e.g. 100kbps which generate about >>7msec sample rate
between PSE chip samples in multiport system (and this is just for MPS while there are
many functions that the host do..)
3.To require PD that for 500msec only after startup, it will use Type 1 MPS values or higher
and after 500msec it will continue to use Type 3 short MPS.
The advantages of the suggested 3rd solution option:
-It doesn't add new requirements to PSE.

-It doesn't add additional burden on PD since PD need to support both Type 1/ 2 and Type
3/4 MPS rules anyway and we just reuse it.
-It will guarantee high reliability of MPS detection at the PSE
-It will allow flexible design of PSEs

SuggestedRemedy
See darshan_011_0116.pdf for updated comment and remedy.

Proposed Response   *Response Status* **Z**
REJECT.

This comment was WITHDRAWN by the commenter.

Yair will present this material (with updates) next time.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **147**   Page 46 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **27**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **33**　　*SC* **33.6.3.2**　　　　*P* **168**　　*L* **9**　　　*#* 214
Schindler, Fred　　　　　　　Seen Simply

Comment Type **TR**　　*Comment Status* **D**　　　　　　　*DLL*

Accepted D1.4 comments 161, 162, 158, 163, 160, and 164, broke how Extended power functions. Note that newly created Table 33-16a has incorrect values for PClass_PD, and was referenced in many of these comments as the reason for the change. One incorrect table resulted in at least six changes to the draft. The changes resulted in Physical layer and DLL power values not agreeing. For example, if a PSE powers a Type-4 class-8-SS PD the PD gets Pclass of 90W using physical layer classification. After the Draft changes, the DLL initialized value is 71W. Therefore, if the PD is using extended power the PSE will see a PD request and power consumption that exceeds the 71W provided by the PSE. The PSE may then remove power to the PD. In the worst-case, the PD will consume more than 25% more than the power allocated by the PSE.

Physical and DLL values will match when D1.4-PSE DLL initial values are used and Table 33-16a are corrected. If required, a PSE supporting DLL can use the power negotiation mechanism to reduce the power supplied to the PD.

SuggestedRemedy

Restore the initial values before the changes made by comments 161, 162, 158, 163, 160, and 164.

On page 132 change PClass_PD for Type-3, SS, class-6 PDs from 51.0 to 60.0, and change PClass_PD for Type-4, SS, class-8 PDs from 71.0 to 90.0.

Note if the Task Force prefers, rather than restoring class-8 maximums to 99.0 W the value 90.0 W may be used. The value 90.0 W is required for correct Extended power operation. The value 99.0W permits Extended power and devices outside the standard to use power levels that meet LPS requirements.

Proposed Response　　　　*Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

TFTD as this was changed as part of D1.4 comment cycle.

Cl **33**　　*SC* **33.6.3.3**　　　　*P* **171**　　*L* **14**　　*#* 48
Bennett, Ken　　　　　　　Sifos Technologies, In

Comment Type **TR**　　*Comment Status* **A**　　　　　　　*DLL*

It seems like PSE_DLL_POWER_TYPE should have been changed to PSE_DLL_POWER_LEVEL in all instances, but was only changed in 33.3.3.3. Also, the definitions have the issues discussed below.

33.6.3.3 definition (Pg 171, ln 24):
PSE_DLL_POWER_TYPE: A control variable that indicates the Type of the PSE by which the PD is being powered...
PROBLEM: It doesn't; it is set by PSE_POWER_LEVEL in the State Diagram, which is based upon the Type that was assumed based upon the allocation.

33.3.3.3 definition (pg 124, ln 17):
PSE_DLL_POWER_LEVEL: a control variable output by the PD power control state diagram (Figure 33-28) that indicates the power level of the PSE by which the PD is being powered...
PROBLEM: PSE_DLL_POWER_LEVEL isn't in 33-28. 33-28 uses PSE_DLL_POWER_TYPE. Also, a given value does not convey a single power level.

SuggestedRemedy

Change all instances of PSE_DLL_POWER_TYPE to PSE_DLL_POWER_LEVEL.

Change the definitions to:
PSE_DLL_POWER_LEVEL: A control variable output by the PD power control state diagram (33-28) that indicates the minimum PSE Type capable of providing the assigned Class.

Response　　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

Change all instances of PSE_DLL_POWER_TYPE to PSE_DLL_POWER_LEVEL.

Change the definitions to:
PSE_DLL_POWER_LEVEL: A control variable output by the PD power control state diagram (33-28) that indicates the power level of the PSE by which the PD is being powered.

Ken, please review this…

Need to align with PSE_power_level variable.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **171**
Li **14**

Page 47 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33.6.3.3**   *P* **171**   *L* **26**   # 51

Bennett, Ken   Sifos Technologies, In

Comment Type **TR**   *Comment Status* **A**   *DLL*

There are two different definitions for PSE_POWER_LEVEL, and each has innacuracies.

PSE_POWER_LEVEL is defined in 33.6.3.3 as "a control variable output by the PD state diagram (Figure 33–16) to indicate the Type of PSE by which it is being powered..."
PROBLEM: It conveys the PSE Type based upon allocation, which may be lower than the actual PSE Type.

PSE_POWER_LEVEL is defined in 33.3.3.3 as "a control variable that indicates to the PD the level of power the PSE is supplying..." (pg 124, line 26)
PROBLEM: It doesn't convey a single power level. For instance, a value of 3 could be an allocation of class 5 or class 6.

SuggestedRemedy

Change both definitions to:

PSE_POWER_LEVEL: A control variable output by the PD state diagram that indicates the minimum PSE Type capable of providing the assigned class.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change both definitions to:

PSE_POWER_LEVEL: A control variable output by the PD state diagram that indicates the power level assigned by the PSE. This value is a result of the class requested by the PD and the power available from the PSE.

Cl **33**   *SC* **33A.3**   *P* **197**   *L* **13**   # 176

Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

"33A.3 Intra Pair Resistance Unbalance"
Section name has every word capitalized.
Not in line with Style Guide.

SuggestedRemedy

change to: "33A.3 Intra-pair resistance unbalance"

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **33A.4**   *P* **197**   *L* **30**   # 177

Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

"33A.4 Recommended Channel Requirement For pair-to-pair Resistance Unbalance in 4-Pair Operation"
Section name has every word capitalized.
Also, something is either a REQUIREMENT or RECOMMENDED, but not both.
Not in line with Style Guide.

SuggestedRemedy

Change to: "33A.4 Pair-to-pair channel resistance unbalance requirement for 4-pair operation"

Response   *Response Status* **C**

ACCEPT.

NonEasy

Cl **33**   *SC* **33A.5**   *P* **198**   *L* **1**   # 178

Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

Figure 33A-4 is titled "PSE PI unbalance specification and E2EP2PRunb"

SuggestedRemedy

Change to "PD Resistance unbalance elements overview"

Response   *Response Status* **C**

ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **198**
Li **1**

Page 48 of 55
1/21/2016 1:23:25 PM

Cl **33**　　*SC* **33A.5**　　　　　*P* **198**　　*L* **21**　　　# 179

Yseboodt, Lennart　　　　　　Philips

Comment Type **E**　　*Comment Status* **A**　　　　　*Unbalance*

"R Pair_PD_max and R Pair_ PD_min represent PD common mode input effective impedance of pairs of the same polarity. The effective resistance Z i is the measured..."
Concept of "resistance" and "impedance" is mixed up.

SuggestedRemedy

"R Pair_PD_max and R Pair_ PD_min represent PD common mode input effective resistance of pairs of the same polarity. The effective resistance R_i in Figure 4 is the measured..."
- Change Z to R in Figure 4.

Response　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

Lennart has editorial license to change all Z's and impedances to R's and resistances in Annex 33A.5

Cl **33**　　*SC* **33A.5**　　　　　*P* **198**　　*L* **22**　　　# 180

Yseboodt, Lennart　　　　　　Philips

Comment Type **E**　　*Comment Status* **A**　　　　　*Unbalance*

"The effective resistance Z i is the measured voltage V eff_pd_i..."
Not clear what 'i' is about. Also choice of 'i' unfortunate since there are also currents involved.

SuggestedRemedy

Clarify: "The effective resistance Z_n (where n is the pair number) is the measured voltage V_eff_pd_n..."

Response　　　　　*Response Status* **C**

ACCEPT.

Cl **33B**　　*SC* **33B**　　　　　*P* **201**　　*L* **1**　　　# 124

Stover, David　　　　　　LTC

Comment Type **E**　　*Comment Status* **A**　　　　　*Pres: Darshan9*

Numbering for Annex 33B tables and figures has been updated; appears incorrect. For example, a reference to "Table 33B-1" on line 12 is now "Table 1".

SuggestedRemedy

Please reapply necessary numbering override to format figure and table references correctly in Annex 33B.

Response　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

Lennart to check with editorial staff on correct table numbering in annexes.

Cl **33**　　*SC* **33B**　　　　　*P* **201**　　*L* **1**　　　# 192

Yseboodt, Lennart　　　　　　Philips

Comment Type **ER**　　*Comment Status* **A**　　　　　*Editorial*

Page numbers are missing for pages in Annex 33B.

SuggestedRemedy

Add page numbers.

Response　　　　　*Response Status* **C**

ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **201**
Li **1**

Page 49 of 55
1/21/2016 1:23:25 PM

Cl **33** *SC* **Annex 33B** *P* **201** *L* **8** # 41
Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **A** *Pres: Darshan9*

[33.2.7.4.1 Page 108, Lines 37-38 in D1.5
Annex B: Page 201 - 204 in D1.5

Background
This comment tries to resolve comment #144 from D1.4.
Summary of comment and remedy of 144 from D1.4:
a) When reading 33.2.7.4.1 (PSE P2PRunb) there is a link to Annex B which is normative
and contains shalls and readers may miss to read these shalls.
b) Annex 33B contains: 2 shalls, 2 musts. Do we need a normative annex for 2 shalls?
c) Also, the shalls are very similar to each other.
The remedy for comment 144 from D1.4:
Proposed remedy: TF to discuss the 'musts' and either reword or turn into 'shalls'.
The final remedy: To consider moving the requirement into the appropriate section ,
33.2.7.4.1 seems like a good candidate.
Add "Editor's Note (TBRBD2.0): Yair working to move the shalls to clause 33. Readers are
encouraged to work with him."
Response to the comments above:
a)33.2.7.4.1 was modified by adding shall to meet Annex B requirements so annex B will
not be overlooked for its shalls.
b)Yes, we need the normative Annex due to the fact that we need to use the test circuit
and procedure as proposed. In addition, the "shalls" there were clarified, some of the
"must" converted to shall and some deleted by editorial changes. So far Annex B is the
simplest way to achieve annex B objectives without complicating the standard body.
c)The shalls are not exactly similar to each other, they are referring to different alternative
tests and for each test different parameters are tested. Some editorial changes were made
to clarify it.
d)It was hard to move all the shalls to 33.2.7.4.1 as proposed, instead, 33.2.7.4.1 was
modified to include shall for the test methods in Annex 33B without changing most of the
shalls in Annex 33B.
e) Some editorial changes made due to typos and other errors

SuggestedRemedy
See darshan_09_0116.pdf

Response *Response Status* **C**
ACCEPT IN PRINCIPLE.

Adopt darshan_09_0116.pdf with editorial liscence to merge with other adopted comments.

Cl **33** *SC* **33B** *P* **201** *L* **24** # 181
Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *Editorial*

In Figure 33B-1 it shows "PD+Channel", this can be misread as the + channel.

SuggestedRemedy
Change to: "PD and Channel".

Response *Response Status* **C**
ACCEPT.

EZ

Cl **33** *SC* **33B.2** *P* **203** *L* **6** # 182
Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *Pres: Yseboodt1*

Voltages V1 and V2 in Fig 33B-3 are not referenced to anything.

SuggestedRemedy
Replace by yseboodt_1_0116_fig33b3_v100.pdf.
In the measurement recipe below, change as follows:
2) Measure Vdiff
4) Measure Vdiff' in the same manner as Vdiff

Response *Response Status* **C**
ACCEPT.

Cl **33** *SC* **33B.3** *P* **204** *L* **7** # 183
Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **A** *Pres: Yseboodt6*

In Figure 33B-4 it is unclear if the load is a current sink or a constant power load.
Also PSE should be PSE PI.
Also 'PD + Channel' should be 'PD and Channel'.

SuggestedRemedy
Replace Figure by yseboodt_6_0116_fig33b4_v100.pdf

Response *Response Status* **C**
ACCEPT.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **204**
Li **7**

Page 50 of 55
1/21/2016 1:23:25 PM

Cl **33**   *SC* **33B.3**   *P* **204**   *L* **26**   # 14
Darshan, Yair   Microsemi

Comment Type **ER**   *Comment Status* **A**   *Editorial*
Typo in the text:
"Swap R_max, R_min, repeat steps 1 and 2."

SuggestedRemedy
Change from:
Swap R_max, R_min, repeat steps 1 and 2.
To:
Swap Rload_max, Rload_min, repeat steps 1 and 2.

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **33**   *SC* **33B.3**   *P* **204**   *L* **31**   # 13
Darshan, Yair   Microsemi

Comment Type **ER**   *Comment Status* **A**   *Editorial*
We have changed in D1.4 comment cycle Rpair_max/min to Rpse_min/max and the following text was forgotten.
"Verification of Icon-2P_unb in step 6 confirms PSE RPair_max and RPair_min are in conformance to Equation (33-4f).

SuggestedRemedy
Change from:
Verification of Icon-2P_unb in step 6 confirms PSE RPair_max and RPair_min are in conformance to Equation (33–4f).
To:
Verification of Icon-2P_unb in step 6 confirms PSE Rpse_max and Rpse_min are in conformance to Equation (33–4f).

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **79**   *SC* **79.3.2**   *P* **213**   *L* **37**   # 80
Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **A**   *Editorial*
The length of the LLDP frame shown in Figure 79-3 is 18 octets. The value show in TLV information string length is 20, which is incorrect.

SuggestedRemedy
Replace the reference value 20 with 18.

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **79**   *SC* **79.3.2.4**   *P* **215**   *L* **6**   # 54
Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Editorial*
Fix the typo, "TLV.."

SuggestedRemedy
Replace with "TLV."

Response   *Response Status* **C**
ACCEPT.

EZ

Cl **79**   *SC* **79.3.2.6b**   *P* **218**   *L* **1**   # 193
Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *Editorial*
Accepted Comment no. 205 from D1.4 cycle was not implemented.

SuggestedRemedy
Implement comment no. 205 from D1.4.

Response   *Response Status* **C**
ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line   *Pa* **218**   *Li* **1**   Page 51 of 55   1/21/2016 1:23:25 PM

Cl **79**   *SC* **79.3.2.6b**   *P* **218**   *L* **34**   # 81
Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **A**   *Editorial*

Please implement the accept D1.4 change to Bit 1 of Table 79.6b.

SuggestedRemedy

Please implement the accept D1.4 change to Bit 1 of Table 79.6b. See comment 205.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 193

EZ

Cl **79**   *SC* **79.3.2.6b**   *P* **220**   *L* **1**   # 82
Schindler, Fred   Seen Simply

Comment Type **TR**   *Comment Status* **A**   *LLDP*

Table 79.6e is associated with section 79.3.2.6b but appears in the Link Aggregation TLV clause. This Table does not belong in the LLDP section. It belongs in a section that covers Autoclassification usage for the PSE and PD, which is similar in design to 33.6. This section should provide a state diagram that covers information contained in the table.

SuggestedRemedy

The Task Force should discuss the implications of this. For now I recommend, moving the reference table to a new section 33.6.5. Add the Editor's note below the table,
"Editor's Note: Participants are encouraged to provide text and a state diagram to complete the requirements for Autoclassification."

Delete the sentence on p 219 L29,
"The sequence of Autoclass as triggered by LLDP is listed in Table 79-6e."

Response   *Response Status* **C**

ACCEPT.

Cl **79**   *SC* **79.3.2.6d**   *P* **220**   *L* **18**   # 55
Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *Editorial*

Table 79.6f is associated with section 79.3.2.6e but appears in the Link Aggregation TLV clause.

SuggestedRemedy

Move the reference table to the clause that covers it.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Is this just Frame sticking the Table where it fits? Editor to fix if possible…

EZ

Cl **79**   *SC* **79.3.7**   *P* **224**   *L* **28**   # 2
Skinner, John   Sifos Technologies, In

Comment Type **TR**   *Comment Status* **A**   *LLDP*

Figure 79-7a indicates that the PD measurements field is 9 octets in length, and that the PSE measurements field is 9 octets in length. Table 79-7a defines the PD measurements field as 96 bits in length, and Table 79-7b defines the PSE measurements field as 96 bits in length. A 96 bit field requires 12 octets, so the stated field lengths are incorrect. Once these field lengths are corrected, the TLV information string length will also need to be corrected.

SuggestedRemedy

Modify the TLV intformation string length field to indicate 32 octets.
Modify the length specified in the TLV information string for the PD measurements field to 12 octets, and the lenght specified for the PSE measurements field to 12 octets.

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

Modify the TLV intformation string length field to indicate 26 octets.
Modify the length specified in the TLV information string for the PD measurements field to 12 octets, and the lenght specified for the PSE measurements field to 12 octets.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Page, Line

Pa **224**   Page 52 of 55
Li **28**   1/21/2016 1:23:25 PM

Cl **79**　　　*SC* **79.3.7**　　　　　*P* **224**　　　*L* **29**　　　# 83
Schindler, Fred　　　　　　　　　Seen Simply

Comment Type **TR**　　*Comment Status* **A**　　　　　*LLDP*

The length of the LLDP frame shown in Figure 33-3 is 24 octets. The value show in TLV information string length is 26, which is incorrect.

SuggestedRemedy

Replace the reference value 26 with 24.

Response　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 2

Cl **79**　　　*SC* **79.3.7.1**　　　*P* **224**　　　*L* **38**　　　# 56
Schindler, Fred　　　　　　　　　Seen Simply

Comment Type **ER**　　*Comment Status* **A**　　　　　*LLDP*

Existing text may be improved by removing repeated text that is not required.

"The PD measured voltage value field may be included to carry the PD's measured voltage
value at the port
defined in Table 79-7a. The PD measured current value field may be included to carry the PD's measured
current value at the port defined in Table 79-7a. The PD measured energy value field may be included to
carry the PD's measured energy consumption value at the port defined in Table 79-7a."

SuggestedRemedy

"The PD measured voltage value field carries a PD measured voltage value at the PI
defined in Table 79-7a. The PD measured current value field carries a PD measured
current value at the PI defined in Table 79-7a. The PD measured energy value field
carries a PD measured energy consumption value at the PI defined in Table 79-7a."

Response　　　　　*Response Status* **C**

ACCEPT.

Cl **79**　　　*SC* **79.3.7.1**　　　*P* **224**　　　*L* **38**　　　# 194
Yseboodt, Lennart　　　　　　　Philips

Comment Type **ER**　　*Comment Status* **A**　　　　　*LLDP*

79.3.7.1 PD measurements refers to 'port' when it should refer to PD PI + reword.

"The PD measured voltage value field may be included to carry the PD's
measured voltage value at the port defined in Table 79-7a. The PD measured current value
field may be included to carry the PD's measured current value at the port defined in Table
79-7a. The PD measured energy value field may be included to carry the PD's measured
energy consumption value at the port defined in Table 79-7a."

SuggestedRemedy

"The PD's measured voltage value field may be included to carry the PD's measured
voltage value at the PI or pairset as defined in Table 79-7a. The PD's measured current
value field may be included to carry the PD's measured current value at the PI or pairset as
defined in Table 79-7a. The PD's measured energy value field may be included to carry the
PD's measured energy consumption value at the PI or pairset as defined in Table 79-7a."

Response　　　　　*Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 56

Cl **79**　　　*SC* **79.3.7.1**　　　*P* **224**　　　*L* **43**　　　# 57
Schindler, Fred　　　　　　　　　Seen Simply

Comment Type **ER**　　*Comment Status* **A**　　　　　*Editorial*

Fix typo "(voltage".

SuggestedRemedy

Replace with "voltage".

Response　　　　　*Response Status* **C**

ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general　　　*Pa* **224**　　　Page 53 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected　　RESPONSE STATUS: O/open W/written C/closed Z/withdrawn　　*Li* **43**　　　1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **79**   *SC* **79.3.7.2**   *P* **224**   *L* **51**   # 58

Schindler, Fred   Seen Simply

Comment Type **ER**   *Comment Status* **A**   *LLDP*

Existing text may be improved by removing repeated text that is not required.

"The PSE measured voltage value field may be included to carry the PSE's measured voltage value at the port
defined in Table 79-7b. The PSE measured current value field may be included to carry the PSE's measured current value at the port defined in Table 79-7b. The PSE measured energy value field may be included to
carry the PSE's measured energy consumption value at the port defined in Table 79-7b."

SuggestedRemedy

Replace referenced text with,

"The PSE measured voltage value field carries a PSE measured voltage value at the PI defined in Table 79-7b. The PSE measured current value field carries a PSE measured current value at the PI defined in Table 79-7b. The PSE measured energy value field carries a PSE measured energy consumption value at the PI defined in Table 79-7b."

Response   *Response Status* **C**

ACCEPT.

Cl **79**   *SC* **79.3.7.2**   *P* **224**   *L* **51**   # 195

Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *LLDP*

79.3.7.1 PSE measurements refers to 'port' when it should refer to PSE PI + reword.

"The PSE measured voltage value field may be included to carry the PSE's measured voltage value at the port defined in Table 79-7b. The PSE measured current value field may be included to carry the PSE's measured current value at the port defined in Table 79-7b. The PSE measured energy value field may be included to carry the PSE's measured energy consumption value at the port defined in Table 79-7b."

SuggestedRemedy

"The PSE's measured voltage value field may be included to carry the PSE's measured voltage value at the PI or pairset as defined in Table 79-7b. The PSE's measured current value field may be included to carry the PSE's measured current value at the PI or pairset as defined in Table 79-7b. The PSE's measured energy value field may be included to carry the PSE's measured energy consumption value at the PI or pairset as defined in Table 79-7b."

Response   *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE by 58

Cl **33**   *SC* **79.3.7.2**   *P* **225**   *L* **54**   # 184

Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

Line missing at bottom of table 79-7a.

SuggestedRemedy

Add line.

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **79**   *SC* **79.3.7.3**   *P* **226**   *L* **5**   # 196

Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *Editorial*

V_Port_PD should be V_Port_PD-2P.

SuggestedRemedy

Fix.

Response   *Response Status* **C**

ACCEPT.

EZ

Cl **33**   *SC* **79.3.7.2**   *P* **227**   *L* **54**   # 185

Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*

Line missing at bottom of table 79-7b.

SuggestedRemedy

Add line.

Response   *Response Status* **C**

ACCEPT.

EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general   *Pa* **227**   Page 54 of 55
COMMENT STATUS: D/dispatched A/accepted R/rejected   RESPONSE STATUS: O/open W/written C/closed Z/withdrawn   *Li* **54**   1/21/2016 1:23:25 PM
SORT ORDER: Page, Line

Cl **79**   *SC* **79.3.7.3**   *P* **228**   *L* **8**   # 197
Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *Editorial*
    V_PORT_PSE is capitalized.
        I_PORT and I_PORT-2P is capitalized.

SuggestedRemedy
    Change to:
        V_Port_PSE-2P, I_Port and I_Port-2P respectively.

Response   *Response Status* **C**
    ACCEPT.

    EZ

Cl **79**   *SC* **79.3.7.3**   *P* **228**   *L* **28**   # 204
Yseboodt, Lennart   Philips

Comment Type **T**   *Comment Status* **A**   *LLDP*
    The meaning of the value of the Power price index field is not specified.
        In order to future-proof this field, a bit should be allocated for future use.

SuggestedRemedy
    The MSB bit set to 1 will have a reserved meaning.
        Add a new row to Table 79-7c
        Bit   Function   Value/meaning
        15   Future use   1 = Reserved / ignore field
        .   0 = Power price index in bits 14:0
        Change existing row:
        14:0   Power price index   Power price index = decimal value of bits.
        .   Valid values for these bits are decimal 1 through
    32767.

Response   *Response Status* **C**
    ACCEPT.

Cl **79**   *SC* **79.3.7.3**   *P* **228**   *L* **28**   # 198
Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *Editorial*
    Table 79-7c is missing a caption.

SuggestedRemedy
    Caption = "Power price index value field"

Response   *Response Status* **C**
    ACCEPT.

    EZ

Cl **79**   *SC* **79.3.7.3**   *P* **228**   *L* **34**   # 199
Yseboodt, Lennart   Philips

Comment Type **ER**   *Comment Status* **A**   *Editorial*
    Table 79-7c, value cell, missing space between '1 through65535'

SuggestedRemedy
    Fix.

Response   *Response Status* **C**
    ACCEPT.

    EZ

Cl **33**   *SC* **79.4.2**   *P* **232**   *L* **49**   # 186
Yseboodt, Lennart   Philips

Comment Type **E**   *Comment Status* **A**   *Editorial*
    Line missing at bottom of table 79-10.

SuggestedRemedy
    Add line.

Response   *Response Status* **C**
    ACCEPT.

    EZ

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
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SORT ORDER: Page, Line

Pa **232**
Li **49**

Page 55 of 55
1/21/2016 1:23:25 PM