Cl **33** *SC* **33.1** *P* *L* **11** # 58

Schindler, Fred — Seen Simply

Comment Type **ER** *Comment Status* **D** *Maintenance*

Several new additions use the construct choice1/choice2 to signify something that may be missinterpreted. Some of this construction are used in legacy text too.

SuggestedRemedy

Replace these constructs with words. For example,

These enitites allow devices to draw or supply ...

Proposed Response *Response Status* **W**

The specific text referenced on line 11 is existing text that we have not changed. This should be filed as a maintenance request.

PROPOSED REJECT.

Cl **33** *SC* **33.1.4** *P* **21** *L* **50** # 139

Jones, Chad — Cisco

Comment Type **T** *Comment Status* **D** *Cabling*

Maintenance Request #1271, on behalf of GEOFF THOMPSON, GRACASI S.A./LINEAR TECHNOLOGY

Move as much of the cabling specification to cabling documents as possible. (This RR was entered as a tracking mechanism for Thompson Comment #59 against P802.3REVbx/D2.0 during initial WG ballot. Resolution of this comment was given over to P802.3bt as they will have Cl 33 open.)

SuggestedRemedy

See attached sheet for proposed new text.
(http://www.ieee802.org/3/maint/requests/maint_1271.pdf, page 2)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

A number of these changes have already been adopted. The two remaining changes are:

Replacing the first sentence in 33.1.4 with:

"A power system, consists of a single PSE, a single PD and the link section connecting them. A power system is
characterized as Type 1 or Type 2 by lowest type number of the PSE or PD in the system, see Table 33–1."

and replacing the first paragraph of 33.1.4.1 with (as well as changing the title of the subclause to "Cabling requirements"):

"The supply of power over the data connection is intended to operate with no additional requirements to the cabling that is
normally installed for data usage. This is approximately true but may require some further attention. Power at Type 1
power levels may be transmitted over all specified premises cabling without further restrictions. Higher power levels may
require heavier gauge conductors than are found in Class C/Category 3 cabling and (more uncommonly) in some lighter
gauge Class D or better cable. The requirements for Type 2 are met by Category 5 or better cable and components as
specified in ANSI/TIA/EIA-568-A."

Cl **33** *SC* **33.1.4** *P* **22** *L* **21** # 114

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *Cabling*

Icable for Type 4 is TBD.

SuggestedRemedy

We have adopted 99.9W as the maximum allowed Ptype.
Icable = (99.9W / 52V) / 2 = 0.960 A (+footnote ref 3)
3: "In Type 4, Class 8 Operation, the current per pair-set might be impacted by pair to pair system resistance unbalance."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Possible OBE by comment #11.

Partial OBE by comment #12.

Cl **33** *SC* **33.1.4** *P* **22** *L* **21** # 11

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *Cabling*

Table 33-1.
Some of the TBD parameters can be updated per the work done at page 10 of: http://www.ieee802.org/3/bt/public/mar15/darshan_01_0315_rev009a.pdf.
Table 33-1 need to be revised per the folowing proposal. Please see attached "Draft D0.4: Revised Table 33-1.pdf:
The parameters are:
Type 4 Icable: 0.962A (TIA guys will have to tell us the # of cables max etc. later)
In addition, the following TBD parameters can be updated as well:
Cable Type: same as in Type 3 and adding a text notifying number of cables per bundle TBD. This will be delivered by TIA etc.
Loop resistance: Same as for Type 3.
To add new row that specify Type 4 parameter for new and better cable that allows 100 cables per bundle. In this row, cabling Type, loop resistance is TBDs.

SuggestedRemedy

Table 33-1 to update the following Type 4 parameters (See attached "Draft D0.4: Revised Table 33-1.pdf" document":

1. Type 4 Icable: 0.962A.
2. Cable Type: same as in Type 3. Add note below table: "Number of cables per boundle TBD per TBD standard.
3. Loop resistance: Same as for Type 3.
4. To add new row that specify Type 4 parameter for new and better cable that allows 100 cables per bundle. In this row, cabling Type, loop resistance is TBDs. The current is the same as in step 1.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Need referenced document.

Cl **33** *SC* **33.1.4.2** *P* **23** *L* **10** # 143

Jones, Chad Cisco

Comment Type **T** *Comment Status* **D** *Cabling*

Maintenance WG Ballot comment #60 on behalf of GEOFF THOMPSON, GRACASI S.A./LINEAR TECHNOLOGY

(through line 28, i.e. the entirety of 33.1.4.2)
The first sentence should be deleted. It would be appropriately handled by updating the reference to 11801 to the 2002 edition which precisely matches this requirement with the following text: 6.4.8 Direct current (d.c.) resistance unbalance
The d.c. resistance unbalance between the two conductors within each pair of a channel shall not exceed 3 % for all classes. This shall be achieved by design.
The remainder of 33.1.4.2 should be deleted as it is purely informative/tutorial material on cabling parameter measurement. It is more appropriate to the referenced cabling documentation. If 802.3 strongly feels that it needs to be retained in our document then it should be moved to an informative annex. (Ref: 2014 Style Manual, cl. 10.1, last paragraph)

SuggestedRemedy

With both of these actions being taken, the entire sub-clause should be deleted.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Move section (with appropriate changes) to informative annex.

Cl **33** *SC* **33.2.0a** *P* **24** *L* **24** # 38

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Types*

Table 33-1a: 75W class is missing

SuggestedRemedy

Add row for 75W class

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The table is for "Permissible PSE Types". 75W is not a Type boundary and should not be listed, just as 45W and all of the classes <15W are not listed.

Cl **33** *SC* **33.2.0a** *P* **24** *L* **30** # 37

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Types*

Table 33-1a, Note 4: "Can operate as 2-pair under fault conditions" is unnecessary and suggests that 2-pair operation is specified behavior for 60W and greater PDs. 2-pair operation is not possible at these power levels, and fault behavior is not typically specified.

SuggestedRemedy

Delete note 4.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

If operating over 2 pairs under fault conditions, the PSE would then be a 30W or less PSE and would be covered by other rows in this table.

Would OBE part of comment #59.

Cl **33** *SC* **33.2.1** *P* **24** *L* **46** # 10

Bustos Heredia, Jairo Würth Elektronik eiSo

Comment Type **E** *Comment Status* **D** *Types*

PSEs may support either Alternative A, Alternative B, or both.

SuggestedRemedy

PSEs may support either Alternative A, Alternative B or both. When using Alternative A, power will be provided through pairs 2 and 3, whereas when using Alternative B, pairs 1 and 4 will be used for power provision.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

These pin definitions are shown in Table 33-2.

Cl **33** *SC* **33.2.3** *P* **31** *L* **8-23** # 88

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *Types*

In a 4P system, the word Alternative in Table 33-2 implies that either A or B can be chosen but not both.

SuggestedRemedy

Rename "Alternative" to "Configuration".
This renaming will also affect other mentions of Alternative in the draft.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

I do not believe that the word "alternative" is causing confusion when applied to 4-pair power.

Cl **33** *SC* **33.2.4.1** *P* **32** *L* **20** # 39

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *4P Power*

Unclear text: "A Type 3 or Type 4 PSE that is capable of delivering power over both Alternative A and Alternative B simultaneously is not required to meet backoff algorithm."

SuggestedRemedy

Replace with: "A Type 3 or Type 4 PSE that intends to provide power on both Alternative A and Alternative B is not required to use the backoff algorithm."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

How about: "A Type 3 or Type 4 PSE that delivers power over both Alternative A and Alternative B simultaneously is not required to use the backoff algorithm.

Cl **33** *SC* **33.2.4.1** *P* **32** *L* **20** # 67

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D** *4P Power*

This text permits a new Type midspan to power the PD using 4P but it does not ensure this will be the case.

Replacing this text to requiring legacy behavior permits a consistent process to be used by customers to locate this potential problem. If a midspan is placed between an end-point PSE and a PD, normally the end-point PSE will power the PD.

This undesirable operation can then be discovered remotely by looking at the end-point PSE. Upon discovery, the admin may disable the end-point PSE port to ensure the midspan always powers the PD.

If the existing text is used the configuration may be different after each power cycle.

SuggestedRemedy

Stike the added sentence.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Should we require 4P midspans to use the back-off algorithm? Maybe.

We should NOT require 4P endspans to use the back-off algorithm which striking this sentence would require.

Cl **33** *SC* **33.2.4.4** *P* **37** *L* **8** # 13

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PSE Classification*

Table 33-3 column "class_num_events" adresses max class_num_events for describing if PSE_DLL_CAPABLE is true or false.

SuggestedRemedy

change column tytle to "max class_num_events"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The definition of class_num_events already indicates that it is the maximum number of class events a PSE supports.

Cl **33** *SC* **33.2.4.4** *P* **39** *L* **32** # 14

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PSE State Diagram*

Missing pointer to do_detection details.

SuggestedRemedy

Add "See 33.2.5"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

None of the other functions have pointers to their respective sections of the standard.

Cl **33** *SC* **33.2.4.4** *P* **40** *L* **14** # 15

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PSE State Diagram*

Addressing the editor note of the meaning of mutual identification is not complete:
Mutual identification is not complete if the objectives of 33.2.6 are not met.
This is mentioned in line 5.
""When a Type 2 PSE powers a Type 2, Type 3 or Type 4 PD, the PSE may choose to assign a value of '1' to parameter type if mutual identification is not complete (see 33.2.6) and shall assign....."

Specifically, Mutual identification is not complete per the text in clause 33.2.6.page 47 lines 15-20.
"Mutual identification is the mechanism that allows a Type 2, Type 3 or Type 4 PD to differentiate between Type 1, Type 2, Type 3 and Type 4 PSEs. Additionally, mutual identification allows Type 2, Type 3 or Type 4 PSEs to differentiate between Type 1, Type 2, Type 3 and Type 4 PDs. PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices."
So if PSE fail to detect the PD class than classification is not complete.
For mutual Identification to be completed, the PD needs to know who is the PSE type etc.

SuggestedRemedy

No need to define "Mutual Identification is not complete". It is already clearly defined in 33.2.6.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Accepting this comment results in no changes to the text.

Cl **33** *SC* **33.2.4.5** *P* **40** *L* **19-2** # 120

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **D** *PSE State Diagram*

"When a PSE powers a PD of a lower Type than its maximum capability, the PSE shall meet the PI electrical requirements of PSE Type that matches the PD Type, but may choose to meet the electrical requirements of a greater Type (up to its maximum capability) for I Con-2P , I LIM-2P , T LIM-2P , and P Type (see Table 33â€“11)."

Unclear and grammatically dubious sentence.

SuggestedRemedy

When a PSE powers a PD of a lower Type than its own, the PSE shall meet the PI electrical requirements
of the PSE Type that corresponds to the connected PD Type.
The PSE may choose to apply the requirements for
I Con-2P , I LIM-2P , T LIM-2P and P Type (see Table 33â€“11) of any Type smaller or equal than the
PSE Type and larger or equal than the PD Type.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Type and power are not directly related and this needs further study (as the editor's note is there to remind us).

Cl **33** *SC* **33.2.4.7** *P* **42** *L* **2** # 75

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE State Diagram*

Where is entry point "A1" coming from?

SuggestedRemedy

If "A1" is just another portion of "A" replace "A1" with "A."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

"A1" needs a separate entrance because it leads to a different state than "A". An "A1" exit from the main diagram needs to be added and this will be done when the state diagram is updated.

Accepting this comment does not result in any changes to the text as of now.

Cl **33** *SC* **33.2.4.7** *P* **42** *L* **27** # 32

Darshan, Yair — Microsemi

Comment Type **T** *Comment Status* **D** *PSE State Diagram*

In state diagrame figure 33-9 there is a missing exit from CLASS_EV3 to point "E" which we have in all other CLASS_EV_XX BLOCKS.

In addition, an exit is missing also from CLASS_EV3 to MARK_EV_LAST as we have it also from other CLASS_EV_XX BLOCKS.

SuggestedRemedy

1) Add exit from CLASS_EV3 to point "E": Tcle3_timer_done*(mr_pd_class_detectted=0)

2) Add exit from CLASS_EV3 to MARK_EV_LAST:
Tcle3_timer_done*(mr_pd_class_detected=4)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

There is no need for an exit from CLASS_EV3 to E as there can be no class mismatch in CLASS_EV3 (all class signatures are valid in CLASS_EV3).

There is an exit to MARK_EV_LAST from CLASS_EV3, but "Tcle3_timer_done * " needs to be added in front of "(mr_pd_class_detected = 4)"

Cl **33** *SC* **33.2.5** *P* **43** *L* **41** # 44

Stencel, Len — Bourns, Inc.

Comment Type **E** *Comment Status* **D** *PSE Detection*

Clarify text. Rewrite sentence "The PSE shall turn on power only on the same pairs as those used for two-pair detection."

SuggestedRemedy

change t: "The PSE shall only turn on power to the pairs on which a valid PD is detected."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This sentence is no longer needed now that "the PI" has been replaced with "a pair-set" in the first sentence in section 33.2.5:

"In any operation state, the PSE shall not apply power to a pair-set until the PSE has successfully detected a valid signature over that pair-set."

Cl **33** *SC* **33.2.5.0a** *P* **43** *L* **52** # 40

Dwelley, David — Linear Technology

Comment Type **T** *Comment Status* **D** *Connection Check*

"In addition, only tests that result in a voltage at the PSE PI that is within the Vvalid voltage range as specified..."

Vvalid is 2.8V-10V. This line as written blocks the use of 0V (i.e., one channel detecting while the other is idle) for Connection Check. This limits the way that connection check can be run.

SuggestedRemedy

Change text to: "In addition, only tests that result in a voltage at the PSE PI that is below Vvalid(max) as specified..."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.5.3** *P* **45** *L* **52** # 61

Schindler, Fred — Seen Simply

Comment Type **ER** *Comment Status* **D** *PSE Detection*

"A PSE shall accept as a valid signature a pair-set within a link section with ..."

The sentence construction is incorrect.

SuggestedRemedy

Consider,

"A PSE valid signature on a pair-set within a link section shall have the following characteristics, ..."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The sentence uses the same form that exists in the current standard. In addition, the suggestion uses the term "PSE valid signature" which is not correct.

Cl **33** *SC* **33.2.6** *P* **47** *L* **17** # 6

Bennett, Ken — Sifos Technologies, In

Comment Type **E** *Comment Status* **D** *PD Classification*

The sentence "PDs or PSEs which do not implement classification..." suggests that PDs don't have to implement classification, which is incorrect. All PDs provide class information via class current (including 0mA). Any PD which provides a bad class current or which operates beyond their class is not a conformant PD.

SuggestedRemedy

Omit "PDs or" at the beginning of the sentence.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This would be a maintenance request as this is existing text which I believe applies to class 0 PDs.

Cl **33** *SC* **33.2.6** *P* **47** *L* **30** # 69

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE Classification*

A definition for Vport_PSE-2p needs to be created.

SuggestedRemedy

A definition for Vport_PSE-2p needs to be created.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Vport_PSE-2p is a parameter whose limits are given in Table 33-11. This sentence assigns the minimum value of this parameter to V_PSE which is defined in 1.4.423 (see line 43).

Cl **33** *SC* **33.2.6** *P* **48-49** *L* **-** # 112

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **D** *PSE Classification*

Table 33-8 PSE and PD classification permutations is unduly difficult to read.

SuggestedRemedy

Replacement table suggested in yseboodt_d04_Table_33_8_v100.pdf
Content of the table identical to the one in D0.4

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Need document referenced in suggested remedy.

Cl **33** *SC* **33.2.6.1** *P* **50** *L* **9-10** # 86

Yseboodt, Lennart — Philips

Comment Type **T** *Comment Status* **D** *PSE Classification*

"If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2, Type 3 or
Type 4 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete."

This refers to Type 2 PSEs that use 1-Event Physical Layer classification and Data Link Layer classification.
This option does not exists for Type 3 or 4 PSEs, unless they are limited to Class 3 power or lower.

SuggestedRemedy

"If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2 PSE
treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

This is indeed in the 1-Event Physical Layer Classification section.

Cl **33** *SC* **33.2.7** *P* **53** *L* **38** # 17

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **X** *PSE Unbalance*

1. In previous work: 2mV was subjected to be reduced to 1mV pending final survey results. See page 4 at http://www.ieee802.org/3/bt/public/jan15/darshan_03_0115.pdf. Now we have it.

2. With 2mV currently in the specifications we have:
2.1 >10x margin. No need for it. It will never happen in real life.
2.2 >100% margin is sufficient (with 1mV).

3. Burden on PD is increased during compliance test with high current at short cable by ~1.6% with 2mV instead of 1mV. This 1.6% can be used by PD diodes at high current instead of PSE that don't need it.

4. At low current it affects MPS unbalance at short cable when Ideal diode is used. It doesn't create us problem with the proposed MPS method however for future best spec, if we will ever need low P2P_unb with Ideal diode bridge we can't go back and reduce PSE Vdiff to lower value. So it is better to kill potential problem when possible and not create new ones in the future.

5. This is all about optimizing the spec, as for who will get higher Vdiff budget at high current.

See attached Updated PSE Vdiff for 802.3bt D0.4, darshan_02_0515.pdf for details.

SuggestedRemedy

To Reduce PSE Vdiff in Table 33-11 to 1mV.

Proposed Response *Response Status* **W**

Would like to hear from system vendors (switch manufacturers) on this topic.

Cl **33** *SC* **33.2.7** *P* **54** *L* **33** # 31

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PSE Power*

In Table 33-11 item 10 (TLIM), there is a missing reference at the additional information column.
In addition to 33.2.7.7, there are additional clauses that are relevant for TLIM such as 33.2.7.1 which defined behavior of power removal when pair-set voltage no longer meets Vport_PSE-2P spec.

SuggestedRemedy

Change additional information column from "See 33.2.7.7"

To:
See 33.2.7.7 and 33.2.7.1.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

TLIM is not referenced is section 33.2.7.1.

Cl **33** *SC* **33.2.7** *P* **54** *L* **36** # 70

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE Power*

This parameter applies to all Types. So does parameter items 13, 14, 15,16, 22, and 24. See related comment on item 11.

SuggestedRemedy

List 1,2,3,4 for valid Types in the above items.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Item 11 should have 1,2,3,4 listed for valid Types.

The other items you list need to be considered for 4-pair operation.

Cl **33** *SC* **33.2.7** *P* **54** *L* **36** # 74

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE Power*

Pcon is the average power of the PI. This may be equal to Pclass or it may be equal to the combined Pclass of each pair-set for dual-signature PDs. This applies to all Types.

SuggestedRemedy

Reference the section that covers these exceptions. List all Types.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This topic needs to be addressed in a Single and Dual PD presentation…

Cl **33** *SC* **33.2.7** *P* **54** *L* **9** # 101

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **D** *PSE Power*

Per Table 33-11: Type 3,4 PSE must deliver 0.5*Pclass / Vport_PSE-2P.
In case the the PSE power over 2P then Icon-2P is off by factor 2.

SuggestedRemedy

Split Type 3,4 up into Type 3,4 in 2P mode and Type 3,4 in 4P mode.
The 2P mode: Icon-2p(min) = Pclass / VPort_PSE-2P
The 4P mode: Icon-2p(min) = 0.5*Pclass / VPort_PSE-2P

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Only Type 3 can act in 2P mode.

Split Type 3 up into Type 3 in 2P mode and Type 3 in 4P mode.
The 2P mode: Icon-2p(min) = Pclass / Vport_PSE-2P
The 4P mode: Icon-2p(min) = 0.5*Pclass / Vport_PSE-2P

Cl **33** *SC* **33.2.7** *P* **55** *L* **26** # 19

Darshan, Yair — Microsemi

Comment Type **T** *Comment Status* **D** *PSE Unbalance*

Table 33-11 item Item 20, Iunb_ptp:
This parameter is redundant for PSE specification after PSE specifications was concluded on March meeting with the new items:
Table 33-11 item 4a: Icon_2P-unb and clause 33.2.7.4a.
It may be used in PD spec Table 33-18 but is not needed for PSE spec.

SuggestedRemedy

Option 1:
a) Remove Iunb_p2p from Table 33-11 item 20. OR

b) Move this parameter to Table 33-18 new item 14, with the following details:
Parameter: Pair to Pair current unbalance of pairs with the same polarity.
Symbol: Iunb_ptp
Unit: %
Value max: TBD.
Additional information:
See 33.2.7.10.
Add sub-claues 33.2.7.10:
Iunb_ptp=(I1-I2)/(I1+I2).
I1, I2 are the pairs current of the same polarity.
I1 and I2 are measured at the maximum operating PD class power for class TBD1 to Class TBD2.
Editor note: To complete the PD PI Pair to Pair Unbalance requirements and add it to this clause.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Remove Iunb_p2p.

Cl **33** *SC* **33.2.7.2** *P* **55** *L* **25** # 7

Bennett, Ken — Sifos Technologies, In

Comment Type **ER** *Comment Status* **D** *PSE Unbalance*

Table 33-11, Item 20. The specification for Iunb_ptp has been superceeded by item 4.1 and section 33.2.7.4a.

SuggestedRemedy

Remove the Iunb_ptp section from item 20.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 19

Cl **33** *SC* **33.2.7.4** *P* **56** *L* **34** # 8

Bennett, Ken — Sifos Technologies, In

Comment Type **TR** *Comment Status* **D** *PSE Power*

33.2.7.4 is the additional information for item 4 in table 33-11 (Icon-2P). The Icon_2P equation (0.5*PClass/Vport_2P) for type 3 and 4 in table 33-11 is based upon a perfectly balanced connection, and does not include the additional pair-set current that would be necessary to maintain PClass in an unbalanced connection (due to E2ERunb).

The additional information (Section 33.2.7.4) currently only addresses Ipeak-2P, and it does consider an unbalanced connection, using the (1+K) factor. However, Ipeak-2P described Equation 33-4 includes pair-set values for the PSE and PD, and it is unclear whether the PD pair-set value in 33-4 will also include the K factor (which would result in including K twice).

SuggestedRemedy

Change section 33.2.7.4 as follows:

33.2.7.4 Continuous output current capability in the POWER_ON state

Icon-2P in table 33-11 is specified for a balanced system. When end-to-end unbalance is present, the PSE minimum requirement is:

Icon-2P_unb = (1+K) x (Icon-2P)33-4

Where K is the factor due to the "system end to end pair-to-pair unbalance effect". K=0 for two pair systems and K=TBD for four pair systems.

In addition to ICon-2P_unb, the PSE shall support the following AC current waveform parameters, while within the operating voltage range of VPort_PSE:

IPeak-2P minimum for TCUT minimum and 5 % duty cycle:

[Editorial note: the equation below is unformatted. The only difference relative to Equation 33-4 in 802.3at is the "N" factor]

Ipeak-2P= N×{(Vpse-[SQR_ROOT[Vpse^2-4N(Rchan)(Ppeak_PD)])/(2N(Rchan))} 33-5

Where:
Ipeak-2P: is the PSE minimum peak current requirement per pair-set in a balanced system
VPSE: is the PSE voltage at the PSE PI as defined in 33.1.4
RChan: is the channel loop resistance as defined in 33.1.4; this parameter has a worst-case value of RCh, defined in Table 33-1
N: N = 1 for 2-pair power, N = 0.5 for 4-pair power
PPeak_PD: is the peak power a PD may draw for its class; see Table 33-18.

Ipeak-2P is specified for a balanced system. When end-to-end unbalance is present, minimum PSE pairset requirement is:

Ipeak-2P_unb = (1+K) x (Ipeak-2P)33-6

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Yair and Ken to work together to find agreement on new text.

Cl **33** *SC* **33.2.7.4** *P* **56** *L* **34** # 20

Darshan, Yair — Microsemi

Comment Type **T** *Comment Status* **D** *PSE Power*

Equation 33-4 parameters need some updates:
1. PPEAK_pd_2P need to be defined as 0.5*Pclass for classes 5 to 8 (It is half the total power).
2. K is different number for Type 3 and 4 systems.
3. K is derived by simulation of E2EP2PIunb with the same data base we used to define Icon-2P_Iunb but now PD power is Ppeak PD which is defined by Equation 33-12.
4. See derivation of values for K in darashan_03_0515.pdf

SuggestedRemedy

(a) Change from:
PPeak_PD-2P is the peak power a PD may draw per pair-set for its class; see Table 33–18.

To:
PPeak_PD-2P is the peak power a PD may draw per pair-set for its class; see Table 33–18. For classes 5-8, PPeak_PD-2P=0.5*Pclass_PD.

(b) Change from:
K is the related to “system end to end pair-to-pair unbalance effect”.
K=0 for two pair systems and K=TBD for four pair system.

To:
K was set at the system operating point were maximum Ipeak-2P is obtained due to “system end to end pair-to-pair unbalance effect”.
K=0 for two pair systems (Type 1 and 2).
K=0.3 for Type 3 systems.
K=0.09 for Type 4 systems.
Note: Meeting Ipeak_2P maximum value is guranteed by the PD by meeting PD PI Pair To Pair Unbalance requirements in clause TBD and by Peak_PD-2P defined by Equation 33-12.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Yair and Ken to work together to find agreement on new text.

Cl **33** *SC* **33.2.7.4** *P* **56** *L* **43** # 3

Maguire, Valerie Siemon

Comment Type **T** *Comment Status* **D** *PSE Power*

Clarify type of unbalance (i.e. resistance or current)

SuggestedRemedy

Replace "pair-to-pair unbalance effect" with "pair-to-pair resistance unbalance effect"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

I believe this is current unbalance

Replace with "pair-to-pair current unblance effect"

Cl **33** *SC* **33.2.7.4a** *P* **57** *L* **10** # 63

Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **D** *Editorial*

We should determine if the IEEE has rules for variable subscripts. Sometimes we use lower case, upper case, or a combination if cases.

SuggestedRemedy

We should review the conventions and adapt variables to fit them.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Cl **33** *SC* **33.2.7.4a** *P* **57** *L* **17** # 72

Schindler, Fred Seen Simply

Comment Type **E** *Comment Status* **D** *PSE Unbalance*

This section only applies to Types 3 and 4.

SuggestedRemedy

Recommend calling Types out that this section applies to near the beginning of this section to reduce text that a reader must parse to discover what is covered.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Need actual text…

Cl **33** *SC* **33.2.7.7** *P* **59** *L* **19-2** # 123

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PSE Power*

"A PSE may remove power from a pair-set of a PI if the pair-set current..."

In case a PD is drawing too much current, this can double the shutdown time.
First one pairset exceeds, and gets disconnected after Tlim.
Then the full current of the PD gets transferred to the other pairset, which also goes down after Tlim. Total shutdown time is doubled.

Some textual clarifications added + distinction between single and dual signature PD.

SuggestedRemedy

"A PSE may remove power from both pair-sets of a PI if any pair-set current meets or exceeds the 'PSE lowerbound template'
in Figure 33-14, when connected to a single signature PD.
A PSE may remove power from a pair-set of a PI if its pair-set current meets or exceeds the 'PSE lowerbound template'
in Figure 33-14, when connected to a dual signature PD.
Power shall be removed from both pair-sets of a PI before any pair-set current exceeds the 'PSE upperbound template' in Figure 33-14,
when connected to a single signature PD.
Power shall be removed from a pair-set of a PI before its pair-set current exceeds the 'PSE upperbound template' in Figure 33-14,
when connected to a dual signature PD."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

I think we can simplify this…

SS: may remove power from both if lower template exceeded, shall remove power from both if upper template exceeded.

DS: may remove power from the pair-set or both if lower template exceeded, shall remove from the pair-set or both if upper template exceeded.

Cl **33** *SC* **33.2.9.1.1** *P* **62** *L* **28** # 71

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE MPS*

The Task Force should determine whether new Types may use AC MPS.

If permited several parameters may need to be recheck to ensure interoperability. For example, the minimum VPSE may need to drop from 52V to a lower value.

SuggestedRemedy

Determine if the Task Force wants to have new Types use AC MPS and adjust text accordingly.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We will ask the task force. I expect the answer to be no.

If no: Add that Type 1 and Type 2 PSEs are the only PSEs that can do AC MPS.

Cl **33** *SC* **33.3.1** *P* **64** *L* **38** # 105

Yseboodt, Lennart — Philips

Comment Type **TR** *Comment Status* **D** *PD PI*

"The PD shall be capable of accepting power on either or both of two sets of PI conductors."
This statement is valid for Type 1 & Type 2.
Type 3 and 4 PDs are required to support 4P power.
This text should be in line with Table 33-13a and we should use the term pair-set.

SuggestedRemedy

Replace line by:
Type 1 and Type 2 PDs shall be capable of accepting power on either or both pair-sets.
Type 3 and Type 4 PDs shall be capable of accepting power on either and both pair-sets.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Are we adding a requirement to Type 1 and Type 2 PDs (they were only required to accept power on either pair-set, we have added both)?

What is the difference between "either or both" and "either and both"?

Cl **33** *SC* **33.3.1** *P* **64** *L* **38** # 104

Yseboodt, Lennart — Philips

Comment Type **T** *Comment Status* **D** *PD PI*

The term pair-set is only defined for the PSE, but also used and valid for a PD.

SuggestedRemedy

Insert "A pair-set in a PD refers to either of the conductor sets." after "The two conductor sets are named Mode A and Mode B."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We agreed in the last comment cycle to add the definition of pair-set to section clause 1.4.

Section 1.4 was not updated accordinly in D0.4.

We accepted “pair-set” and its definition as referring to either of the two valid 4-wireconnections as
listed in 33.2.3.

Do we need this if the definition exists? Yes, maybe for clarification

Cl **33** *SC* **33.3.1** *P* **64** *L* **53** # 142

Jones, Chad — Cisco

Comment Type **T** *Comment Status* **D** *PD PI*

Maintenance Request #1274 on behalf of George Zimmerman, CME Consulting/LTC

Text in the existing standard is ambiguous and is inconsistent with terminations and usage commonly found in Ethernet equipment. The intent is to require PDs to be able to withstand application of common-mode PoE voltage. Application of 57V DC voltages in across the pins corresponding to the two pairs twisted differentially to form a balanced pair of the link segment would run a DC current across the transformer windings commonly found in BASE-T Ethernet equipment and burn them out.

SuggestedRemedy

Change: The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.
To:The PD shall withstand any common-mode voltage from 0 V to 57 V applied to any two sets of two pins at the PI indefinitely without permanent damage. The two pins in each set shall correspond to the balanced twisted wire pairs of the connected link segment.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This should be clarified. Can we use the definition of pair-set make this simpler?

Cl **33** *SC* **33.3.2** *P* **65** *L* **-** # 109

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PD Types*

Table 33-13a lists the maximum PD power, but for Type 3 (51W) and Type 4 (71.3W) it does
not take extended power into account.

SuggestedRemedy

Possible solutions:
Replace power values with a "Highest Class" column (preferred).
That column would look like
PD Class
* 0-3
* 4
* 0-3
* 4 (line removed)
* 4-6
* 7-8
See replacement table suggestion in yseboodt_D04_Table_33-13a_v100.pdf

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Classes are a better way to refer to power levels. The actual power levels should only be referred to once (Pclass_pd)

Cl **33** *SC* **33.3.2** *P* **65** *L* **37** # 107

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PD Types*

Table 33-13a, column DLL classification, Type 3 / 13W row, content = "Yes".
There is no reason for a Type 3 13W (Class 3 max) PD to have mandatory DLL support.

SuggestedRemedy

Replace "Yes" by "Optional" in the column "Data Link Layer Classification",
row "Type 3, 13W".
See replacement table suggestion in yseboodt_D04_Table_33-13a_v100.pdf

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Possible OBE by comment # 109

make change if comment #109 is not resolved with a change to this text.

Cl **33** *SC* **33.3.2** *P* **65** *L* **49** # 41

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *PD Types*

Table 33-13a, Note 2: "Needs 4-Pair Identification before enabling 4-pair power. See Section TBD for details."

Enabling 4-pair power is a PSE function, not a PD function.

SuggestedRemedy

Remove Note 2.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace "Yes" in 4-pair Capable column with "Mandatory" for all Type 3 or Type 4 rows.

Replace "Allowed" in 4-pair Capable column with "Optional" for all Type 1 and Type 2 rows.

Remove note 2. Need to add 4PID information to PSE section.

Cl **33** *SC* **33.3.2** *P* **66** *L* **12** # 98

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PD Power*

Line 9 says: The maximum power a PD expects to draw from a PSE is P Class_PD max as defined in Table 33-18.
Purpose of this statement is unclear. If the reference point is the PSE, then the power is Pclass.
If the reference point is the PD PI, the it is Pclass_pd for class 0-5 & 7 and Pclass for classes 6 and 8.

SuggestedRemedy

Remove altogether or replace by:
The maximum power a PD expects to draw from a PSE is P_Class at the PSE PI as defined in Equation 33-3 and Table 33-7.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Remove this sentence. This information is covered in Table 33-18 and section 33.3.7.2.

Cl **33** *SC* **33.3.2** *P* **66** *L* **4-10** # 108

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PD Types*

"Type 3 PDs operating up to a max power draw corresponding to Class 3 or less implement both 1-Event
Physical Layer Classification and Data Link Layer classification (see 33.6) and advertise a 1-Event class
signature of 0,1,2, or 3."

There is no reason for a Type 3 13W (Class 3 max) PD to require DLL support.

SuggestedRemedy

"Type 3 PDs operating up to a max power draw corresponding to Class 3 or less implement a minimum of
1-Event Physical Layer classification and advertise a 1-Event class signature of 0, 1, 2, or 3.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Agree. Class 0-3 PDs should not be required to support LLDP.

Cl **33** *SC* **33.3.3.3** *P* **68** *L* **16-3** # 91

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **D** *PD State Diagram*

Variable is renamed from pse_dll_power_type to pse_dll_power_level,
but it describes the type of the PSE connected.
pse_dll_power_type is a more apt name.

SuggestedRemedy

Rename pse_dll_power_level to pse_dll_power_type or to pse_dll_type

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Leave name as pse_dll_power_level

Change description to: "A control variable output by the PD power control state diagram (Figure 33-3) that indicates the power level of the PSE by which the PD is being powered.

Values: 1: The PSE is delivering class 3 power or less.
2: The PSE is delivering class 4 power.
3: The PSE is delivering class 5 or class 6 power.
4: The PSE is delivering class 7 or class 8 power.

Cl **33** *SC* **33.3.3.3** *P* **68** *L* **17** # 51

Beia, Christian STMicroelectronics

Comment Type **E** *Comment Status* **D** *PD State Diagram*

The variable name change from pse_dll_power_type to pse_dll_power_type is unnecessary and does not correspond to the name in the state diagram on page 111 (clause 33.6.3.5)

SuggestedRemedy

restore the variable name "pse_dll_power_type" instead of "pse_dll_power_level"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 91.

Cl **33** *SC* **33.3.3.4a** *P* **69** *L* **12-1** # 94

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PD State Diagram*

"Type 3 MPS: A control variable that indicates to the PD the Type of PSE to which it is connected.
This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use.
Values:
TRUE: The PSE uses Type 3 MPS requirements.
FALSE: The PSE uses Type 1 MPS requirements."

Bad variable name. Type description incomplete.

SuggestedRemedy

"short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected.
This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use.
Values:
TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

"short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected.
This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use.
Values:
TRUE: The PSE uses Type 3, 4 MPS timing requirements.
FALSE: The PSE uses Type 1, 2 MPS timing requirements."

Cl **33** *SC* **33.3.5.2** *P* **75** *L* **21** # 42

Dwelley, David — Linear Technology

Comment Type **TR** *Comment Status* **X** *PD Classification*

Table 33-16a: class mapping will cause LT legacy PDs to motorboat. Reversing classes 7 and 8 looks weird but will improve interoperability in the field.

SuggestedRemedy

Reverse class_sig_B mappings for classes 7 and 8:
class 7: class_sig_B: 3
class 8: class_sig_B: 2

Proposed Response *Response Status* **W**

Would like to hear group's opinion…

Cl **33** *SC* **33.3.5.2** *P* **75** *L* **33** # 56

Beia, Christian — STMicroelectronics

Comment Type **TR** *Comment Status* **D** *PD Classification*

Table 33-17.
Among the PD Classification electrical requirements, the long first class event definition, used to determine the PSE MPS capability, is missing. The PD TLCF definition is necessary because it is mentioned in table 33-19a.
The Auto class signature timing in 33-17a (TACS) cannot be used, as it specifically refers to the Autoclass feature and not to MPS.
However the timing requirements are the same for both (in the range of Tpdc_max to TLCF_min as specified in table 33-10), with some grey area margin.
To keep PD design simple (5% clock accuracy) a grey area margin of 1ms is suggested.

SuggestedRemedy

Add a line in Table 33-17 for:
Item: "7"; parameter: "Long first class event timing"; Symbol: "TLCF"; Units:"ms"; Min: "76ms"; Max: "84ms"; Additional information: "See 33.3.8"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Added as much range as possible while still keeping some margin. Added PD to the symbol name to differentiate from the PSE variable.

Add a line in Table 33-17 for:
Item: "7"; parameter: "Long first class event timing"; Symbol: "TLCF_PD"; Units:"ms"; Min: "75.5ms"; Max: "84.5ms"; Additional information: "See 33.3.8"

Cl **33** *SC* **33.3.5.3** *P* **76** *L* **29** # 73

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PD Classification*

Some of the requirements for Autoclass need to be covered.

SuggestedRemedy

Add requirements for the time over which the measurement is averaged. Suggest a 1-second sliding window is used that is valid within TAUTO_PD1 to TAUTO_PD2.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We should make it clear that the power drawn during the timeframe Tauto_pd1 to Tauto_pd2 is used to determine a new Pclass_pd (which has a definition of how it is measured in 33.3.7.2).

Cl **33** *SC* **33.3.5.3** *P* **76** *L* **37** # 54

Beia, Christian — STMicroelectronics

Comment Type **TR** *Comment Status* **D** *PD Classification*

Table 33-17.
The autoclass signature timing specification TACS introduces an unnecessary design burden to the PD, since +-3ms window over a 80ms timer requires a clock accuracy better than +-4%.
This is the only parameter requiring such a high accuracy of PD internal clock.
Since this PD behavior is a response to a PSE long finger, tentatively specified in table 33-11 as TLCF=85ms min, the requirement for TACS can be relaxed still maintaining a good margin (grey area) on PSE timings (1ms after Tpdc_max and before TLCF_min)

SuggestedRemedy

Change TACS min value to 76ms and max value to 84ms.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change TACS min value to 75.5ms and max value to 84.5ms.

Cl **33** *SC* **33.3.7** *P* **77** *L* **27-3** # 103

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PD Power*

The minimum input voltage for a PD VPort_PD-2P(min) is based on the highest power class of the Type.
PDs in Class 1,2,5 and 7 will never see a voltage as low as currently specified.
Hence their design calls for an input voltage operating window that is unnecessarily wide.
Also, the PD Type alone does not determine the minimum input voltage: eg. a Type 3 PD/15W can still
get a 37.0V input voltage from a Type 1 PSE.

SuggestedRemedy

Base minimum PD voltage on PD assigned class rather than Type.
VPort_PD-2P(min) =
Class 1: 42.2V
Class 2: 40.8V
Class 3: 37.0V
Class 4: 42.5V
Class 5: 44.4V
Class 6: 42.5V
Class 7: 43.0V
Class 8: 41.2V

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Interesting idea…would like to hear the group's opinion.

Cl **33** *SC* **33.3.7** *P* **78** *L* **37** # 25

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PD Power*

Table 33-18 item 5 and 6.
Peak operating power for class 5 and 6. can be 1.11*Pclass_PD as well due to the fact that class 6 is 2xType 2 power and it is higher than class 5.

Class from analysis done in darshan_03_0515.pdf, class 7 and 8 may also use equation 33-12 as is.

SuggestedRemedy

Replace TBDs in Table 33-18 item 7 for class 5 -8 with 1.11*Pclass_PD.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Will wait to see referenced presentation.

Cl **33** *SC* **33.3.7** *P* **79** *L* **15** # 26

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PD Power*

1)Table 33-18 item 11 Von and Voff:
PD Type need to be 1,2,3,4.
2) Typo in additional information.

SuggestedRemedy

1) Change PD Type from 1,2, to 1,2,3,4 for both Von and Voff.
2) Change 33.3.7.133.3.7.1 to 33.3.7.1.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Proposal "1)" is possibly OBE by comment # 126.

Proposed accept for proposal "2)"

Cl **33** *SC* **33.3.7.3** *P* **80** *L* **46** # 27

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PD Power*

It is not clear from Table 33-18 item 9 that the Cport_min=5uF is per pair set.

SuggestedRemedy

Add the following text at the end of 33.3.7.3:
Cport_min is the the minimum value of Cport seen by an attached PSE on two twisted pairs.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

There is already a note at the end of 33.3.7.3 that address Cport per pair set. This note should be altered to make the meaning clear.

Cl **33** *SC* **33.3.8** *P* **84** *L* **24** # 95

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **D** *PD MPS*

"The MPS is made up of current draw equal to or above Iport_MPS for a ..."

SuggestedRemedy

"The MPS consists of current draw equal to or above Iport_MPS for a ..."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is existing langauge and I believe it is clear enough.

Cl **33** *SC* **33.3.8** *P* **85** *L* **13** # 35

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PD MPS*

The Iport_MPS conditions for Type 1-4 are not specified.

SuggestedRemedy

In Table 33-18 item 1 for PD Type 1-4:
Add to th econdition column:
for Single Signature PD and class 0-4.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

There will be presentation(s) including baseline text on this topic in May. Hold comment until then.

Cl **33** *SC* **33.3.8** *P* **85** *L* **1-4** # 96

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *PD MPS*

The note is only correct for PDs that draw Iport continuously.
PDs that make use of duty cycling will need to take measures also with smaller capacitors.
PDs that draw just Iport_mps with the minimum duty cycle (all types) also get in trouble with even the smallest allowed Cport.

SuggestedRemedy

Replace note by:
PDs may not be able to meet the I Port_MPS specification in Table 33-19 during the maximum allowed port
voltage droop (V Port_PSE max to V Port_PSE min with series resistance R Ch).
Such a PD should increase its I Port min or make other such provisions to meet the Maintain
Power Signature.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The note is informative and thus making it broader reaching is not a problem. I think it is a good idea for PD designers to consider the effect of PSE behavior on their PD.

However, the 180uF number seems to work and I have not heard any issues with it in implemenations that use pulsing.

Cl **33** *SC* **33.3.8** *P* **85** *L* **15** # 28

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PD MPS*

Table 33-18 do not cover MPS input current requirements for PDs that are need to be supported by Type 3 and 4 PSEs under P2P current balanced and unbalanced conditionall.

SuggestedRemedy

Updated Table 33-18 item 1 per proposal attached in darashan_01_0515.pdf.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Will hold comment until presentation(s) on this topic.

Cl **33** *SC* **33.3.8** *P* **85** *L* **15** # 36

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *PD MPS*

Type 3/4 MPS has become more complicated and the 22mA number is obsolete

SuggestedRemedy

Rewrite spec based on results of joint presentation in May

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Will hold comment until presentation(s) on this topic.

Cl **33** *SC* **33.4.9.13** *P* **97** *L* **5** # 137

Shariff, Masood CommScope

Comment Type **T** *Comment Status* **D** *AES*

Connector RL is not correct for Category 5 connectors.

SuggestedRemedy

Use the following for the first row:

10/100/1000BASE-T 1 MHz <=f <= 31.5 MHz 30 dB
20 MHz < f <= 100 MHz 20 - 20 log(f/100)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Need expert opinion…

Cl **33** *SC* **33.6.3.2** *P* **105** *L* **35-4** # 76

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *DLL*

PD_DLLMAX_VALUE is still TBD for Class 5 and up. Can now be filled out since PD powers are known.
Note: pd_max_power for class 8 is still TBD pending another comment.

SuggestedRemedy

PD_DLLMAX_VALUE =
pd_max_power 5 399
pd_max_power 6 510
pd_max_power 7 620
pd_max_power 8 TBD

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.6.3.2** *P* **105** *L* **35-4** # 77

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *DLL*

For Type 4 the Type max power is 99.9W
LLDP is a way for the PD to request power beyond what L1 classification can deliver.
A PSE that sources 99.9W (@52V) will deliver 76.8W at the PD PI (6.25 ohm channel).

SuggestedRemedy

PD_DLLMAX_VALUE =
pd_max_power 8 768

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

No real PSE will be able to supply this power as some margin is needed in the power limit.

Cl **33** *SC* **33.6.3.2** *P* **105** *L* **42-5** # 78

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *DLL*

PD_INITIAL_VALUE is still TBD for Class 5 and up. Can now be filled out since PD powers are known.

SuggestedRemedy

PD_DLLMAX_VALUE =
pd_max_power 5 <= 399
pd_max_power 6 <= 510
pd_max_power 7 <= 620
pd_max_power 8 <= 713

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.6.3.2** *P* **106** *L* **13-1** # 122

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *DLL*

PSE_INITIAL_VALUE is still TBD for Class 5 and up. Can now be filled out since PD powers are known.

SuggestedRemedy

PSE_INITIAL_VALUE =
mr_pd_class_detected 5 399
mr_pd_class_detected 6 510
mr_pd_class_detected 7 620
mr_pd_class_detected 8 713

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.8.3.4** *P* **127** *L* **20** # 5

Maguire, Valerie Siemon

Comment Type **T** *Comment Status* **D** *Unbalance*

Clarify type of unbalance (i.e. resistance or current)

SuggestedRemedy

Replace "PSE and PD channel unbalance" with "PSE and PD channel current unbalance"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.