Cl **33** *SC* **33.1.4** *P* **22** *L* **6** # 4

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X** *Cabling*

Maintenance Request #1271, on behalf of GEOFF THOMPSON, GRACASI S.A./LINEAR TECHNOLOGY

Move as much of the cabling specification to cabling documents as possible. (This RR was entered as a tracking mechanism for Thompson Comment #59 against P802.3REVbx/D2.0 during initial WG ballot. Resolution of this comment was given over to P802.3bt as they will have Cl 33 open.)

SuggestedRemedy

See attached sheet for proposed new text.
(http://www.ieee802.org/3/maint/requests/maint_1271.pdf, page 2)
A number of these changes have already been adopted. The two remaining changes are:
Replacing the first sentence in 33.1.4 with:
"A power system, consists of a single PSE, a single PD and the link section connecting them. A power system is
characterized as Type 1 or Type 2 by lowest type number of the PSE or PD in the system, see Table 33–1."
and replacing the first paragraph of 33.1.4.1 with (as well as changing the title of the subclause to "Cabling requirements"):
"The supply of power over the data connection is intended to operate with no additional requirements to the cabling that is
normally installed for data usage. This is approximately true but may require some further attention. Power at Type 1
power levels may be transmitted over all specified premises cabling without further restrictions. Higher power levels may
require heavier gauge conductors than are found in Class C/Category 3 cabling and (more uncommonly) in some lighter
gauge Class D or better cable. The requirements for Type 2 are met by Category 5 or better cable and components as
specified in ANSI/TIA/EIA-568-A."

Proposed Response *Response Status* **W**

Waiting for Yair to review.

Yair to review by September, or these changes will be accepted.

To be held open.

Cl **33** *SC* **33.2.4.3** *P* **34** *L* **29** # 176

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **X** *Pres: PSE SD*

To allow for PSEs that perform connection check before, during, between, or after detection, a new constant is needed to define the disparate pathways these PSEs take through the state diagram and their associated timing requirements.

SuggestedRemedy

Add constant "PSE_CC_DET_SEQ" as follows:

PSE_CC_DET_SEQ
A constant indicating the sequence in which the PSE performs connection check and detection.
Values: 1: Connection check and detection performed simultaneously
2: Connection check performed prior to detection
3: Connection check performed between detections
4: Connection check performed after detection

Proposed Response *Response Status* **W**

Wait for presentation.

Cl **33** *SC* **33.2.4.4** *P* **33** *L* **43** # 255

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **X** *Pres: Inrush*

"legacy_powerup:
This variable is provided for PSEs that monitor the PI per pair set voltage output and use that information to indicate the completion of PD inrush current during POWER_UP operation. Using only the PI pair set voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed TInrush-2P period is recommended. A variable that is set in an implementation-dependent manner.
Values:TRUE:The PSE supports legacy power up; this value is not recommended.
FALSE:The PSE does not support legacy power up. It is highly recommended that new equipment use this value."

Doesn't this only apply to 2 pair PSEs? At a minimum, there should be no legacy-power-up 4pair PSEs.

SuggestedRemedy

insert "two pair" so it reads, "This variable is provided for two-pair PSEs"

Add to TRUE: (after 'not recommended'), "and is not allowed for 4-pair PSE operation."

Proposed Response *Response Status* **W**

Wait for Yair's Presentation.

Cl **33** *SC* **33.2.4.4** *P* **35** *L* **38** # 71

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *Pres: PSE SD*

IPort-2P is also per pair set
original text:
"IInrush-2P
Output current per pair set during POWER_UP (see Table 33-11 and Figure 33-13).
IPort-2P
Output current (see 33.2.7.6)."

SuggestedRemedy

"IPort-2P
Output current per pair set (see 33.2.7.6)."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We need to be careful. We should not change the Type 1/2 State Diagram variables if we are going to leave that diagram as is. We need to create new variables for Type 3/4.

Group to discuss.

Cl **33** *SC* **33.2.4.4** *P* **35** *L* **45** # 138

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PSE Inrush*

There is missing word "only" in the text:
The text "This variable is provided for PSEs that (only)monitor the per pair set voltage output and use that information ....".

The above text should match lines 46-47 that do use the word "only" which is the correct intent:
lines 46-47 says:
Using only the PI pair set voltage information may be insufficient..."

SuggestedRemedy

Repalce The text "... for PSEs that monitor the per pair set voltage output and use that information ...."
with:
"... for PSEs that monitor only the per pair set voltage output and use that information ...."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Yair, if we add the word only, then this variable would not apply to PSEs that use more than the output voltage. Thus, your PSE would not be allowed to leave inrush early. I don't think this is what you want.

Cl **33** *SC* **33.2.4.4** *P* **35** *L* **52** # 111

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Inrush*

legacy_powerup state variable definition.

This refers to a commonly implemented inrush behavior associated with 802.3af and many 802.3at PSE's whereby inrush is deemed completed as soon as port voltage is in a nominal range. This behavior is not recommended in 802.3at because Type-2 PSE's are allowed to set Type-2 parameters for Icut and Ilim upon the completion of inrush meaning all PD's that delay or stagger inrush loads might not experience inrush current limiting at all resulting in effective inrush currents at 684mA or higher. Type-3 and Type-4 may allow even higher inrush currents to Type-1 / Type-2 PD's if they implement the "traditional" legacy_powerup. This should be avoided.

SuggestedRemedy

legacy_powerup....

FALSE: The PSE does not support legacy power up. Type-3 and Type-4 PSEs shall use this value. It is highly recommended Type-1 and Type-2 PSEs use this value.

Proposed Response *Response Status* **W**

Wait for Yair's Inrush presentation.

Cl **33** *SC* **33.2.4.4** *P* **36** *L* **49** # 133

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *Pres: PSE SD*

At the system level we need to know if we have over load condition over pair set A and pair set B.
The current text says "...over at least one pair set.." means that if we know the status on pair set A it is sufficient and it is not.
What about the status of pair set B?
As a result, the variable ovld_detected text need to be updated.

SuggestedRemedy

Change from:
A variable indicating if the PSE output current over at least one pair set has been in an overload condition (see 33.2.7.6) for…"

To:
A variable indicating if the PSE output current over 1st pair-set or 2nd pair set has been in an overload condition (see 33.2.7.6) for…"

Proposed Response *Response Status* **W**

waiting for presentation

Cl **33** *SC* **33.2.4.4** *P* **39** *L* **5** # 72

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Pres: Types*

A Type 4 PSE is distinct from a Type 3 PSE in ways other than power (Vpse min, polarity, must implement 4P).
A Type 4 PSE that is powering below class 7 should still be a Type 4 PSE.
Currently Table 33-3 requires a Type 4 PSE to have class_num_events = 5, possibly restricting it to Class 7 and 8.

(This is an updated version of the comment against D1.0).

Presentation on this topic "Type 4 Classrange"

SuggestedRemedy

Add class_num_events 1, 2 and 4 also for Type 4.

Proposed Response *Response Status* **W**

Waiting for Presentation

Cl **33** *SC* **33.2.4.6** *P* **41** *L* **17** # 175

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **D** *PSE SD*

Values for variable "PD_signature" within the do_connection_check function do not match the values shown in Section 33.2.4.4 (see page 34, line 40).

SuggestedRemedy

Delete the "Invalid" value.

Change the value "Open_circuit" as follows:

"Open_Circuit: Open circuit detected on both pairsets."

Modify the value "Single" to be the default case and applicable to PDs that operate over a single pairset:

"Single: Either connection check has not been performed or a single-signature PD configuration is connected through one or both of the two pairsets at the PI."

Corresponding comment entered against the variable values flagged with DW1

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 7.

Cl **33** *SC* **33.2.4.6** *P* **41** *L* **22** # 124

Bullock, Chris Cisco Systems

Comment Type **TR** *Comment Status* **D** *PSE SD*

If connection check is performed prior to detection, a result of invalid will keep you from entering detection state. As such, an result of "open_circuit on one of the pair sets" should not cause an "invalid" result.

SuggestedRemedy

replace "open_circuit on one of the pair sets" to "open_circuit on both of the pair sets"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 7.

Cl **33** *SC* **33.2.5.0a** *P* **53** *L* **34** # 178

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **X** *Pres: PSE SD*

In Table 33-3a, under Additional Information for Item 2, it's stated that "Applies only when connected to a single-signature PD."

This may not be true if we allow connection check to occur between the 2 detections and don't want to create new timing parameters.

SuggestedRemedy

Presentation forthcoming to cover this and other aspects of connection check.

Proposed Response *Response Status* **W**

Wait for presentation

Cl **33** *SC* **33.2.7.5** *P* **72** *L* **50** # 104

Jones, Chad Cisco

Comment Type **T** *Comment Status* **D** *Pres: Inrush*

HOLD OVER for Ken Bennett:
There is a recommendation that POWER_UP mode persist for the complete duration of TInrush in section 33.2.7.5 of the existing standard. Commensurately, there is a recommendation against using LEGACY POWER_UP in section 32.2.4.4. This is because legacy power-up can end POWER_UP mode prior to the end of PD Inrush.
The result of an early exit of POWER_UP mode is that current is not limited to the levels in figure 33-13, and inrush current could exceed expected values for a PD, potentially damaging an existing Type 1 or Type 2 PD. Type 3 and Type 4 PSE's could deliver higher currents during PD Inrush in this scenario, increasing the probability of damage to a legacy PD.
The recommendations used in the existing standard have been applied to Type 3 and Type 4 PSE's in the draft. The suggested remedy makes it a requirement for Type 3 and Type 4 PSE's. For reference, the existing text is shown below:
However, for practical implementations, it is recommended that the POWER_UP mode on a pair set persist for the complete duration of TInrush-2P, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

SuggestedRemedy

Change the text to:
However, for practical implementations, it is recommended that POWER_UP mode in Type 1 and Type 2 PSE's persist for the complete duration of TInrush-2P, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior. Type 3 and Type 4 PSE's shall remain in POWER_UP mode until the Tinrush_2P period in table 33-11 is met.

Proposed Response *Response Status* **O**

Waiting for Yair's presentation.

Cl **33** *SC* **33.2.7.5** *P* **73** *L* **15** # 136

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

It is usefull to allow higher Inrush current than 450mA after TBD time from POWER UP start for the following reasons:
a)Reach faster startup with lower probability for startup oscilations
b)Handle different load behaviour during startup that is time dependent e.g1: Adress the issue of some PDs that turn ON full power during POWERUP. e.g.2: Supports PDs with high input capacitance to reach steady state faster.
I doesnt add any burden on PSE as PSE move from Inrush limits to ILIM any way.
See darshan_02_0715.pdf

SuggestedRemedy

Add the following text after line 36.

The maximum inrush current sourced by the PSE per pair set may exceed the per pair set PSE inrush template in Figure 33–13 only TBD msec after POWER UP has started and shall not excedd ILIM-2P maximum as specified by Table 33-11 item 9.

Proposed Response *Response Status* **W**

I asked for a presentation on this for July. Is there one?

Cl **33** *SC* **33.3.1** *P* **80** *L* **47** # 145

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **X** *Pres: PD PI*

New PD Types will need to accept up to 57V on each pair set. Fix text,
The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

SuggestedRemedy

Replace the Draft text with,
Type 1 and Type 2 PDs shall withstand any voltage from 0 V to 57 V at the powered pair set indefinitely without permanent damage. Type 3 and Type 4 PDs shall withstand any voltage from 0 V to 57 V on both pair sets indefinitely without permanent damage.

Proposed Response *Response Status* **W**

Waiting for Presentation

See comment 189, 5

Cl **33** *SC* **33.3.1** *P* **80** *L* **47** # 189

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **X** *Pres: PD PI*

The following sentence is ambiguous:

"The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage."

SuggestedRemedy

Presentation forthcoming.

Proposed Response *Response Status* **W**

Waiting for Presentation

See comment 5, 145

Cl **33** *SC* **33.3.1** *P* **80** *L* **47** # 5

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X** *Pres: PD PI*

Maintenance Request #1274 on behalf of George Zimmerman, CME Consulting/LTC

Text in the existing standard is ambiguous and is inconsistent with terminations and usage commonly found in Ethernet equipment. The intent is to require PDs to be able to withstand application of common-mode PoE voltage. Application of 57V DC voltages in across the pins corresponding to the two pairs twisted differentially to form a balanced pair of the link segment would run a DC current across the transformer windings commonly found in BASE-T Ethernet equipment and burn them out.

SuggestedRemedy

Change: The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.
To: The PD shall withstand any common-mode voltage from 0 V to 57 V applied to any two sets of two pins at the PI indefinitely without permanent damage. The two pins in each set shall correspond to the balanced twisted wire pairs of the connected link segment.

Proposed Response *Response Status* **W**

Waiting for Presentation

See comment 189, 145

Cl **33** *SC* **33.3.7** *P* **94** *L* **23** # 219

Dwelley, David Linear Technology

Comment Type **TR** *Comment Status* **D** *Pres: Inrush*

Table 33-18 item 5: This places a new inrush requirement on Type 1/2 PDs when connected to a Type 3/4 PSE - can't do this

SuggestedRemedy

Move _2p text to item 5a, add PD Type "3,4"
Restore original item 5 from AT

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is not a new requirement as we have now increased the max inrush current from 400mA total to 400mA per pairset (800 total). However, we do need to make sure this is in alighnment with the PSE inrush numbers.

If PDs are limited to 400mA per pairset, they will work with existing Type 1 and Type 2 PSEs that supply at least 400mA over a single pairset.

Cl **33** *SC* **33.3.7** *P* **94** *L* **48** # 106

Jones, Chad Cisco

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

HOLD OVER for Dave Dwelley:
Table 33-18, item 9: Change to "per pair set capacitance" allows 360uF. We changed this to 180uF per Straw Poll 2 in Pittsburgh.

SuggestedRemedy

Change back to "PD capacitance"
Chair note: This is done? It's now called "PI capacitance during MDI_POWER states" and "C_port"

Proposed Response *Response Status* **W**

Wait for presentation

Cl **33** *SC* **33.3.7.3** *P* **90** *L* **43** # 139

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

The following comment adresses Iinrush in Table 33-11 item 5a and PD Cport max to be supported by PSE Iinrush. Since both parameters aretied together, they are adressed at the same comment.
See detailes in darshan_02_0715.pdf titled: Type 3 and 4 PD Cport_max to be supported by PSE Iinrush_min.

SuggestedRemedy

1. No changes to Table 33-11 item 5a Iinrush. It is in line with the work done on September 2014.
2. For capacitance valuse for Type 3 and 4 for SS and DS PD:
see darshan_02_0715.pdf.

Proposed Response *Response Status* **W**

Waiting for presentation.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **27** # 134

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

33.3.7.3 Input inrush current
Inrush current per pair-set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in Table 33-18, and ending before TInrush-2P min per Table 33-11. After TInrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level.

The time point when PD Inrush is ending is not function of PSE Tinrush Timer.
It is only a function of the PD internal design that regardless of the choices it has to use Cport between 5uF to 180uF e.g. for Type 1 and 2 and load current of up to 350mA during POWERUP phase, it has to complete Iinrush within 50msec which is the number equivalent to Tinrush_min at Table 33-11 which is a PSE requirements.
See detailed analysis in darshan_01_0715.pdf,
titled: "Only PD affects PD POWERUP Tinrush max (Not the PSE Tinrush Timer).

SuggestedRemedy

See detailed analysis and updated suggested remedy in darshan_01_0715.pdf.

Change lines 26-27 from:
"Inrush current per pair set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in To:
"Inrush current per pair set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in Table 33–18, and ends when Vport_PD-2P reaches steady state within time duration TInrush-2P min per Table 33–11. After TInrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level."
"

Proposed Response *Response Status* **W**

waiting for presentation.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **28** # 216

Dwelley, David — Linear Technology

Comment Type **TR** *Comment Status* **D** *Pres: Inrush*

"After TInrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level."

PDs are limited to power, not current, in POWER_ON mode. SS PDs are treated differently in this regard than DS PDs are.

SuggestedRemedy

Change to: "After Tinrush-2P min, a single-signature PD shall not exceed the power level, Pclass_pd, corresponding to its class level."
"After Tinrush-2P min, a dual-signature PD shall not exceed its per pairset power level, Pclass_pd, corresponding to the class level advertised at that pairset."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Change to: "After TInrush-2P min, the PD shall meet Pclass_pd as specified in Table 33-18."

Should we fix in the 33.3.7.2?

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **39** # 236

Yseboodt, Lennart — Philips

Comment Type **ER** *Comment Status* **D** *Pres: Inrush*

The following three statements in D1.1 are correct but highly misleading:
"Input inrush current at startup is limited by the PSE if C_Port per pair set < 180 mF, as specified in Table 33-11."
"If C Port per pair set >=180 mF, input inrush current shall be limited by the PD so that I Inrush_PD per pair set max is satisfied."
"NOTE-- C port per pair set is the C port seen by an attached PSE on two twisted pairs"

The note changes the technical meaning of the first two statements.

SuggestedRemedy

"For single-signature PDs, the input inrush current at startup is limited by the PSE if C_Port < 180 uF, as specified in Table 33-11."
"For dual-signature PDs, the input inrush current at startup is limited by the PSE if C_Port per pair set < 180 uF, as specified in Table 33-11."
"A single-signature PD with C_Port > 180uF, or a dual-signature PD with C_Port > 180uF shall limit the input inrush current
below I_Inrush_PD-2P max."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Wait for presentation

"For single-signature PDs, the input inrush current at startup is limited by the PSE if C_Port < 180 uF, as specified in Table 33-11."
"For dual-signature PDs, the input inrush current at startup is limited by the PSE if C_Port per pair set < 180 uF, as specified in Table 33-11."
"A single-signature PD with C_Port > 180uF, or a dual-signature PD with C_Port per pair set > 180uF shall limit the input inrush current
below I_Inrush_PD-2P max."

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **39** # 46

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **X** *Pres: Inrush*

"Input inrush current at startup is limited by the PSE if C_Port per pair set < 180 mF, as specified in Table 33-11."
Cport is not defined in Table 33-11

SuggestedRemedy

Cport is defined in Table 33-18. Change reference.

Proposed Response *Response Status* **W**

waiting for presentation.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **46** # 153

Schindler, Fred — Seen Simply

Comment Type **ER** *Comment Status* **D** *Pres: Inrush*

The PD inrush requirements are dependent on PSE operations that are not disclosed in the PD section.

SuggestedRemedy

Add the following note above the existing note on line 46.

NOTE-PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or when PSE time Tinrush expires. See 33.2.7.4 for PSE details.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Add the following note above the existing note on line 46.

NOTE-PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or when PSE time Tinrush expires. See 33.2.7.4 for details.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **47** # 125

Picard, Jean — Texas Instruments

Comment Type **TR** *Comment Status* **D** *Pres: Inrush*

The note needs some clarifications, Cport is the capacitance the PSE will see during inrush and operation.

SuggestedRemedy

Cport per pair set is the port capacitance seen by an attached PSE during startup and steady-state operation on two twisted pairs.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Cport per pair set is the port capacitance seen by an attached PSE during startup and steady-state operation on a pair set.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **48** # 135

Darshan, Yair — Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

(WAS ALSO IN D1.0 COMMENT #334)
We don't want to wait 50- 75msec in Type 3 and 4 systems for Iinrush to be ended if not required due to measuring PD voltage/current/time profile by the PSE and knowing that it was ended earlier.
In some large mutiport systems time for all ports to be ON is affected by Tinrush*N. N number of ports and PSE power supply power capability and its response to dynamic load behavior.

SuggestedRemedy

Withdrawn comment #334 from D1.0.

Proposed Response *Response Status* **W**

Waiting for presentation.

Cl **33** *SC* **33.3.7.6** *P* **99** *L* **48** # 150

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D** *Pres: Transient*

New PD Types need to have their current demands constrained. The text region to be modified is,

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 PD with peak power draw that does not exceed PClass_PD max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after
TLIM min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current
limited voltage source is applied to the PI through a RCh resistance (see Table 33–1). The current
limit meets Equation (33–14) and the voltage ramps from VPort_PSE min to VPort_PSE max at
2250 V/s.

A Type 2 PD shall meet both of the following:
a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 ?, and a source that supports a current greater than 2.5 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE min to 56 V at 2250 V/s, the source impedance is RCh (see Table 33–1), and the voltage source limits the current to MDI ILIM per Equation (33–14).

SuggestedRemedy

Replace referenced Draft text starting on line 48 with,

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. Type 2, Type 3, and Type 4 PDs,
with peak power draw that does not exceed PClass_PD max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

- The input current for Type 1 and Type 3 PDs consuming less than class-4 power levels, shall not exceed the PD upperbound template (see Figure 33-18) after TLIM min (see Table 33-11 for Type 1 and Type 3 PSEs) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33-1). The current limit meets Equation (33-14) and the voltage ramps from VPort_PSE min to VPort_PSE max at 2250 V/s.

A Type 2, Type 3 PDs consuming more than class-4 power levels, and Type 4 PDs, shall meet both of the following:
a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33-18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 [ohms], and a source that supports a current greater than 2.5 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE min to 56 V at 2250 V/s, the source impedance is RCh (see Table 33-1), and the voltage source limits the current to MDI ILIM per Equation (33-14).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace referenced Draft text starting on line 48 with,

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. Type 2, Type 3, and Type 4 PDs,
with peak power draw that does not exceed Pclass_PD max and has an input capacitance of 180 µF (TBD) or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

- The input current for Type 1 and Type 3 PDs consuming less than class-4 power levels, shall not exceed the PD upperbound template (see Figure 33-18) after TLIM min (see Table 33-11 for Type 1 and Type 3 PSEs) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33-1). The current limit meets Equation (33-14) and the voltage ramps from Vport_PSE min to Vport_PSE max at 2250 V/s.

Type 3 PDs consuming more than class-4 power levels, and Type 4 PDs,
shall meet both of the following:
a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33-18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 [ohms], and a source that supports a current greater than 2.5 A.

B) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from Vport_PSE min to 56 V at 2250 V/s, the source impedance is RCh (see Table 33-1), and the voltage source limits the current to MDI ILIM per Equation (33-14).